


Doctoral Dissertation
Doctoral Program in Electronic Engineering (30^{th} cycle)

Variability analysis of FinFET AC/RF performances through efficient physics-based simulations for the optimization of RF CMOS stages

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Summary

A nearly insatiable appetite for the latest electronic device enables the electronic technology sector to maintain research momentum. The necessity for advancement with miniaturization of electronic devices is the need of the day. Aggressive downscaling of electronic devices face some fundamental limits and thus, buoy up the change in device geometry. MOSFETs have been the leading contender in the electronics industry for years, but the dire need for miniaturization is forcing MOSFET to be scaled to nano-scale and in sub-50 nm scale. Short channel effects (SCE) become dominant and adversely affect the performance of the MOSFET. So, the need for a novel structure was felt to suppress SCE to an acceptable level. Among the proposed devices, FinFETs (Fin Field Effect Transistors) were found to be most effective to counter-act SCE in electronic devices. Today, many industries are working on electronic circuits with FinFETs as their primary element.One of limitation which FinFET faces is device variability.

The purpose of this work was to study the effect that different sources of parameter fluctuations have on the behavior and characteristics of FinFETs. With deep literature review, we have gained insight into key sources of variability. Different sources of variations, like random dopant fluctuation, line edge roughness, fin variations, workfunction variations, oxide thickness variation, and source/drain doping variations, were studied and their impact on the performance of the device was studied as well. The adverse effect of these variations fosters the great amount of research towards variability modeling.

A proper modeling of these variations is required to address the device performance metric before the fabrication of any new generation of the device on the commercial scale. The conventional methods to address the characteristics of a device under variability are Monte-Carlo-like techniques. In Monte Carlo analysis, all process parameters can be varied individually or simultaneously in a more realistic approach. The Monte Carlo algorithm takes a random value within the range of each process parameter and performs circuit simulations repeatedly. The statistical characteristics are estimated from the responses. This technique is accurate but requires high computational resources and time. Thus, efforts are being put by different research groups to find alternative tools. If the variations are

small, Green's Function (GF) approach can be seen as a breakthrough methodology. One of the most open research fields regards "Variability of FinFET AC performances". One reason for the limited AC variability investigations is the lack of commercially available efficient simulation tools, especially those based on accurate physics-based analysis: in fact, the only way to perform AC variability analysis through commercial TCAD tools like Synopsys Sentaurus is through the so-called Monte Carlo approach, that when variations are deterministic, is more properly referred to as incremental analysis, i.e., repeated solutions of the device model with varying physical parameters. For each selected parameter, the model must be solved first in DC operating condition (working point, WP) and then linearized around the WP, hence increasing severely the simulation time. In this work, instead, we used GF approach, using our in-house Simulator "POLITO", to perform AC variability analysis, provided that variations are small, alleviating the requirement of double linearization and reducing the simulation time significantly with a slight trade-off in accuracy. Using this tool we have, for the first time addressed the dependency of FinFET AC parameters on the most relevant process variations, opening the way to its application to RF circuits.

In this thesis, Chapters 2 and 3 are oriented towards developing the literature about FinFETs and the variability issues affecting the device performance. Chapter 4 embodies the novel Green's Function approach for AC sensitivity analysis of FinFET device. Chapter 5 focuses on the AC sensitivity analysis of a single and a double fin shorted-gate FinFET in response to the variations, with the help of the efficient GFs approach validation with the conventional incremental approach. In Chapter 6, we studied the behavior of the Local Variability Sources (LVSs) inside the device regions to understand the source of variations from different device regions. LVS provides more direct insight into device regions, i.e., pinpoint regions of the device sensitive to the respective variation in process parameters. Chapter 7 is dedicated to the AC sensitivity analysis of Independent Gate (IG) FinFET using the concept of sensitivity charts. Chapter 8 is oriented towards the optimization of a mixer conversion gain along-with variability minimization using sensitivity charts. Finally, Chapter 9 includes concluding remarks and future recommendations.

This work is ultimately dedicated to the successful implementation of RF stages in commercial applications by incorporating variability effects and controlling the degradation of AC parameters due to variability. We exploited the POLITO (in-house simulator) limited to 2D structures, but this work can be extended to the variability analysis of 3D FinFET structure. Also variability analysis of III-V Group structures can be addressed. There is also potentiality to carry out the sensitivity analysis for the other source of variations, e.g., thermal variations.

Acknowledgements

First and foremost, I would like to express my deep and sincere gratitude to my supervisor, Dr Simona Guerrieri Donati, for her continuous support and encouragement throughout this research. Without her guidance as a great mentor, this work would not have been possible. I am also deeply grateful to her being patient with me throughout this research. She provided me with lots of good advice and clear guidance throughout my PhD. Her wide knowledge, understanding and encouragement provided me with a good basis for the thesis. I am really indebted to her for the valuable knowledge that she gave me throughout this research. I will also like to mention her contribution during the write-up of this thesis and dedicating her time during write-up process to meet the deadlines.

I would also like to thank my father and mother for the continuous support they have given me throughout my life, from the day I was in secondary school to the graduate school.

I also want to thank my wife for her unconditional support for her constant presence in my life, during the good as well as tough days and also being supportive and understanding during my PhD. Without my wife, nothing of what I have done was ever possible.

I would like to dedicate
this thesis to my Son

List of Publications

Journals

[1] Ahsin Murtaza Bughio et al. "Multi-gate FinFET mixer variability assessment through physics-based simulation". In: IEEE Electron Device Letters 38.8 (2017), pp. 1004–1007.

[2] Ahsin Murtaza Bughio et al. "Variability of FinFET AC parameters: A physics-based insight". In: International Journal of Numerical Modelling: Electronic Networks, Devices and Fields (2017).

Conferences

[1] Ahsin Murtaza Bughio et al. "Physics-based modeling of FinFET RF variability". In: Microwave Integrated Circuits Conference (EuMIC), 2016 11th European. IEEE, pp. 237–240. isbn: 2874870447.

[2] Ahsin Murtaza Bughio et al. "Physics-based modeling of FinFET RF variability under Shorted-and Independent-Gates bias". In: Integrated Nonlinear Microwave and Millimetre-wave Circuits Workshop (INMMiC), 2017. IEEE. 2017, pp. 1–4.

[3] Ahsin Murtaza Bughio et al. "RF sensitivity analysis of independent-gates FinFETs for analog applications exploiting the back-gating effect". In: (2017), pp. 256–259. doi: 10.23919/EuMIC.2017.8230708.

Posters

[1] Ahsin Murtaza Bughio et al. "Physics-based analysis of FinFET RF variability including parasitics". In: Associazione Gruppo Italiano di Elettronica (2016).

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Chapter 1

Introduction

The electronics technology is evolving dynamically in every sector of life. With the advancement in the technology, the industry has no longer remained homogeneous; the continuous quest for new knowledge, development, and innovation is surging. The semiconductor industry has experienced an expeditious development in the course of recent decades [1], which has enabled unrestrained scaling of micro/nano-electronic devices. Since the introduction, the cutting-edge manufacturing technologies and modernization of field-effect transistor (FET) design have improved performance, cost, and compactness in modern day chips. The devices which were sized 10 μm in 1970 have shrunk to as low as 7 nm in 2017, e.g., by IBM, gate all around transistor using the extreme ultraviolet (EUV) technology [2]. The FET design has gone through some of the most spectacular changes within the past decade, including Ultra-Thin Body (UTB) or Silicon On Insulator (SOI) technologies [3], implementation of high-K gate stacks [4] and compressing silicon channels with strained-silicon channels [5] aiming at sub-0.1 μm generations. This change in design is driven by issues regarding dissipation of standby power and speed limitations. The 22 nm node has recently seen commercial influx towards 3-D multi-gate (MG) FETs in 2011 [6]. This step was seen as a significant shift from the planar technologies since Moore's Law, proposed by Gordon Moore as a universal Industry driver. Despite over the years, there have been major advancements in spanning the life of silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) technology, radical innovations are still required to continue scaling into the nanometer technologies. Improvements are needed in various aspects of FET designs including the operational control mechanism or the structural configuration, for which many innovative technologies have been proposed. These innovative technologies and enhancement in the structural configuration intends to improve the electrostatic control of the gate over the channel region to increase overall transistor performance (fast switching, low leakage, reliable), and may involve the use of quasi 1-D nanowires (NWs), carbon nanotubes (CNTs), or 2-D sheet materials such as graphene for the semiconducting channel. Whereas improvements in operational

control mechanism intended to circumvent some physical limitation such as carrier velocities in silicon channel, the sub-threshold swing limit, or source/drain junctions in emerging CMOS devices as well as in novel silicon devices such as FinFETs. Academia and industry are currently involved in active research in investigating the performance of devices using technologies like tunnel FETs (TFETs), heterogeneous integration of Group IV/III-V FETs, junction-less FETs (JL-FETs) and nano-wire FinFETs.

Process variations, however, face the challenges associated with manufacturing and design features of incorporating new technologies. The reduction in sizes of devices makes variability, a significant concern for an integrated circuit (IC) at the nanometer scale. Sources of variability in transistors include line edge or width roughness (LER/LWR), random dopant fluctuation (RDF), oxide thickness variation (t_{ox}), fin thickness variations (W_{fin}), work function variation (WFV), and many others. The forms of variability when included in real designs, tend to demonstrate unpredictable behaviors and performance, merely due to the fluctuations in the performance of individual or supposedly identical devices. Although various researches have been conducted on the effects of variability in planar CMOS technology, the designers are still encountering issues which are getting worse for future generations. The most concerned vulnerability associated with the semiconductor industry now-a-days is deciding on innovative technology solutions that deem fit for future commercial adaptability. The performance of post-CMOS technologies (e.g., multi-gate FinFET) have witnessed a brisk rise in publications in recent years. Regardless of that, there is indecisiveness about whether or not certain technologies should value manufacturability outlook, particularly considering the ramifications of process variability found in present-day foundry instruments. The study of these devices and their behavior should be before their implementation addressed on a commercial scale. Monte-Carlo-like simulations are used to predict the device behavior based on the principle of repeated device simulations:Monte Carlo analysis takes random combinations of parameter values chosen from the range of each process parameter. The result is an ensemble of responses from which the statistical characteristics are estimated. Monte-Carlo requires a huge number of simulations/iterations to accurately predict the device characteristics, subject to process variations which are ultimately very time consuming and requires high computational resources. An alternative technique to estimate device variability is GF based [7]. These techniques come with the advantage of reduced computational resources and are very time efficient in comparison to Monte-Carlo method. GFs approach has also been recently demonstrated for AC variability [8].

1.1 Statement of Problem

The purpose of this thesis is to study, using numerical simulations, different sources of intrinsic parameter variations in a Double Gate(DG) FinFET as a 2D cross section of advanced FinFET technology, typically the sub-50 nm technology node. It will focus on the introduction of different sources of parameter variations into a device simulation and will study the effect that each source has on the behavior and performance of a FinFET focusing on the AC response. Further, to show the application of this analysis, we present the variability-aware optimization of a RF CMOS stage, i.e., CMOS Mixer.

This work focuses on the variability analysis for the most effective parameters of FinFET device. The AC parameters such as transconductance and output conductance are the basic parameters that are affected by the fundamental uncertainty of technological parameters, like the uncertainty in the lithography process and other device fabrication steps (e.g., the etching) and the doping uncertainty. The lithography and etching problem affects the precise definition of the device size and dimensions collectively named geometric variations. All those errors are inherently linked to the aggressive downscaling of the device volume and way out from these limitations of the current technology are not easy to foresee at the moment. Basic sources of variability are also work function variations, oxide thickness variations, fin width variations, source/drain doping variations etc. In this work, the effect of these sources of variations on the FinFETs is studied.

Despite the enormous amount of work dedicated to the fabrication, optimization, and modeling of these devices, comparably less effort has been dedicated to their AC characterization and modeling, although the interest towards analog Radio Frequency (RF) and microwave applications fosters research in this field. On the other hand, the peculiar 3D device structure brings along a considerable amount of parasitic capacitances and resistances, which may impair, in RF applications, the advantages brought by the gate length reduction. Since variability is known to significantly impact DC device behavior, the same is expected for AC performance, both at the active device and at the parasitics level. Some of the variations (geometrical) may have a mild effect on the DC performance of the device, but can affect, e.g., the capacitances related to the device, i.e., AC performance. It is therefore mandatory to assess reliable and efficient tools allowing for the evaluation of AC performance variations as a function of the most important physical parameters of the FinFET structure.

A detailed literature review in the area of process variations in FinFETs leads to the conclusion that in the current scenario, it is essential to take a look at the AC performance of the FinFET device through an improved approach. For accurate variability estimation, GF based techniques are widely used [7], especially for ultra-scaled CMOS devices [9], since they retain the link to the physical device insight with extremely reduced simulation time and with an accuracy comparable to the

more numerically intensive Monte Carlo approaches.

This work addresses the need for efficient tools to perform AC analysis of the FinFET and also present *sensitivity charts* as a tool to study the RF performance enabling the direct comparison of both parameter variations and Y parameters, in terms of relative variation in AC parameter in response to the percent variation in the parameter. Sensitivity charts are further exploited to optimize the RF mixer. In fact, like any other electronic device, mixers are also prone to variability. In this thesis, we will present sensitivity chart technique to circumvent the parameter variations and predict the device voltage which can offer least variance in conversion gain.

1.2 Thesis Outline

The structure of this thesis is divided into three parts. The first part chapter 2-4 address the problem of variability in FinFETs and reviews the modeling approach based on GF. Chapter 5-7 are dedicated to the analysis of AC variability in relevant Independent gate(IG) FinFET. Chapter 8 is finally dedicated to the application example, i.e., mixer design robust to process variations. More in detail:

- **Chapter 2**: In this chapter, the multigate devices will be reviewed with its background. The peculiarities of FinFET device structure and parasitics related to it are also presented.
- **Chapter 3**: This chapter is dedicated to the concept of variability and its sources. We categorized the variability into AC and DC variability. These variabilities are studied with respect to the variation in relevant technological parameters.
- **Chapter 4**: The idea of GF is discussed and its implementation into basic physical models is also under focus in this chapter.
- **Chapter 5**: This chapter is dedicated to AC analysis of Single Fin FinFETs and Double Fin FinFETs, with the focus on the verification of GFs.
- **Chapter 6**: This chapter focuses on the GFs ability to address the device regional sensitivities. LVS portray the internal sources of AC parameter variations and paves the way to true device optimization.
- **Chapter 7**: This chapter is dedicated to the AC variability analysis of IG DG FinFET. This chapter also introduces the concept of *sensitivity charts* for relative sensitivities of the device.

- **Chapter 8**: In this chapter, we will turn our focus to RF mixers, implemented with IG FinFETs. RF mixer optimization using the sensitivity charts is also discussed in this chapter.
- **Chapter 9**: This chapter provides the summary and conclusion of this thesis. This chapter also discusses the future recommendations.

Chapter 2

FinFETs and Multi-Gate Devices

An Italian scientist born in Como in 1745, Alessandro Volta, first discussed the term “semiconducting” in 1782 [10]. Michael Faraday, famous for his contributions in the field of electromagnetism, was the first person to observe a semiconductor effect in 1833 [11] [12]. In 1947, the first transistor was invented in Bell Labs [13]. So, by the passage of time, semiconductor technology evolved from the concept of diodes to transistors, and these devices can be found everywhere around us in the shape of computers, mobile phones, televisions, automotive systems, health and safety equipments.

The contribution of CMOS to the semiconductor industry cannot be ignored, the important element of CMOS technology being MOSFET, i.e., Metal Oxide Semicondutor Field Effect Transistor. In the start of 1980’s, the issue of sub-micron dimension was resolved with the advent of the high resolution electron, X-ray, molecular and ion-beam lithographic techniques; this reduction in sizes is to keep in line with Moore’s Law, i.e., after every three year, transistors linear dimensions are shrunk to the half of size. Currently, transistor technology has been reduced to 10 nm technology and recently even 7 nm and 5 nm transistors are proposed [14] [15]. Initially, transistors were manufactured on "mass" silicon wafers; however, a significant change was attained in 1990’s by modifying to a novel kind of substrate called SOI. In SOI, semiconductor layer such as silicon is formed on an insulator layer which may be a buried oxide (BOX) layer formed on top of a semiconductor substrate. As SOI’s devices have abridged parasitic capacitances and improved current drive, both switching speed of the circuit and power consumption/utilization will be improved with this technology. The downscaling of MOSFETs, below 50 nm is limited due to short channel effects (SCE), which degrades the overall performance of the device, see later. But, the never-ending need for downscaling of devices, forces the researchers to look for novel structures. FinFET can be seen as a possible alternative for MOSFETs, below 50 nm scale. FinFETs were first introduced in 2001 by Chenming Hu et al., where the channel of the device is surrounded by the gate to provide better control over the device, discussed in section

2.4 and hence, reduce SCE.

In this chapter, we will briefly review SCE. After understanding the need for alternative structures to suppress SCE, we will discuss different type of Multi-Gate FET devices. Then, we will turn our focus towards FinFETs and will discuss it in detail. We will discuss a brief history of FinFETs in section 2.4 and then will turn our focus towards the structure of Double Gate (DG) FinFET and it's two variants i) Short-circuited Gate Double-Gate FinFET and, ii) Independent Gate Double Gate FinFET.

2.1 Basic Concept of MOS devices

2.1.1 Short Channel Effects

The need for high speed transistors with reduced fabrication costs, is the main motivation behind transistor scaling. This reduction in transistor size, i.e., their length, makes the circuits smaller, which in turn increases the transistor count on the integrated circuits. However, as transistors are scaled below 50 nm, the reduced channel length becomes the same order of magnitude as the depletion layer widths of the source and drain junctions. With all their advantages, this scaling down of MOSFETs comes with their share of issues, called the SCE. SCE impacts the performance and the overall reliability of the device [16]. Due to SCE, the problem of fabricating more and more transistors on the chip would not be possible.

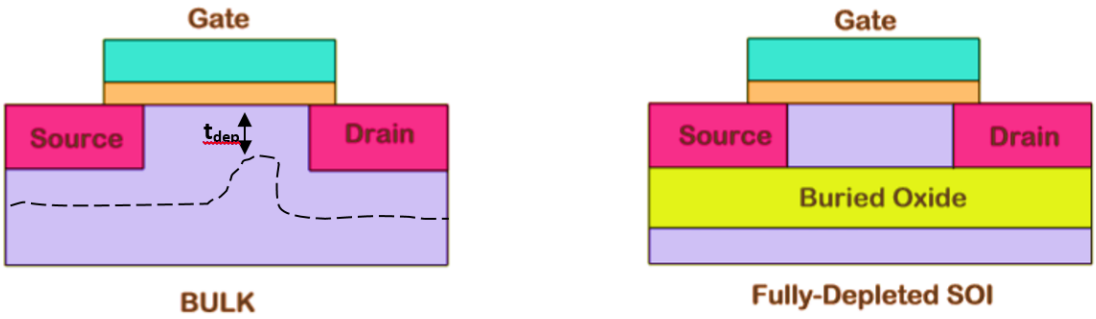

Figure 2.1: Bulk MOSFET and SOI MOSFET [17]

The electric field lines from drain to source reduces the gate control over the channel region: this effect of weakening control over the gate is SCE. Field lines propagate through the depleted junctions and affects the channel of the device. Their effect on the channel can be decreased, for instance, by increasing the doping concentration between source/drain regions. Nevertheless, the doping in scaled devices turns out to be extremely high (10^{19}) to allow proper functionality of devices. On the other hand, in Fig. 2.1, we have shown two different topologies of MOSFETs, one is the bulk and the other one is SOI.In SOI MOSFETs, the introduction

of buried oxide (BOX) can reduce the effect of electrical field lines on the channel region, but it also comes with its own price. These SOI devices have two main drawbacks, one is self-heating, which is due to the introduction of BOX(good thermal insulator) and other is the fabrication of thin body SOI wafers. In comparison to SOI devices, FinFETs, see later, offer high drive current and are more robust to SCE.

2.1.2 Drain Induced Barrier Lowering

The combined charge in the depletion region of the device and that in the channel of the device is balanced by three electrostatic charges: the gate, the source and the drain. As the drain voltage is increased, the depletion region of the *pn*-junction between the drain and the body increases in size and extends under the gate. So, the drain takes a greater portion of the burden of balancing the depletion region charge, leaving a smaller burden for the gate, which results in the lowering of threshold voltage V_{th}.

The DIBL (Drain Induced Barrier Lowering) effect is defined as "the decrease in threshold voltage when the drain voltage is increased from a low value $V_{ds,low}$ to a high value $V_{ds,high}$. If the barrier between the source and the channel is decreased, electrons are more freely injected into the channel region. Therefore, the threshold voltage is lowered and the gate has less control on the channel. The DIBL can be expressed as:

$$DIBL = V_{th}(V_{ds,high}) - V_{th}(V_{ds,low}) \tag{2.1}$$

2.1.3 Threshold roll-off

Among SCE, threshold roll-off is also very important parameter and is defined as: "as an effect where there is a decrease in threshold voltage with the decrease in channel length." At shorter channel length, the device turns on at lower gate voltage, which degrades the device performance, i.e., higher leakage current in comparison to a long-channel device. The voltage roll-off can be expressed by:

$$\Delta V_{th} = V_{th,longchannel} - V_{th,shortchannel} \tag{2.2}$$

2.1.4 Sub-threshold Swing

Another important factor is subthreshold swing, because it ultimately set the minimum values of power dissipation and power supply voltages. The sub-threshold swing is defined as the gate voltage required to change the sub-threshold drain current by one order of magnitude [decade]. The sub-threshold swing of the MOSFET

is proportional to $\frac{KT}{q}$ [18], i.e., 60 mV/decade at room temperature 300K. The subthreshold swing can be shown as:

$$SS = \left(\frac{\delta V_{GS}}{\delta log_{10} I_{DS}} \right) \tag{2.3}$$

With scaling, it has been seen that the sub-threshold swing increases which is a detrimental effect [19]. As the gate length deceases, the SS increases. The main approach is to optimize the value of the Sub-threshold slope to get the proper value of SS for which the device gives the better performance.

2.2 ITRS perspective

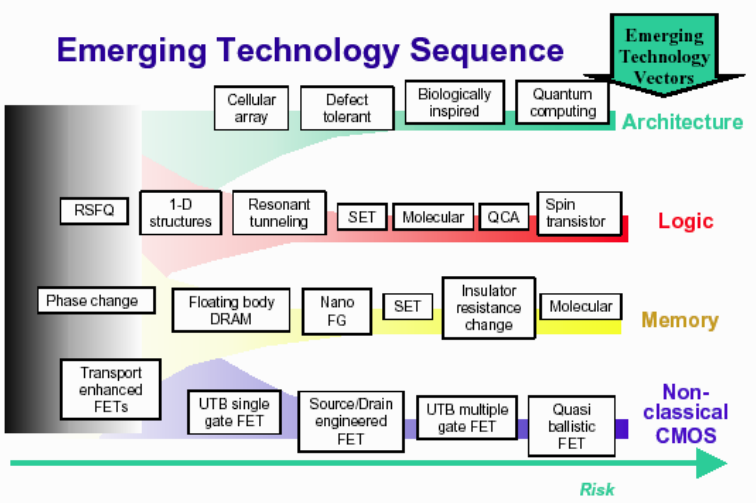

Figure 2.2: ITRS vision of emerging technology vectors and their applications. Adapted from the 2003 edition of the ITRS, Emerging Research Devices section, page 3.

The impact of downscaling on MOSFET devices fosters the need for the advancement in the electronic industry, like explained in 2.1.1.

This scaling of the electronic devices are limited by the challenges like SCE, tunneling through thin gate dielectrics, reduced sub threshold performance and the quantum effects. While the most aggressive scaling efforts have already produced sub-50 nm devices, it is already well understood that MOSFET's device performance is too limited at nano-scale and researchers have resorted to the novel device structures. In particular, as shown in Fig. 2.2, the International Technology Roadmap for Semiconductors (ITRS) in 2003, has identified several types of devices that could be the breakthrough technology replacing the classical CMOS devices.

Many devices have been proposed including UTB multigate FETs in Emerging Research devices in 2003 edition of 'ITRS' [20].

"Emerging Research Devices" chapter in ITRS documents [20], many devices were proposed, but most are actually a careful application of the idea of UTB multigate FET, where very thin transistor body is employed to ensure good electrostatic control of the channel by the gate in the "off" state [20].

2.3 Multi-Gate Transistors

Multi-Gate Transistors refer to a MOSFET incorporating more than a single gate in a single device. A single electrode may control more than one gates, depending on whether the surface of multiple gates operates by independent gate electrodes or as a single contact. Multi-Gate transistors depict a substitute to SOI MOSFETs that enhance the electric current and provide better control for SCE. DG transistors, Tri-gate transistors, Bulk FinFETs, Gate-All-Around transistors are few examples of Multi-Gate Transistors as shown in Fig. 2.3. The DG is basically a unique gate electrode present on opposite sides of a structure of device; same is the case in defining the "tri gate". For DG transistor, usually top side is hard masked, and the fin is controlled by the two gates from opposite sides, while in the triple gate, fin electrostatics are controlled by three gates. For "quadruple-gate", the gate is all around the rectangular fin. Whereas in Multiple-Independent Gate FET, usually two different gate electrodes can be influenced with different voltages across the gate terminals, also shown in Fig. 2.3. Bulk FinFETs, shown in Fig. 2.3 **f**, are built on bulk-Si wafers, which have less defect density and are cheaper than SOI wafers, and offers better heat transfer rate, but is limited in terms of power consumption, high parasitics capacitances, higher leakage currents in comparison to SOI technology [21] [22].

2.3.1 Early idea: Double-Gate MOSFET and FinFET

In 1984, Sekigawa and Hayashi published a pioneering paper on DG MOSFET [24]. The results showed that with the insertion of a Fully depleted (FD) SOI device between two gate electrodes, a huge reduction in SCE could be observed. This device cross-section's has resemblance with the Greek letter Ξ, hence the device is named as XMOS. Compared with the conventional SOI MOSFET, this configuration provides enhanced control in the depleted channel region; specifically, the effect of the electric field by the drain on the channel is less concentrated.

DELTA transistor was first invented, in 1989, formed with a thin and high silicon region known as "fin" [25]. Implementation of DELTA transistor is shown in Fig. 2.4. A FinFET is the modification of DELTA, having a similar structure to DELTA except for an oxide layer (hard masked) over silicon fin, allowing for a

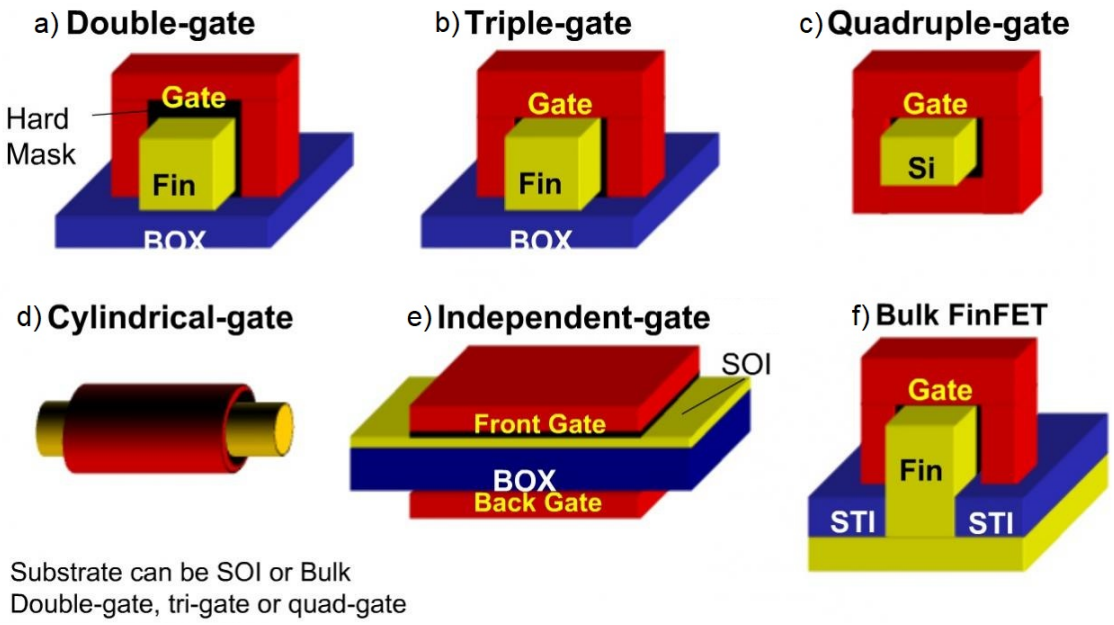

Figure 2.3: Example of MultiGate transistors [23]

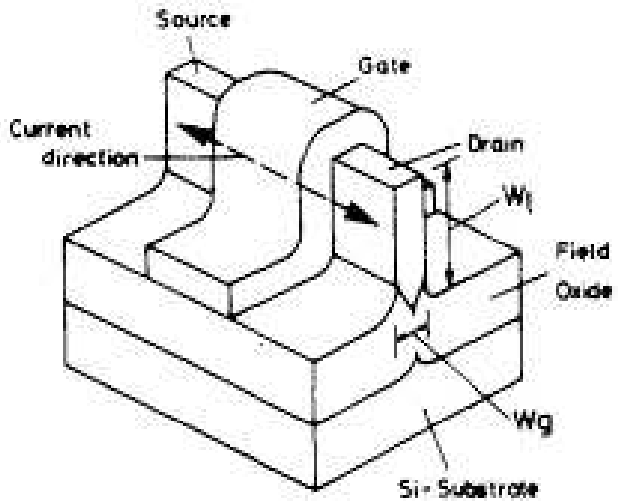

Figure 2.4: Delta Transistor "Fully DEpleted Lean-channel TrAnsistor" [25]

third channel on the fin top. In the high segments of the device, this hard mask, also averts the creation of parasitic channels in inversion corners of the device.

The researchers interest in the FinFET device, can be acknowledged from academia as well as from commercial manufacturers [26], Intel [27], and AMD [28] in the FinFETs. The interest in FinFETs is due to its capability of suppressing SCEs and having the high drive current. It is very important to note that most

research of the DG FinFET structure points to a need for ultra-thin body devices to ensure full depletion, high performance, and suppression of SCE. More specifically, research from the inventors of the device [29, 30], suggests that the fin width must be smaller than the gate length for optimal device performance. These findings also suggest that the fin width can be as large as 70% of the gate length to effectively suppress SCE, while more aggressive estimates place the maximum fin width at $\frac{1}{2}$ and $\frac{1}{3}$ of the gate length.

The detailed discussion about FinFET structure and operating principle is discussed in section 2.4.

2.3.2 Multiple-Independent Gate FET (MIGFETs)

The MIGFET is a double-gate device whose gate electrodes are insulated and the gates can have different voltages applied at their terminals as shown in Fig. 2.3. This feature of MIGFET has driven the attention of the scientific community towards the possibility of developing novel circuit topologies, both for digital as well as analog applications exploiting the independent gates. MIGFET has a unique feature of threshold voltage adjustment by having different voltages at the gate terminals, and this threshold voltage can be tuned as desired by the voltage choice. This effect is called back gating effect. In this back-gating effect, one of the gate terminals is tuned to adjust the threshold voltage [31][32]. Having independent gates, though, requires very complicated and advanced technologies to keep the gate metallization apart[33]. Hence, this technology is nowadays at the research stage.

2.3.3 Gate All around transistors (GAA)

GAA has a inherent feature of suppressing SCE by having a gate all around its structure as shown in Fig. 2.5. By having the gate around the device it enables even better control over the device and best control on the channel. In this structure, the channel can be cylindrical as well as rectangular. Despite, it is not compatible with standard planar technology, it has perspective interest for nanotechnologies based on nanowires. Therefore, it is the objective of intense research [34].

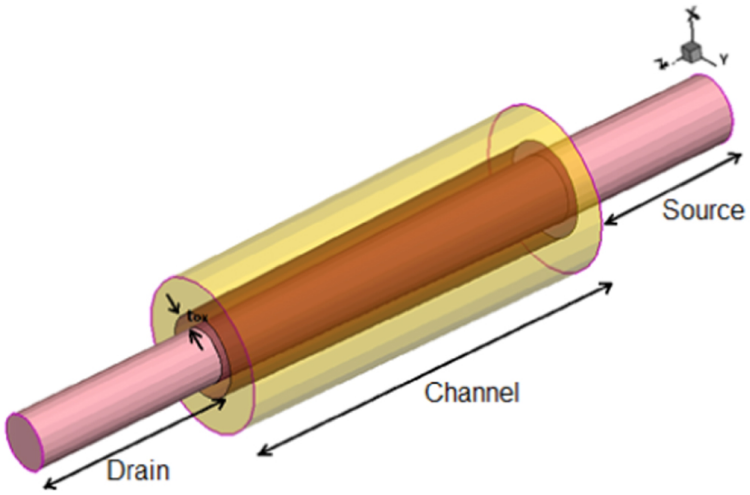

Figure 2.5: Gate All around [35]

2.4 FinFET Device

In this section, we will focus on the detailed discussion on FinFETs.

2.4.1 FinFET Device Structure

In this thesis, we focus attention on the state of art FinFET devices, commercially introduced by INTEL in 2011 and later by other manufacturers. The main feature of the FinFET structure is that the front and back gates are inherently self-aligned and the channels are in the sidewall of the silicon fin. Also, the fin body is lightly/undoped. Understanding FinFET device structure is very important to understand device performance and its vulnerability to process variations, which will be discussed in the next section. First, we will discuss the fabrication steps of FinFET development.

The most important fabrication steps are:

1. Fin formation
2. Gate stack formation
3. Source and drain extension implants
4. Spacer formation
5. Epitaxial raised source/drain formation
6. Deep source/drain implantation and activation anneal

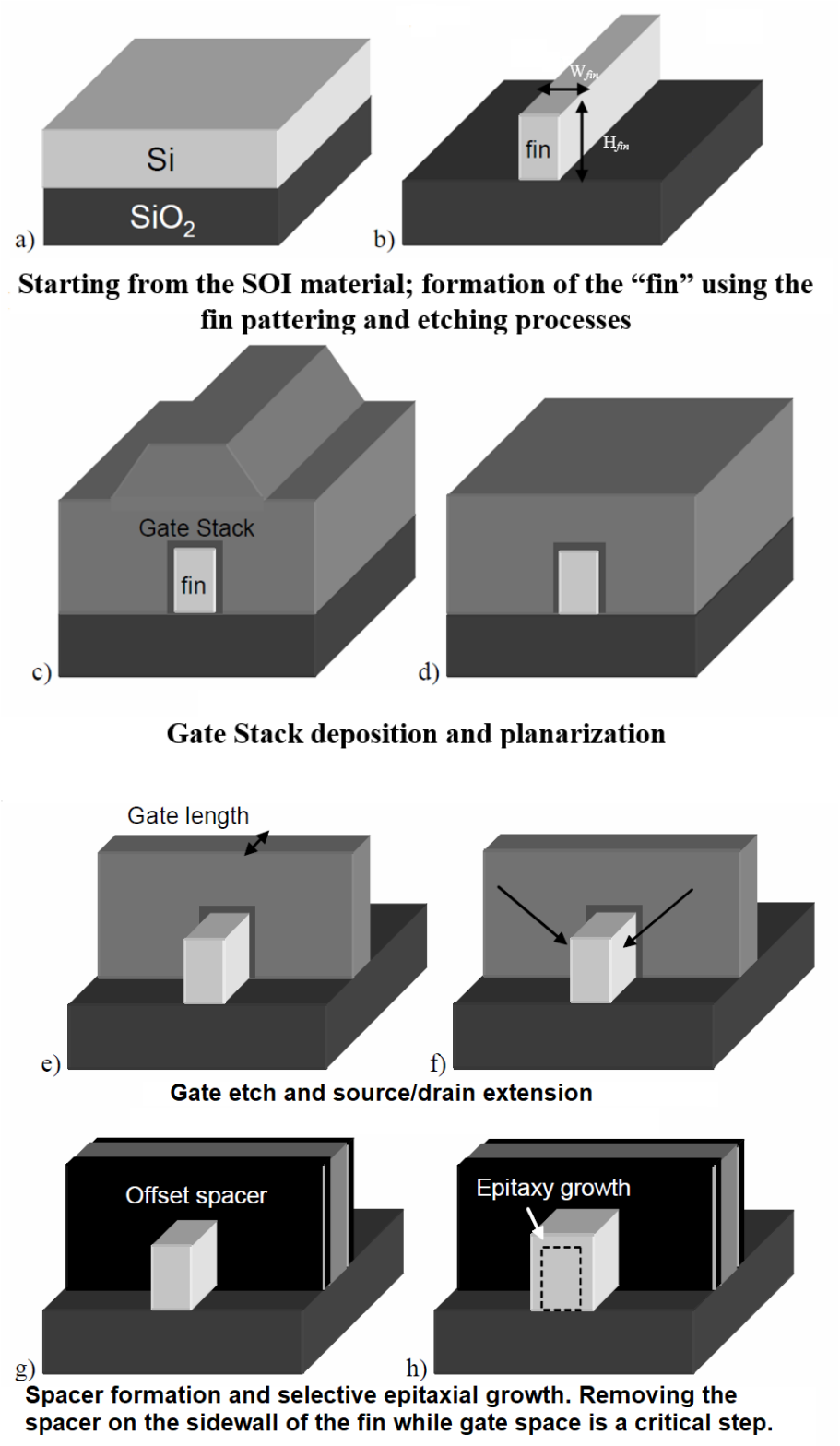

Figure 2.6: Fabrication sequence of FinFET [36]

The formation of FinFET tri-gate structure on an SOI substrate can be seen in Fig 2.6. The H_{fin} is the fin height. While W_{fin} is the thickness of the fin. The dimensions of the fin width are quite critical and its formation is done by the use of optical lithography or by the use of spacer image transfer (SIT) [37] [38], followed by plasma etching.

Post etching process, the sidewalls are rough and the process of oxidation and H_2 annealing are performed for the smoothness of the sidewall surfaces[40, 39]. After that, the gate dielectric is grown and the metal gate is deposited. It is suitable to tune the threshold voltage of the device by using a gate material that has the appropriate effective workfunction rather than by doping the channel. This is because, in conventional MOSFETs, V_{th} is tuned by the use the channel doping. While in the case of FinFET, the channel is usually lightly doped to suppress SCE, hence, it is preferable to tune the V_{th} with the help of gate workfunction.

Next step is the gate stacking over the fin, while depositing the gate material. After this step, planarization of the Gate stack is required, so that, the gate etching can be performed. Significant over-etch of the gate material is required to clear the bottom of the fins. As a result, the gate etch must have a high selectivity to the gate dielectric on top of the fin, if one wants to avoid damage to the fin during gate etch. Source and drain (S/D) extensions are formed after gate patterning using low-energy and large-tilt angled implants [41, 42]. Next, S/D offset spacers are formed along the sidewalls of the gate and fin. The sidewall spacers on the fins are subsequently removed to expose the fin to grow raised source and drain using selective epitaxy [**hang2006investigation**, 41]. The raised source and drain structure helps to reduce the parasitic resistance associated with thin fins [41].

2.4.2 FinFET's Principle of operation

The main concept for the development of FinFET was to suppress SCEs, when the device is scaled below 50 nm. The idea behind the FinFET structure is to have the gate capacitance closer to the channel of FinFET. The fin body is usually very thin, so that the gate has better control over the channel. To achieve this, the silicon body is very thin so that, no leakage path is far from one of the gates reducing leakage current. As the channel is controlled by two or more gates, they offer more control throughout the channel. The area which is least influenced by the gate, is the center of the Fin. The resulting structure of the FinFET is 3D by nature as it can be seen in Fig. 2.7.

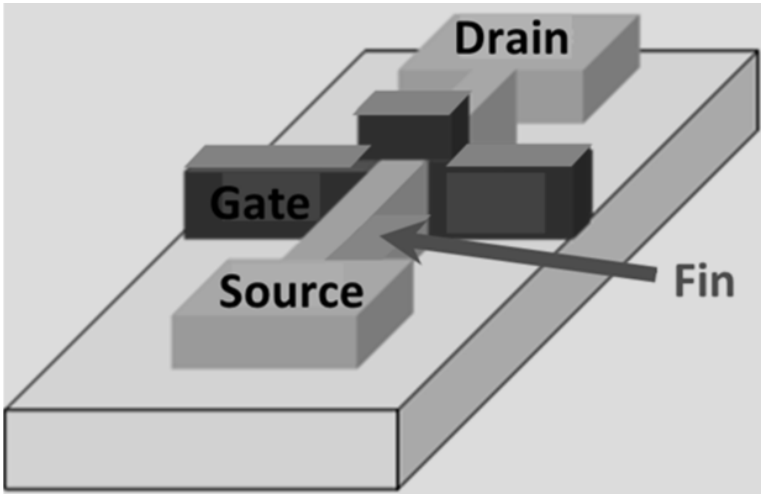

Figure 2.7: 3D structure of Triple Gate FinFET

The width/height of the channel controls the drive current of the FinFET. For example, increasing fin width W_{fin}, increases the current. Since, the current may turn out to be too low, it is conventional, especially in RF applications to enhance the drive current by increasing the number of fins. The multi-fin structure and cross-section can be seen in Figs. 2.8 and 2.9.

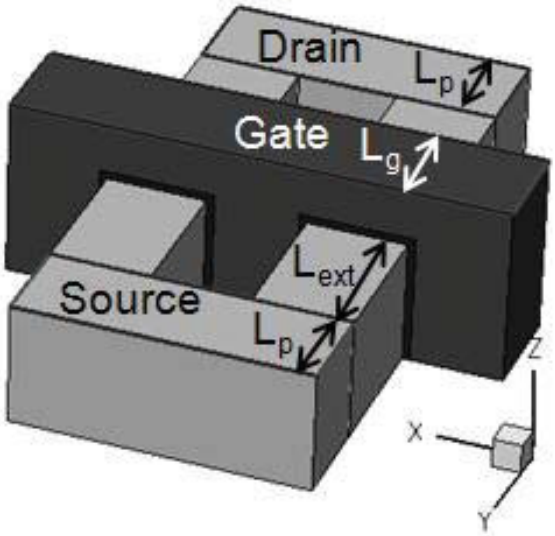

Figure 2.8: Schematic diagram of MultiFin FinFET structure: 3D view [43].

The parameters governing the structure are tabulated in table 2.1.

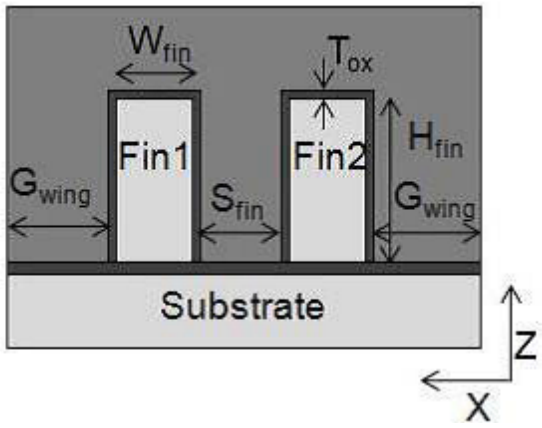

Figure 2.9: Schematic diagram of MultiFin FinFET structure: 2D cross section [43].

Table 2.1: Schematic definition of parameters shown in Fig. 2.8 and 2.9

Symbols shown in Fig.2.8 and 2.9	**Parameter**
L_g	Gate length
L_{ext}	Source/Drain extension length
L_p	Source/Drain pad width
G_{wing}	Gate extension Length for the fins located at the edge
S_{fin}	Spacing between the neighboring fins

2.4.3 Small-signal equivalent circuit of FinFET

In general, a definite advantage of physical simulations is that they don't require an equivalent circuit for RF characterization. Nontheless, a reference to possible small-signal equivalent circuits may be helpful to interpret the outcome of physical simulations.

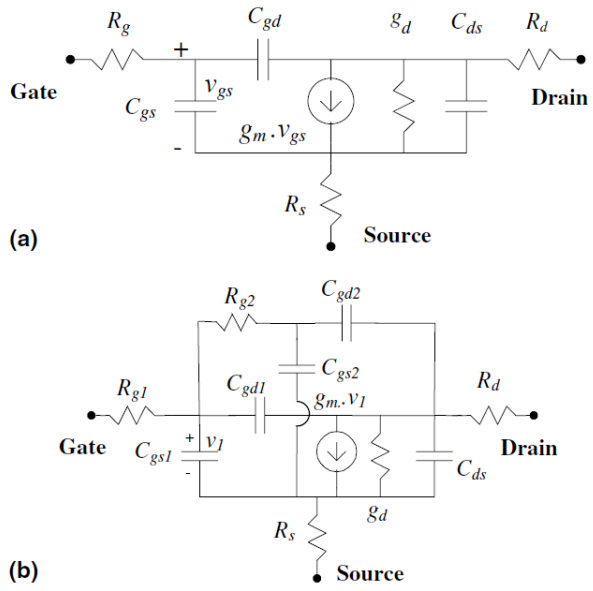

Figure 2.10: Small-signal equivalent circuits. **(a)** Conventional equivalent circuit for single gate FET. **(b)** Expansion of equivalent circuit to improve high frequency fitting for FinFET. [44]

The conventional small-signal model for high frequency FET can be applied also for FinFETs, provided the two gates are used as a single electrode. Modifications of the conventional topology for FinFETs have been proposed in many papers, e.g., Ref. [44] proposed, the slightly modified version of small signal equivalent model for FET devices shown in Fig. 2.10 (**b**). Lederer et al. showed that the conventional equivalent circuit in Fig. 2.10 can be used to model single-gate devices but such simple topology fails to accurately represent the FinFET device behavior. As reported in Fig. 2.10 (**b**), a parasitic RC network (i.e., R_{g2}, C_{gs2}, C_{gd2}) has been added to improve the behavior up to 110 GHz. Further, it should be noted that this is simplified equivalent circuit for FinFET and many effects are not included in this model, e.g., time delay caused by the DIBL is not incorporated.

Ref. [45] discussed, a lumped equivalent circuit network for modeling both open and short test structures and included its contribution in the FinFET model. Crupi et al. in [45] also emphasized on FinFETs superior SCE performance and pronounced the fact that the microwave performance of the FinFET is degraded by the contributions from the 3D FinFET structure. They also pointed the need for significant research interest toward FinFET devices to enhance high-frequency performance.

2.4.4 FinFET Parasitics

In the previous sections, we discussed about the FinFET structure and it's operation. In this section, we will discuss and give the basic idea about the FinFET parasitic resistances and capacitances. In FinFETs, the parasitic resistances and capacitances are of paramount importance, because, its magnitude is comparable to the channel resistance in scaled devices. Due to the FinFETs inherent 3D structure, the parasitics are very difficult to model.

Parasitic Resistances

Source/drain resistances along with the gate resistance are included in the parasitic resistance of a FinFET. The gate resistance is less influential than the source/drain resistances on the overall performance of the device. This is due to the recent innovation in gate technologies, i.e., using highly conductive metal as a gate contact. The gate resistance is in any case, due to the finite conductivity of gate material along with the reduced metal thickness. It is more influential on the AC behavior than the DC behavior of the device. In small-signal equivalent circuit of Fig. 2.10, R_g refers to the gate parasitics, and R_s and R_d points to the sources/drain resistances.

Similar to standard MOSFETs, the FinFETs source/drain resistance can be separated into three components [46], as shown in Fig 2.11:

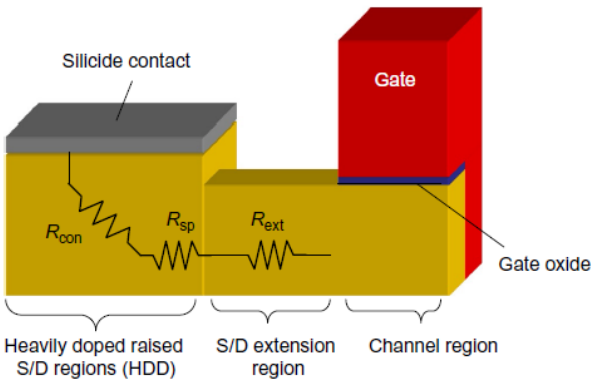

Figure 2.11: FinFET Source/Drain resistance distribution [46]

1. **Contact resistance (R_{con}):** The combined resistance due to the raised source/drain region bulk resistivity and the silicon/silicide interface resistance.

2. **Spreading resistance (R_{sp}):** The resistance due to current spreading from the source/drain extension into the raised source/drain. When current flows from the source/drain extension region into the raised source/drain region, it

spreads out gradually. Modeling of the increased resistance to such spreading is required and is performed usually as a new component, the spreading resistance. This spreading phenomenon is also known as current crowding.

3. **Extension resistance (R_{ext}):** The bias-dependent resistance in the thin source/drain extension region under the spacer. The modeling of extension resistance requires knowledge of the doping profile in the extension region, which is often not accurately known in reality. The profile shape varies depending on the process condition. In addition, surface accumulation due to the fringe field originating from the gate creates bias dependency.

Parasitic Capacitances

In addition to the standard capacitances like in CMOS, FinFET devices consist of additional parasitic contributions. These parasitic capacitances are divided in two different capacitances, i.e., overlap capacitance, C_{ov}, and the fringing capacitance, C_{fr}. We show how the fringe capacitance is separated into gate-to-fin, gate-to-contact components in the top and sides of the fin, as well as the corners. Each of these components are shown in Fig. 2.12

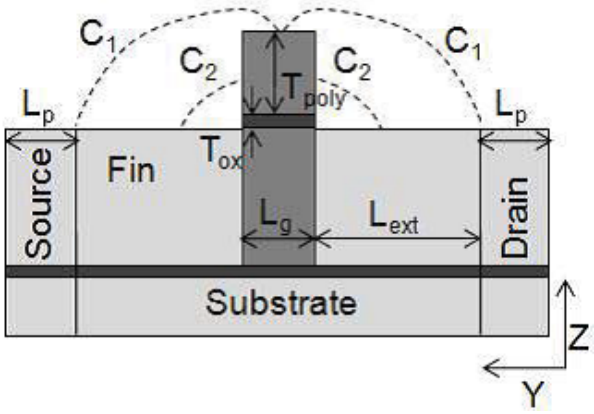

Figure 2.12: Fringe capacitances of the single FinFET

An analytical models for both the overlap and fringing capacitances are discussed in the later part of this chapter 3.2.

2.5 FinFET Configurations

Fig. 2.13 shows, the DG structure, as already mentioned, when introducing Multigate devices, we can select two relevant types of FinFET variants:

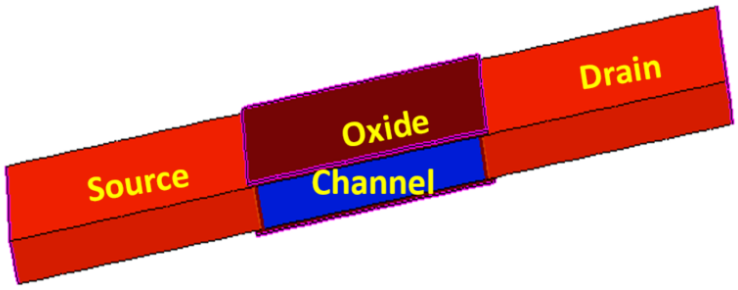

Figure 2.13: Double Gate MOSFET

1. **Short-circuited Gate(SG) DG FinFET:** In this type of topology, which is the most common and commercially developed, since, it represents the 2D cross-section of commercial tri-gate FinFETs, the gates are physically connected by unique metallization. In this configuration, we have the same voltage at both gates of the DG FinFET, as shown in Fig.2.14. The electrostatics of the devices in this configuration are controlled by both gates. This type of FinFET variant, offers higher on and off currents as compared to IG DG FinFETs, when having all the parameters same. They offer good transconductance and sub threshold performance as well.

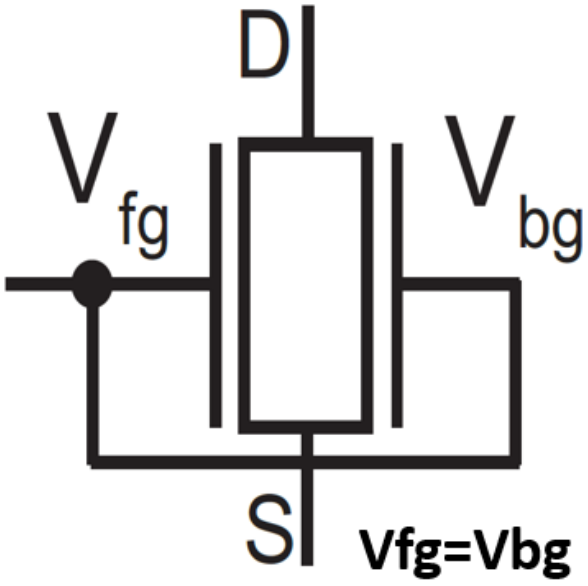

Figure 2.14: SG FinFET device configuration.

2. **Independent Gate(IG) Double Gate FinFET:** The gates are isolated physically in this topology, hence named, Independent Gate DG FinFET. We can have different voltages at the gate, i.e., the front gate voltage will

not be equal to the back gate voltage. Keeping the gate metallization apart requires more sophisticated technology and resources. But, it provide us with wide possibilities for analog circuit applications, specially tuning the threshold voltage, with the help of back gate bias. IG FinFETs require more space area, due to separate gate terminals.

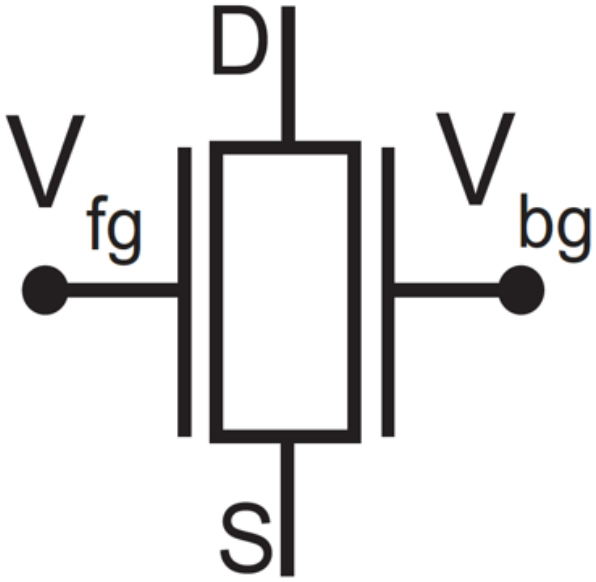

Figure 2.15: IG FinFET device configuration.

2.6 Summary

The ever increasing need for semiconductor electronic device downscaling and never ending approach to advancement motivates research towards Semiconductor industry. The need for development of novel FETs arouse from SCE, when the conventional devices were scaled below 50 nm. SCE take the toll on the device performance and affect the electrical parameters adversely, e.g., through threshold voltage, DIBL, SS, etc. The multigate transistors offer better control over channel and possess the inherent feature of suppressing SCE. Different multigate transistors are under study for commercial use. FinFETs have been widely accepted as the next generation transistors, offering scaling to sub-20 nm regime. But it also comes with different parasitics, which affects the performance of the FinFET. In this chapter, we have reviewed main FinFET concepts and operation, focusing in particular on two variants, the shorted gate and independent gate FinFETs. Both types have their own advantages.

FinFET, like any other MOSFET device, are also prone to device variability. Due to the fabrication of FinFETs in nano-scale, many process variations occur and they cannot be avoided. In the next chapter, we will focus on these peculiarities of FinFET device.

Chapter 3

Parametric variability and sensitivity in FinFET devices

When semiconductor devices are fabricated in the nano-meter regime, they are prone to variability in physical parameters due to technological limitation. In chapter 2, we reviewed the literature about multigate device. This chapter discusses the variability issues faced by semiconductor devices with special focus on FinFET devices. This chapter is divided into two parts: one is for DC variability analysis, while, the other is for AC variability analysis. The major part of this chapter is dedicated to the different sources of variability, e.g., fin variations, oxide variations e.t.c. These sources of variations and their effects on DC variability are reported. While in AC variability Section 3.2, we will discuss parasitic capacitance model with respect to fin variations, both with single as well as multifin structure. We also discussed the cutoff frequency response to relevant variability parameters.

FinFETs offers better performance in comparison to the conventional CMOS transistors. Both these devices are prone to variability. However, FinFETs are superior in comparison to MOSFETs due to its capability of current flow through the undoped channel. FinFETs lightly doped channel makes the channel less susceptible to the random fluctuation of dopants. But, FinFET is affected by the variations and is vulnerable to other variability issues. The fabrication of FinFETs, in practice is very difficult, for example, it is quite hard to control the thickness of the fin along the channel length (gate length) due to the limitations in the fabrication technology [47]. FinFETs overall are also vulnerable to different sources of variability, as discussed in Section 3.1 for DC variability and Section 3.2 for AC variability. Usually the channel of FinFET is undoped, but, in the case of low power applications, the fin channel is still doped to control the threshold voltage, hence making RDF an important aspect in FinFET modeling. Also, if we consider the cumulative effects of all process variations, e.g., fin variations, doping fluctuations and workfunction variations, precise behavior of the device is affected by the strong statistical spread. Depending on the type of performance parameter under study,

the variability in FinFETs can be characterized in two ways:

- DC variability: addresses the spread of DC currents, e.g., I_{on} and I_{off} e.t.c. (see section 3.1)
- AC variability: addresses AC parameters like Y matrix. (see section 3.2)

The statistical or systematic imperfections in the process of manufacturing, that consequence in the non-deterministic performance of transistors are known as Process Variations. The process variation is further classified as statistical or systematic variation.

If the dimensions of a device are very small and etching, oxidation, ion implantation, diffusion e.t.c., schemes are used for fabrication, the statistical variations are very hard to control because of the development process; for example, the quantity of dopants in the channel will be extremely high if channel length is large, but, even if few atoms are not positioned ideally, the error in totality would be small. On the contrary, if the aggregate numbers of dopants are very small as well as the channel is also very short, an unavoidable error would be produced by every single atom that diverges from the projected outcome. These are total random variations and there is not any better solution than to pinpoint them statistically or eliminate doping dependence in the device. Hereafter, we will discuss DC and AC variability in detail.

3.1 DC variability

Due to FinFETs distinct gate shape, which is used to control the conducting channel, it is very important to maintain the gate immunity to process variations. Now, if there is any variability in the gate or the conducting channel, it will directly affect the DC performance of the device. It needs special consideration and needs to be studied properly. In this section, we present how process variations, adversely affect the device performance. For example, etched sidewalls influence the current flow in the channel, so if these sidewalls are not etched properly, then the current flow through the device will not be consistent with the expected current [48]. This etching problem can also be the case where the etching results in the trapezoidal fin shape which is not ideal for commercial applications because it results in the shape of corner effects which again affects the device current [49]. This peculiar case of trapezoidal fin shape is discussed in section 3.1.3. Hereafter, we discuss the main process variations influencing DC performance.

3.1.1 Random Dopant Fluctuations

In 1975, Keyes et al. studied the effects of random fluctuation in the number of impurity atoms [50], as one of the issues for continued transistor scaling. Experiments confirmed his theory, for a wide range of fabricated devices. A type of variation that is caused by errors in the process of dopant implantation ensuing by the random quantity of dopant atoms in the channel is called RDF. A variation in a device's threshold voltage is resulted by the quantity of dopants in the transistor channel [51]. The frameworks built on MOS based devices gets more receptive to device fluctuations when supply voltages are steadfastly brought down to curtail power consumption and also control the system reliability. Fig. 3.1 shows an example of the decreased number of dopants in the channel region of MOSFET, resulting in random position and a spread in average concentrations.

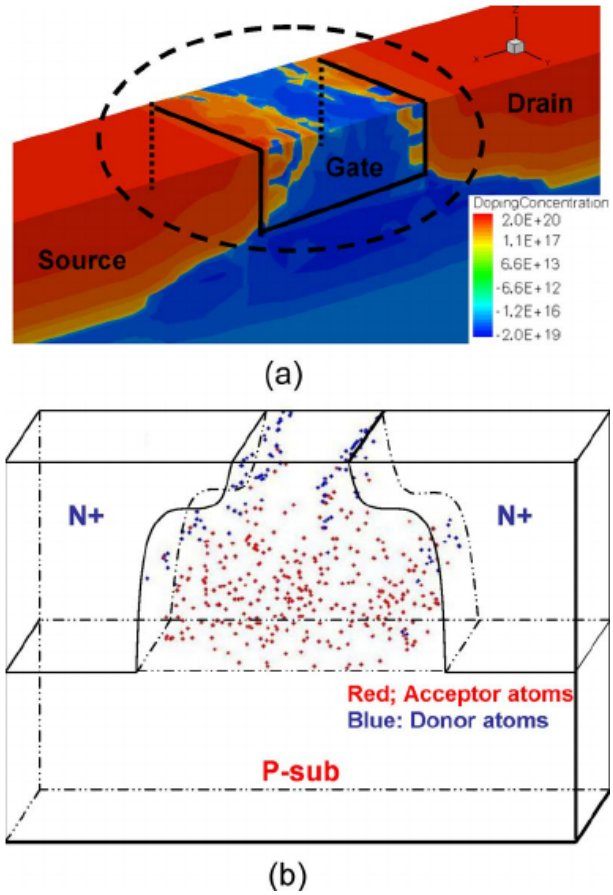

Figure 3.1: Example of atomistic doping profiles in Bulk MOSFET. (b) Isometric view of the RDF in Bulk MOSFET [52]

Fig 3.2 relates the technology node and average number of dopants. Fig 3.2

shows the decreasing the average number of dopant atoms in the channel as a function of the technology node. The major impact of random fluctuations and dopant arrangements in the channel, results in significant fluctuation on drive current and threshold voltage. Understanding and modeling RDF has been popular subject of research in recent past, since RDF is considered one of the main source of variability in FET devices.

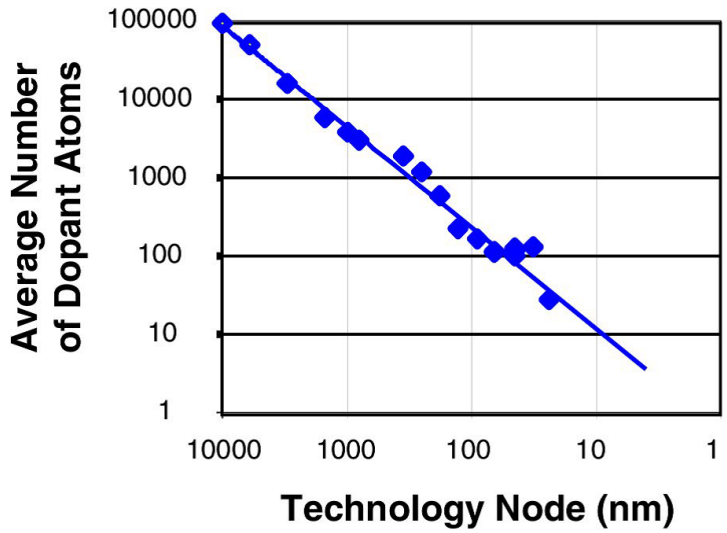

Figure 3.2: Number of Dopants vs Technology node [53]

The random dopant atom fluctuations are discussed in detail, e.g., in [50] and [54]. The standard deviation of threshold voltage σV_{th} are attempted to be estimated by analytical models, which are based on variation in the dopant numbers of the transistor's channel zone, also known to follow Poisson distribution. There are different analytical models for threshold voltage variations, e.g., Stolk's formulations are known to characterize RDF in MOS transistors [55].

$$\sigma V_{th} = \left(\frac{\sqrt[4]{4q^3 \epsilon_{si} \phi_B}}{2} \frac{EOT}{\epsilon_{ox}} \frac{\sqrt[4]{N_A}}{\sqrt{W_{eff} L_{eff}}} \right) \tag{3.1}$$

where $\phi_B = 2\ \mathrm{k_B T}\ \ln(N_A/n_i)$ (with k_B Boltzman's constant, T the absolute temperature, n_i the intrinsic carrier concentration, q the elementary charge, EOT is the equivalent oxide thickness, N_A is the channel doping, and ϵ_{Si} and ϵ_{ox} are the permittivity of silicon and oxide respectively. The effective channel length L_{eff} and width W_{eff} are used instead of the physical values in order to correct for offset in the active device area. Eq.3.1 also explains the inverse relation between σV_{th} and square root of the device active area. However, [56] shows that Eq. 3.1 doesn't completely incorporates the σV_{th}. The numerical simulation on full scale demonstrates that

only dopant number fluctuations are inadequate to elucidate the real amount of threshold voltage fluctuation. The unpredictability in dopant arrangements within the devices consisting of the similar quantity of dopants in depletion region further adds to variability and causes adverse effects on the behavior of the devices which force the technologist for the evolution in FinFET technology, which is expected to be more immune to RDF. To maintain electrostatics in the channel, i.e., immunity to SCE, the increase in the channel doping is required, which in turn, according to eq. 3.1, would bring to large variability unless EOT is reduced. Further, the area reduction due to scaling of the devices also causes the increase in V_{th} variability, again according to eq. 3.1.

Ref. [57] studied in particular, the impact of RDF on threshold variation. The analytical models discussed in [57] provides us with essential information about the threshold voltage variations, explaining the inverse relation of oxide capacitance to threshold voltage, and it's direct proportionality to the square root of channel doping. [57] also discussed the RDF effects on the NMOS and PMOS type of transistors. Table 3.1 [57] gives us the idea of threshold voltage dependence on RDF, it concludes that σV_{th} is heavily dependent on RDF, but there are many other factors influencing the overall V_{th}.

Table 3.1: Impact of RDF on threshold variation [57]

Type	Node	σV_{th} due to RDF
PMOS	45 nm	60%
NMOS	65 nm	65%

3.1.2 Line Edge Roughness

Line Edge Roughness (LER) is described as imperfection in the device structure caused by the fabrication step. LER can cause significant variations as device scaling persists in nanometer regimes[58]. LER effects are caused by fabrication limitations, as we are compelled to use light sources with wavelengths higher than the minimum feature size. In FinFET technologies, LER can be termed as FER-Fin Edge Roughness and GER- Gate Edge Roughness. For example, Ref. [59] studied the statistical variability in 14 nm FinFET with respect to different sources of variability. Fig. 3.3 shows the 14 nm FinFET structure with GER and FER.

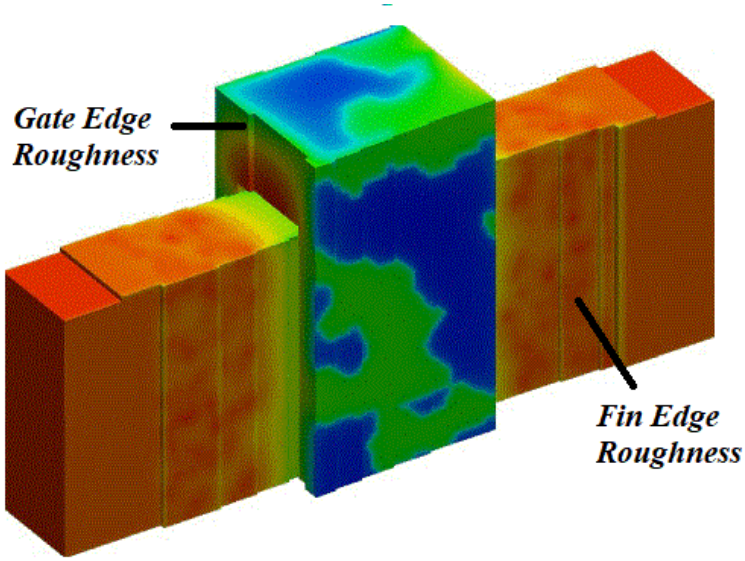

Figure 3.3: Example of LER with Fin and Gate edge roughness[59]

If we look at the Fig. 3.4, we can observe that GER produces skewed V_{th} distribution with a prolonged tail, specially with a 10 nm variant, in comparison to the FER, due to stronger SCE. However, for thin fin width, the FER can also produce a skewed distribution.

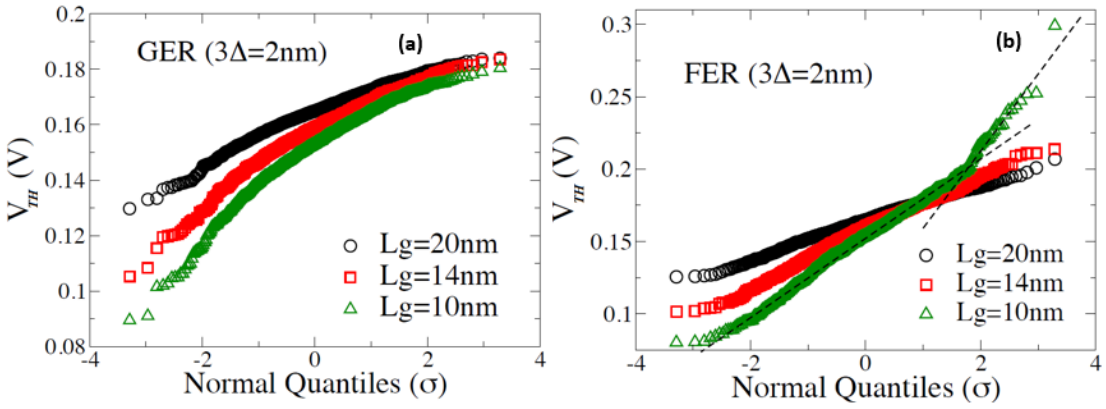

Figure 3.4: Threshold voltage distribution **(a)** GER effect on threshold voltage shows that for smaller FinFET have prolonged tail due to SCE. **(b)** FER effect on threshold voltage, it shows the deviation in 10 nm FinFET from the normal distribution [59]

As transistors are scaled down, the gate length is reduced to a level that a slight deviation from the nominal value can have a large effect on electrical performance.

The threshold voltage variation is dominated by variation generated by LER for the sub-50 nm SOI FinFET technology.

Surface smoothing is required to reduce LER , for example, thermal annealing [39, 40], sacrificial oxidation [60], and resist trimming [61] are equipped for wiping out the larger part of fast varying surface roughness, leaving for the most part lower magnitude of surface roughness. Also, it has been demonstrated in [62] that low-recurrence unevenness is the more critical fluctuation with regards to LER.

The fabrication limitations results in LER, thus, statistical analysis of the system prone to these variations is required. Commonly, harsh line edge designs are depicted by two parameters: the root-mean-square (rms) roughness σLER and the correlation length λ. As a rule the $3\sigma LER$ esteem is inferred when one alludes to LER in the literature [63]; while in [64] 1 sigma rms value is used. On the outside chance, if the σLER on the two edges of a line design are equivalent, at that point the LWR is identified with LER and it can be expressed as:

$$\sigma^2_{LWR} = 2\sigma^2_{LER}(1 - \rho_x) \tag{3.2}$$

here ρ_x is the cross-correlation coefficient between the two edge patterns. Standard resist patterning normally creates uncorrelated edges, i.e., $\rho_x = 0$, while spacer patterning produces associated edges, i.e., $\rho_x = 1$ (in a perfect world) which yields σLWR $= 0$. Defining these two points of confinement in the process technology enables us to cover the whole scope of LER-LWR cross-correlation, and licenses us to gauge the fluctuation for ρ_x by straightforward interpolation.

Ref. [64] suggests that FER is more important and more influential source of variability in comparison to GER, due to the fact that FinFETs V_{th} is more sensitive to fin variations than gate-length variations, causing larger FER variability than GER.

3.1.3 Fin width Variations

By expanding the volume of the channel, the thickness of fin is varied. At the point when the thickness of the film is sufficiently wide, depletion regions of the two gates stops interacting and the FinFET channel is transformed into two parallel transistors. With the continuous reduction in fin's thickness, there is a merger of depletion regions and we basically have a completely depleted channel. In the thin channel, a volume inversion occurs, which prompts increment in the quantity of charge carriers as energy bands in the channel travel in conformance with gate voltage. Hence the control of fin width is exceptionally important. In [65], authors discussed the effect of fin variations on the sensitivity of performance parameters such as V_{th}, on and off current. Fin variations can be categorized as:

- Uniform Fin thickness

- Non-uniform Fin thickness

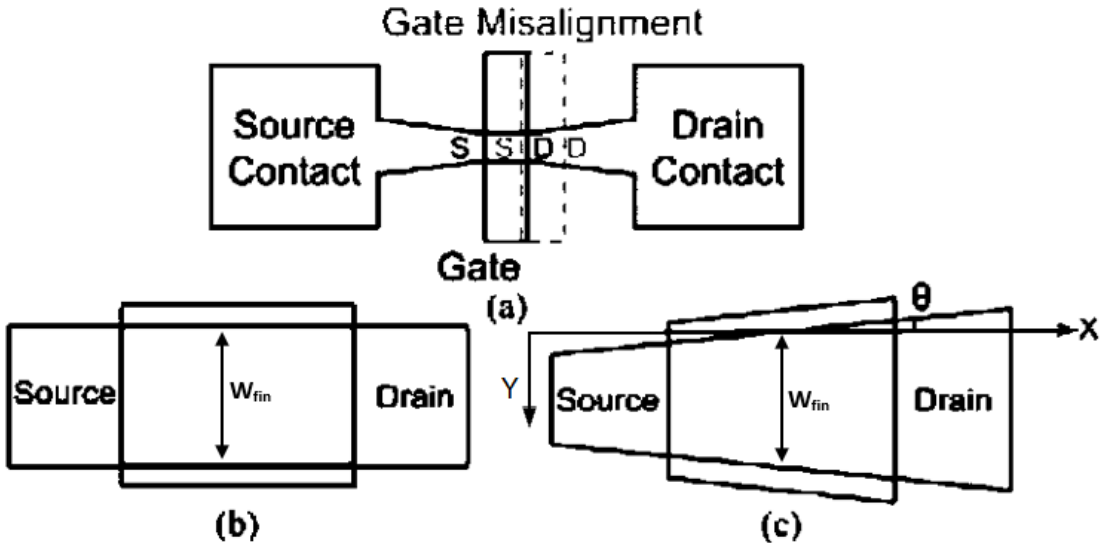

Figure 3.5: **(a)** FinFET top-view showing gate misalignment causing lateral fin-width variation. **(b)** DG FinFET ideal structure. **(c)** Structure with fin-width variation characterized by tapering angle (θ) to x-axis [66]

From Fig. 3.5 **(b)** and **(c)**, we can see the two different cases of fin variations. The fin variations shown in Fig. 3.5 **(b)** are the uniform fin variations and the one shown in Fig. 3.5 **(c)**, represents the non-uniform fin thickness variations.

Uniform Fin variations

In FinFETs, keeping up uniform film thickness (fin-width) is challenging. Nonetheless, fin-width is known as one of the vital parameters that decide the response of the device, where lesser the size of the film the better. Some past work [67] and [68] incorporates the analysis about the lateral thickness fluctuations due to the fabrication limitations. Since, the created fin-width geometry is diverse from the drawn geometry, one approach to show the real device is to estimate the fin-width utilizing the average thickness, i.e., 3.5 **(c)**, overlooking the way that the thickness fluctuates along the sidelong gate length. To explore the inaccuracy presented due to fabrication process, this examination depends on fluctuating the tapering angle θ along the horizontal way, yet keeping up the overall thickness. In [66], impacts of the non-consistency on performance parameters, for example, I_{on}, I_{off}, V_{th}, DIBL, and SS, are examined by matching with the nominal geometrical values of the structure. It is demonstrated that the thickness fluctuation influences subthreshold parameters significantly, with the results showing the adverse effect on the SCE.

Cheng-Li Lin et al. [69] also work on the effect of dimensions and on how, fin height (H_{fin}) and width (W_{fin}) influence the device's performance and reliability. In addition, the carrier mobility of the device is correlated with the carrier scattering in the channel of the Si-fin. Hence, the fin designing deformities influence the carrier mobility [70], [71]. Moreover, fin width impacts the inversion carriers in the fin. If the fin width size is small, then it enables the inversion carrier to stream in the middle of fin body instead of the surface edges of the fin [58, 72]. But the reduced fin size increases the parasitic source/drain resistance, which ultimately reduces the driving current. Reduced fin improves the high-frequency FinFET performance [73]. Hot-carrier injection (HCI) stress [74] and negative-bias temperature [75] instability reduces the FinFET reliability, when the fin width is small.

Lee et al. [76], on the contrary, discusses fin width dependency its impact on the DC performance of device. For 14 nm technology node, the nominal value of the fin width was kept at 12 nm and then reduced down to 8 nm, keeping height of fin at 100 nm: 18% reduction in the on current I_{on} was observed while off-current I_{off} decreases by 100 times, as depicted by the Fig.3.6. Along these lines, the I_{off} is very sensitive to the fin body width, which ought to be controlled precisely to keep up a with I_{off} distribution. Since in FinFETs the effective channel width is defined as twice the height plus the width of FinFET.

$$Effective\ channel\ width = 2xH_{fin} + W_{fin} \tag{3.3}$$

H_{fin} is the height of fin, when the W_{fin} is reduced, it also changes the effective channel width.

The explanation behind the reduction of I_{on} can for the most part be credited to the change in V_{th} and effective channel width with the change in W_{fin}. On the other hand, the lessening of I_{off} with reduction in W_{fin} can be clarified by the increment in SS with the fin width reduction. V_{th} values are lowered by 0.14 at I_D of 1 μA/um at the W_{fin} of 8 nm. Fig.3.6 b, shows change of the SS and DIBL with the W_{fin}. At the lessened fin width, the SS decreases from 106 to 77 mV/dec, while the DIBL decreases to 80 from 183 mV/V. In this way, W_{fin} likewise significantly ameliorates the SS and DIBL. The W_{fin} of around 9 nm gives a DIBL of 100 mV/V at the given body doping of $2 \times 10^{17}\ /cm^3$. When doping is increased to 2.5–3 $\times\ 10^{17}\ /cm^3$, the DIBL improves, and the W_{fin} required to give a DIBL of 100 mV/V will be around 10 nm.

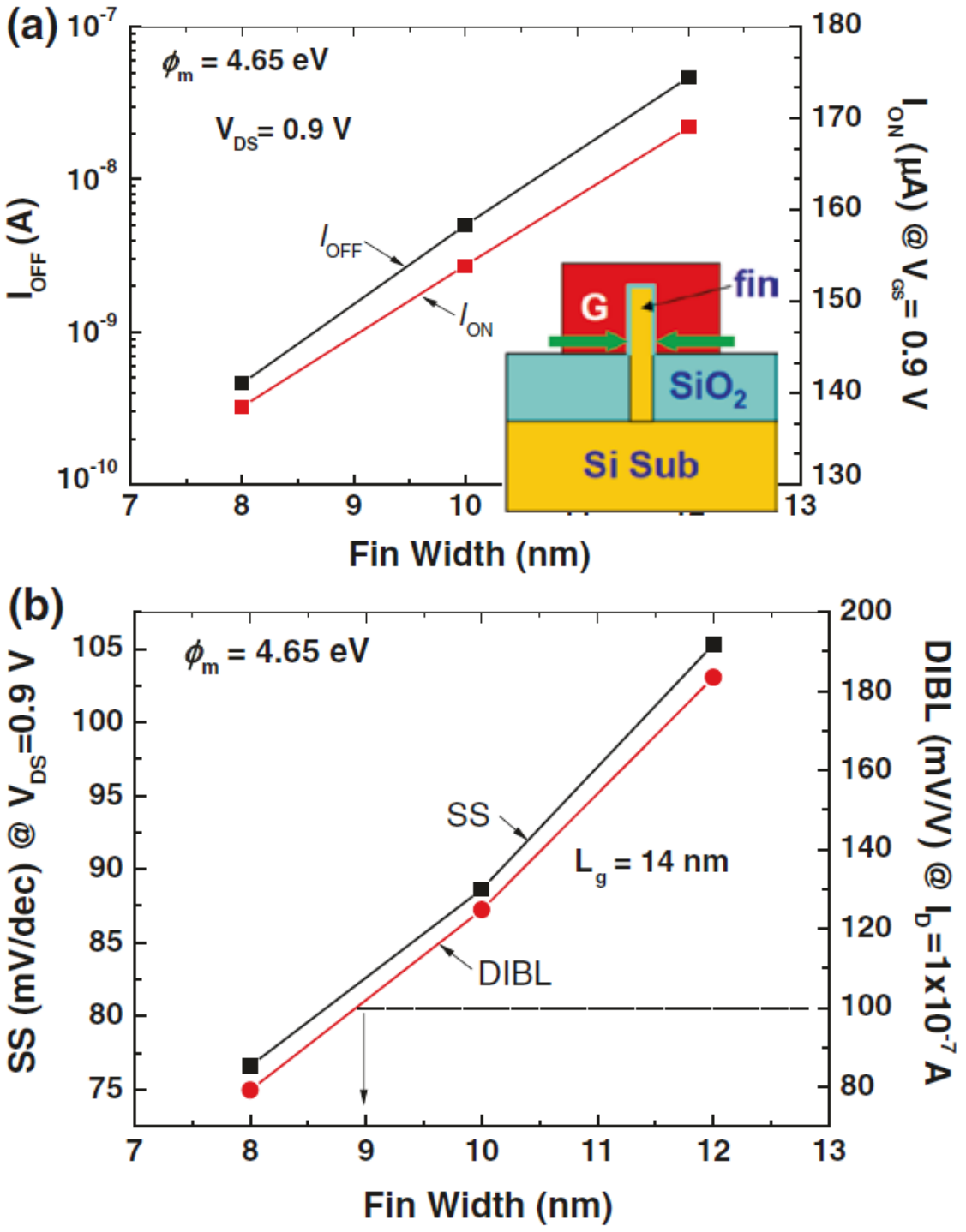

Figure 3.6: **(a)** Behavior of I_{on} and I_{off} with respect to fin width. **(b)** Behavior of SS and DIBL according to the fin width [77].

More simple structure, i.e., DG MOSFET was also studied in [48] showing an increment in threshold voltage with reduction in device body thickness. This outcome is due to various physical phenomena. As the silicon body gets more slender, the two gates show signs of improved control over the channel, eradicating short channel effects and threshold roll-off. This is in line with more established model as well. The change in threshold voltage with fin variation can be also due to the quantum confinement: as the body thickness falls below 10 nm, a quantum well is shaped between the two gates. Electrons in the quantum well possess more energy in comparison to the other electrons present in bulk material, which ultimately increases the inversion charge energy. If the thickness is further reduced, then the energy states in the smaller quantum well are further increased, which increases the threshold voltage.

Non-Uniform Fin variations

In previous section, we discussed the case of uniform variation in fin thickness. The fin variations can result in the trapezoidal shape and they also affect the threshold voltage, output conductance, transconductance, gate capacitance and unit-gain frequency. Here, in this section, we will discuss the peculiar case of fin variations, where one end of fin is larger than the other. The test case implemented to study the DC variability w.r.t. fin variation can be seen in 3.7. Researchers are working to contemplate the impacts of non-uniform thickness in the vertical course, i.e., y-axis as shown in Fig. 3.5 **(c)** [78, 79]. But there are not many investigations concerning the horizontal course of the device,refer Fig. 3.5; despite the fact that this sort of thickness fluctuation is present in manufacturing process because of horizontal misalignment of the gate.

The FinFET shown in Fig.3.7 is the device with a larger source-side fin width compared with the nominal, namely, the larger source side (LSS) structure is showing a FinFETs trapezoidal structure with W_{fin} along the channel. The models are designed for four different fin thickness variation structures to investigate the effect of W_{fin} variations from the device properties: smaller source side (SSS), larger source side (LSS), larger drain side (LDS), and smaller drain side (SDS).

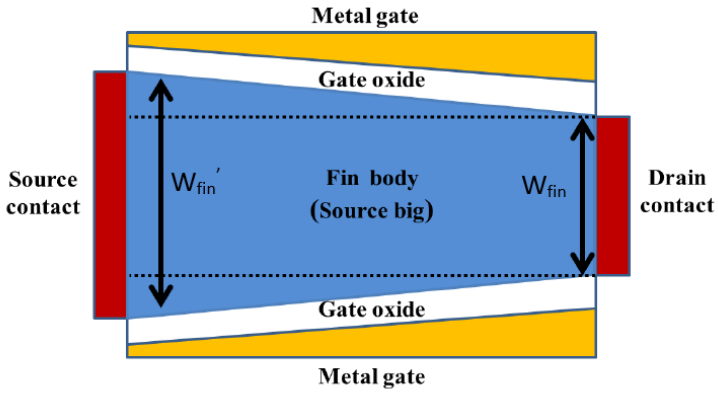

Figure 3.7: 2D view of Larger source side FinFETs [80]

Simulation of 32 nm FinFET was carried out on Sentaurus TCAD [81] and the Table 3.2 lists the nominal values of the simulated structure. The DC electrical characteristics (e.g., Id-Vg, Id-Vd) of the nominal FinFET are calibrated with BSIM FinFET models [82]. Further, the variations of 10-20% were applied to the nominal values on one side of either or drain or source to analyze the overall device performance , including the leakage and on current.

The normalized I_{on} and I_{off} values with 10% and 20% variations of the source- and drain-side thicknesses are arranged in Table 3.2. In this table, for the source-side W_{fin} of 9 nm (i.e., -10% with respect to the nominal, in the case of SSS), around 4% increment is observed in I_{on} while increment in the off current is twice of the nominal structure. Therefore, the structure with smaller source side, i.e., SSS has the advantage of improved operational speed; however, these results show the huge penalty in leakage power savings. For the larger source-side W_{fin}, I_{off} is reduced by 32%. As a result, the LSS fin body has the disadvantage of a slight reduction in the operation speed. For smaller drain side (SDS), I_{on} rises by 2% and I_{off} is two times greater than that of the nominal structure. For the increased silicon channel width near the drain terminal i.e. W_{fin} of 11 nm (LDS), there is no reduction in I_{on} and I_{off} decreases by 24%.

Table 3.3 summarizes that the FinFET of large- source or -drain (LSS or LDS) W_{fin} type achieves high leakage power savings while experiencing a slight reduction in the on current. In contrast, the FinFET of small- source or -drain (SSS or SDS) W_{fin} type achieves enhanced on-current consuming increased leakage power. Moreover, when W_{fin} variation increases, the variation in the currents increases. These analyses depicts that the effect of the source side is prominent then the drain side variation in fin width effects. In addition, it is quite interesting to note that I_{on} increases with a decrease in the drain-side thickness (SDS), while I_{off} decreases with an increase in the source-side thickness (LSS).

Table 3.2: Structural Parameters of the DG FinFET [80]

Symbol	Parameters	Values
T_{si}	Fin body thickness	10 nm
H_{fin}	Fin height	50 nm
L_g	Gate channel length	32 nm
T_{ox}	Oxide thickness	1 nm
V_{DD}	Supply voltage	0.9 V
N_{ch}	Channel doping	1×10^{19} cm^{-3}
$N_{S/D}$	Source and Drain doping of nFinFET	$2\times10^{24}cm^{-3}$
$N_{S/D}$	Source and Drain doping of pFinFET	$1\times10^{23}cm^{-3}$

Table 3.3: Normalized on current and off current w.r.t. fin variations

	ΔW_{fin}	Normalized I_{on}				Normalized I_{off}			
		SSS	LSS	SDS	LDS	SSS	LSS	SDS	LDS
nFinFET	Nominal	1				1			
	10%	1.04	1.00	1.02	1.00	1.91	0.68	2.00	0.76
	20%	1.16	0.99	1.07	1	3.42	0.53	2.95	0.65

As summarized in Table 3.3, when the LSS source side W_{fin} is 12 nm, 1% fall in I_{on} is observed while I_{off} is reduced by half of the nominal current. It can be concluded that whichever side (source or drain) is reduced, it results in the rise in both on and off current. While, both currents are reduced from its nominal values when the thickness of either side is increasing. From this analysis, we can expect that the structure of the FinFET with a large fin on the source side and a small fin

on the drain side will achieve reduced I_{off} and increased I_{on}. However, practically, I_{off} is increasingly reduced while I_{on} does not increase, owing to the increasingly larger depletion area and V_{th}.

3.1.4 Workfunction variations

The workfunction variations(WFV) can be considered as one of the significant source of variability in the FinFET device, and more in general in metal gate technology. It is caused by the granularity and the crystal size of the metal gate material [83]. The material used for the gate and its granularity brings another type of variability in the FinFETs. The multiple grains of crystals possessing different grain orientations are combined to form polysilicon or metal gate electrodes [84]. Each grain can have a different work function, which causes a variation in the V_{th}. To alleviate this granularity, and hence variability, researchers have proposed different methods, e.g., using amorphous metal as the gate material[84]. Variability in work function can also be reduced by having smaller grain size.

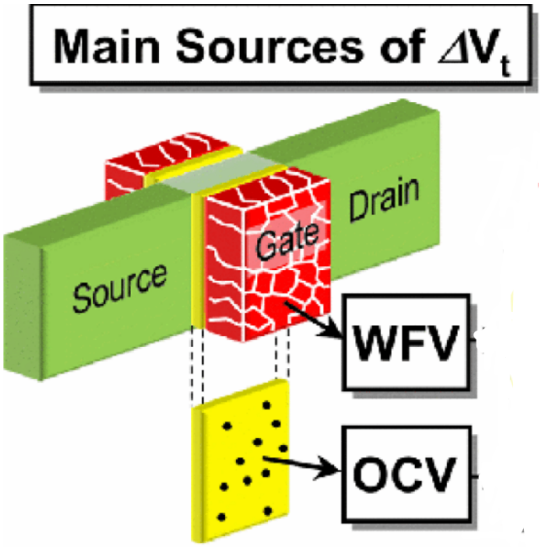

Figure 3.8: Individual grains producing WKV[84]

Ref. [85] also studied the DC behavior of the DG MOSFET and its sensitivity to work function variations. This is an important research field, since different applications require different threshold voltages. Hence, we can tune the threshold voltage to achieve desired device response by using different metals as per our requirements for the gate terminal. Unfortunately, due to the WFV, we are unable to achieve precise values of threshold voltage. In [85] workfunction value was varied from 4.29 to 5.2 eV to examine the V_{th} variations. It can be depicted from the figure

that the workfunction value and V_{th} has linear relation i.e., V_{th} is increasing with increment in workfunction values. These results were obtained with the device parameters set at: L_g = 20 nm, W_{fin} = 12.5 nm, EOT = 1.2 nm and V_{dd} = 0.86 V.

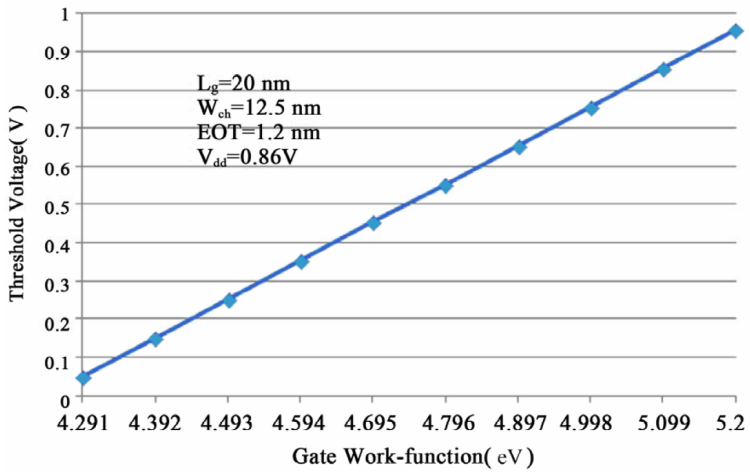

Figure 3.9: Threshold voltage versus gate work-function of DG FinFET [85]

Other DC parameters such as I_{on} and I_{off} have instead, inverse relation with the workfunction variations as shown in Fig. 3.10 and 3.11. This is due to the fact that, as at low values of workfucntion, the threshold voltage is minimal and the channel is formed at the very low gate voltages, ultimately increasing the drain current. Also at lower values of workfunction, leakage current is higher, which is not acceptable for low power applications.

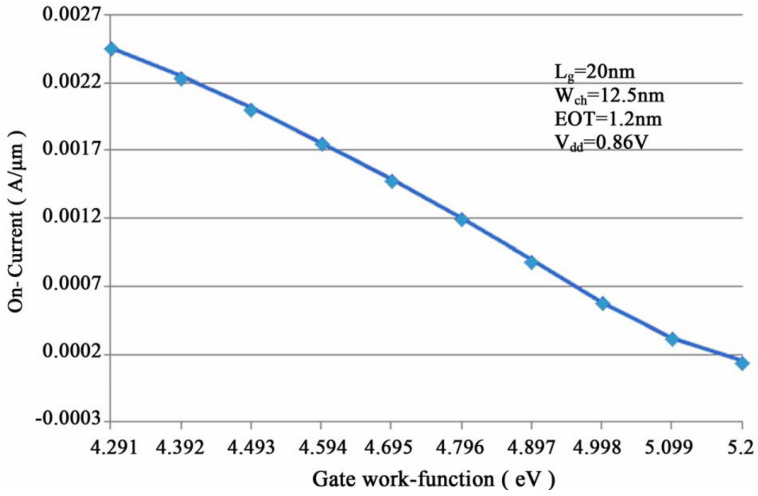

Figure 3.10: On-current versus gate work-function of DG FinFET[85]

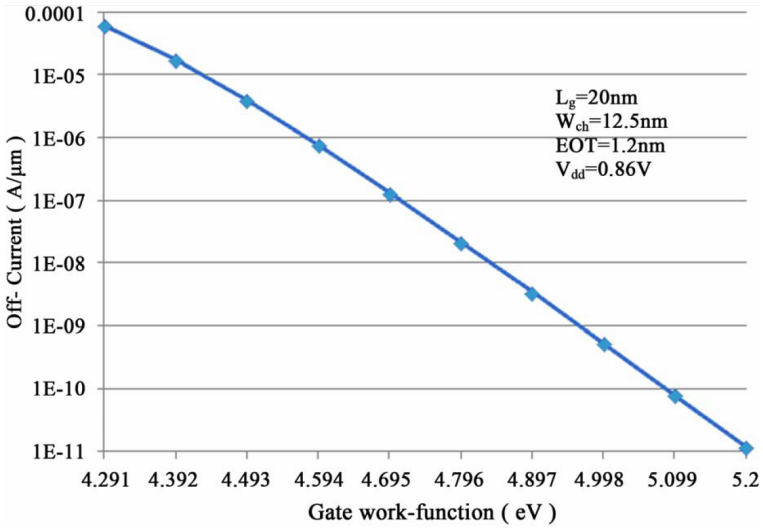

Figure 3.11: Off-current versus gate work-function of DG FinFET[85]

3.1.5 Oxide Variations

The applied gate voltage influences the energy bands in channel which, are therefore, directly affected by thickness of the oxide. In a FET, the oxide operates as an insulating film. Above threshold voltage, the oxide thickness essentially determines the gate capacitance. As gate voltage is varied, the energy bands in the silicon moves along with the energy band in the metal, tied across the oxide. An extremely high electric field, however, can prompt leakage in thin oxide and can cause insulator to collapse.

The gate oxide can be precisely deposited i.e., with the accuracy of 1-2 inter atomic layers, with the method known as atomic layer deposition. On the contrary, threshold voltage variations are inflicted in the system, when traditional deposition techniques for oxide, i.e., thickness of up to 10's inter atomic layers, are used. In below 30 nm technology where thickness in oxide is about 1-3 nm i.e. 5–15 inter atomic layers, t_{ox} variations can add to uncertainty of threshold voltage significantly. In MOSFETs, this uncertainty becomes of the same order of magnitude to RDF effects [86].

Ref. [87] studies the effect of t_{ox} on FinFET devices, the nominal value of gate oxide was kept at 1 nm, while 20% variations variations were applied. Since the monolayer for depositing the oxide on the silicon surface for fabricating SiO_2 dielectric is around 2 Å, 20% percent variations seem the minimum logical value for analysis of oxide variations on FinFETs. In [87], they observed the increase in on-current with decreasing oxide thickness. The threshold voltage, in fact, decreases with increase in oxide thickness and I_{off} increases with decreasing t_{ox}. But, for smaller t_{ox} the accumulation of charges across the FinFET corners will increase,

thereby, the threshold voltage increases. It is also apparent from Fig.3.13, that as t_{ox} contracts, V_{th} is rising because of the leakage charges collecting at silicon body and oxide interface. The threshold voltage is increasing with lower values of t_{ox} because the charges are accumulated over the edges. As expected, DIBL is shown to reduce with reduction in oxide thickness. Furthermore, as t_{ox} decreases, sub threshold swing decreases. But electric field across the t_{ox} layer is high, as a result tunneling of charges from gate to channel will increase, which may lead to failure of device. Even though the results for SS are good for lower t_{ox}, scaling is not advisable below 1.5 nm. Fig.3.12 shows I_{on} and I_{on}/I_{off} variation with respect to gate oxide thickness variation. I_{on} increases as gate oxide decreases, due to large electric field in the channel. I_{on}/I_{off} shows good gate controllability only at higher t_{ox}, while at lower t_{ox}, leakage current increases.

In [88], a FinFET is considered with W_{fin} and H_{fin} of 3 nm and 7 nm separately. The oxide thickness is changed from 1 nm to 3 nm. Gate oxide and I_{on} has inverse relation as depicted in the Fig. 3.12.

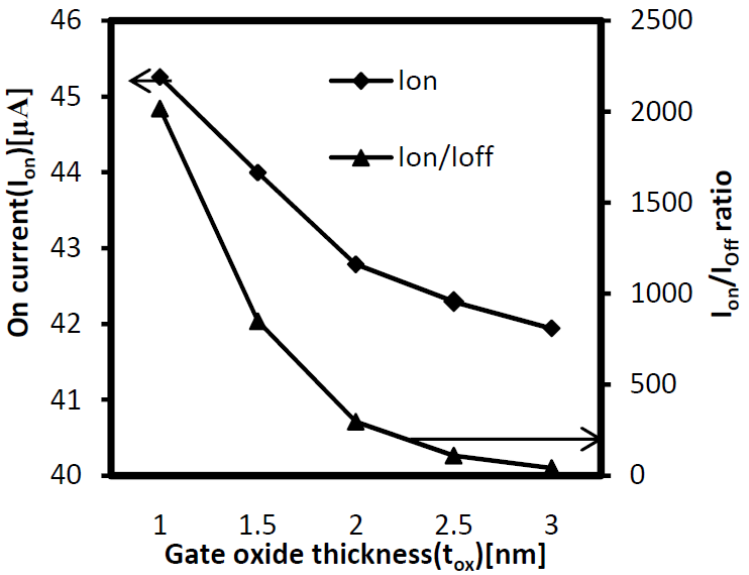

Figure 3.12: I_{on} and I_{on}/I_{off} vs t_{ox} [88]

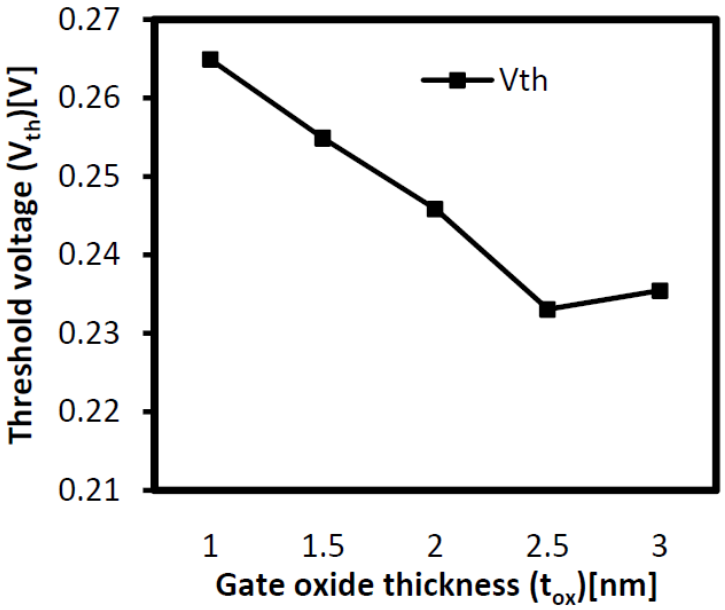

Figure 3.13: Threshold voltage V_{th} response to Oxide variations t_{ox} [88]

Ref. [48] also discusses the effect of t_{ox} on the threshold voltage and DIBL. The dimensions, they used for their analysis are: L_g= 20 nm, V_{dd}=0.8 V, t_{ox}=1 nm, N_A at 10^{15} cm^3 and S/D doping at $2 \times 10^{20}/cm^3$. They used ideal metal for the gate contact for their work. As the gate dielectric gets thinner, the gate voltage controls the channel more effectively and DIBL reduces. As a result, the threshold voltage increases with decreasing oxide thickness. [48] establishes that around 5 mV fluctuation can be observed for every 1 Å of oxide thickness variation for both nMOS and pMOS devices.

3.1.6 Temperature Variations

In mass CMOS technology, the heat generated is spread via silicon substrate and wires. In the SOI technology, instead the heat is drained, primarily, along the wires due to the poor thermal conductivity of buried oxides causing temperature to rise rapidly in the channel. The spatial temperature variation is also determined by actual application on the system. Selective sections of an IC, can be consistently utilized as a part of few workloads to keep temperature under control. In multi-core processors, for example, few of cores are kept idle, and cool down for a certain amount of time. This requires reliance upon the system's capacity to progressively deal with the workload, while, periodically rolling out jobs to dissimilar cores or moving operations from a core to another one. The variation of temperature firmly impacts static energy utilization. The issue of leakages and dynamic energy consumption have become important constituent with the rising innovation of high

density of devices on die. In the chip design, the impact of temperature should, therefore, be considered carefully.

In [89] discussed, for example, the importance of temperature variations of the device on overall system. In their work they studied the impact of process variations on temperature and leakage power. They performed about 1000 Monte Carlo simulations for each activity conditions and concluded the inter-dependency of leakage current and temperature. Due to the dependency of temperature on the leakage power, high activity circuits are more prone to temperature variations. Their work shows that the thermal runaway can occur in 15% more chips at the nominal activity level, if the variability parameters elevating the temperature are not optimized properly.

Ref. [90] focuses on drain current dependence in response to temperature variations and compares the results of Bulk MOSFETs and FinFETs. Varying the temperature from -40 C to 125 C. As shown, T variation in bulk CMOS affects both on-current (I_{on}) and the leakage power consumption (I_{off}), while in FinFET, it more significantly changes I_{off}. However, off current variation in FinFET is more severe. Another feature that is affected by temperature variation is the threshold voltage. Increasing the temperature from -40 C to 125 C decreases the threshold voltage by 10% and 16% for bulk CMOS and FinFET respectively. Hence, the threshold voltage dependency to the temperature is higher in FinFETs [90].

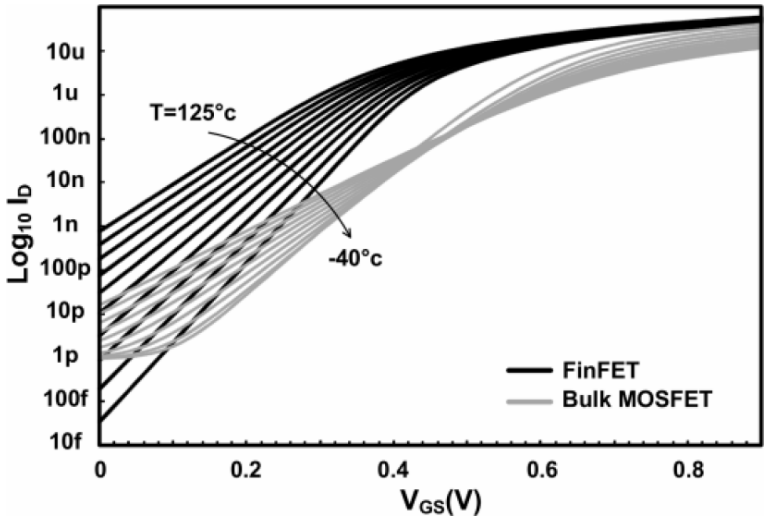

Figure 3.14: Drain current I_{on} versus gate source voltage for different temperatures for FinFET and bulk MOSFET [90].

3.1.7 Source/Drain variations

In FinFETs, the volume of source and drain is usually increased adequately through Source and Drain extension (SDE) due to improved transconductance g_m,

reduction in drain conductance g_{ds} and reduction in parasitic capacitances, due to optimal gate underlap regions. Source/drain extension in result turns to higher current and reduced resistance. Further, the parasitics related to the source/drain extensions in FinFET are further discussed in section 2.4.4. The source/drain thin fin extension regions are highly resistive, so, it is essential to minimize their length. In the context of minimizing the parasitic resistances of this region, [91] uses selective Germanium growth technique to introduce the raised source/drain regions. Lot of work has been already presented on reduction of source/drain resistances, e.g., dopant segregation, co-implantation, and selective epitaxy growth on the source/drain extensions. Another important parameter, that must be considered for source/drain variations is the doping of the source/drain extensions. Fig 3.15, e.g., demonstrates the effects of the random dopant placements in source/drain extensions. Every tiny dot represents one dopant atom and their effects are studied in [58] to highlight the importance of source/drain variations.

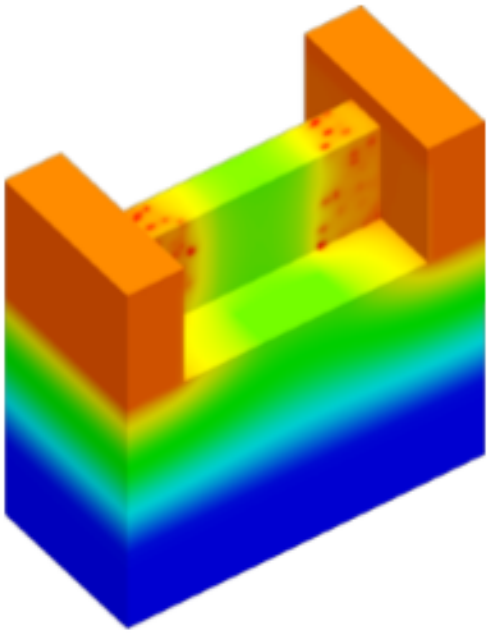

Figure 3.15: FinFET Random Dopants in SD extensions [58]

3.2 AC variability in FinFETs

As seen from the previous sections, lot of work has been devoted to the DC variability of FinFETs in terms of V_{th}, *SS*, I_{on} and I_{off}. On the other hand, the AC variability requires higher computational resources, especially in the case of 3D device simulations and is, therefore, less investigated, mostly in terms of sensitivity and dependency on technological parameters. Ref. [92] (see Fig. 3.16) studied

FinFETs with two structures, one with smaller fin width (3 nm) and the other with larger(10 nm), showing the effect of fin variations on the cutoff frequency, discussed later in this section.

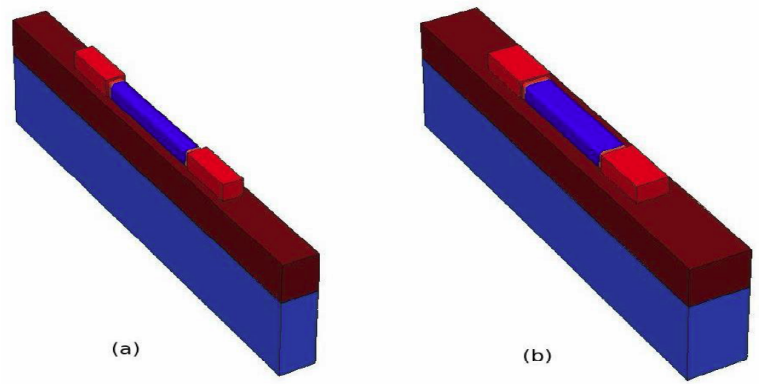

Figure 3.16: Simulated fin structure FinFET for (a) smaller fin width (b) larger fin width [92]

In [92], capacitances are taken as primary factor for AC analysis. C_{gg} is described as:

$$C_{gg} = \frac{C_{ox}C_{Si}}{C_{ox} + C_{Si}} + C_{ov} + C_{fringing} \tag{3.4}$$

where,

Table 3.4: Capacitances naming convention

Capacitance	**Symbol**
Gate Capacitances	C_{gg}
Oxide Capacitance	C_{ox}
Overlap Capacitance	C_{ov}
Silicon body Capacitance	C_{Si}
Fringing Capacitance	$C_{fringing}$

The overlap capacitance is given by:

$$C_{ov} = n(2W_{fin}.c_{ov}(T_{mask}) + 4H_{fin}.cov(T_{ox})) \tag{3.5}$$

The reason for overlap capacitance is the overlapping length (region of the source/drain extension under the gate electrode) which makes the doping process in source/drain extension area important as smaller overlapping length is needed. Also here T_{mask} refers to hard mask thickness.

$C_{fringing}$ in turn taken from [93]:

$$C_{fringing} = \frac{WK\epsilon_{di}}{\pi} ln \frac{\pi W}{\sqrt{L_{un}^2 + T_{ox}^2}} e^{|\frac{L_{un}-T_{ox}}{L_{un}+T_{ox}}|} \tag{3.6}$$

where K is the relative dielectric constant, dielectric permittivity is ϵ_{di}. When L_{un} (gate underap region) increases, current degrades and thereby g_m monotonically decreases. The combined behavior of g_m and C_{gg} is responsible for the f_t decrease as also shown in Fig. 3.20. The relation between g_m and C_{gg} can also be deduced from Eq. 3.7.

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{3.7}$$

For AC analysis, parasitics become the most significant source of concern with respect to DC. The importance of parasitic components in multiFin FinFETs are discussed, for example, in [94]. The gate resistance (introduced in Section 2.4.4), is of paramount important in FinFETs and is directly related to the device geometry. Hence, is prone to variability. In [95], the parasitic fringing capacitance is modeled for the multifin structure. The parasitic resistive or capacitive parts end up similar in extent to or even significantly bigger, if the fin width is reduced. Additionally, regular capacitance and resistance models can't be connected straight-forwardly to non-planar MOSFETs because of the 3-D device structure. Physical models need to be build up for the 3D design of FinFET. In the study of device parasitics, three important parameters to be taken into consideration are gate resistance (R_g), S/D series resistances, and gate parasitic capacitances. Gate parasitics (Rg and gate parasitic capacitances) are imperative factors in deciding gate RC delay and RF figure of merit f_{max}.

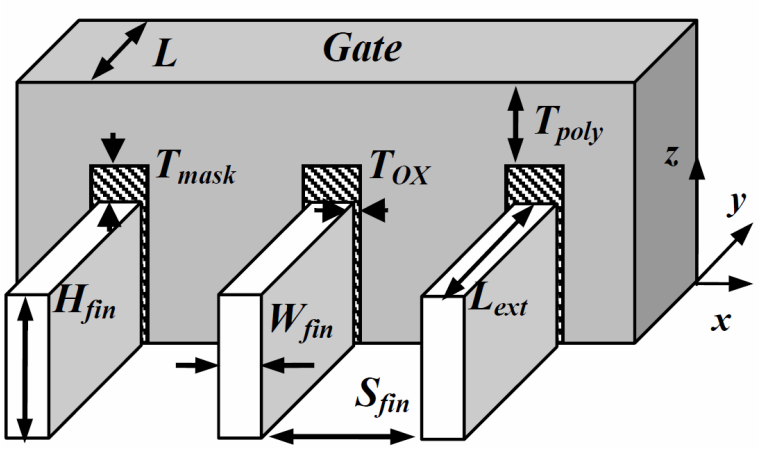

Figure 3.17: Three-fin FinFET structure [95]

Fringing capacitances are further analyzed in [95], separating various contributions, for AC characterization of FinFETs, as can be seen in Fig. 3.17.

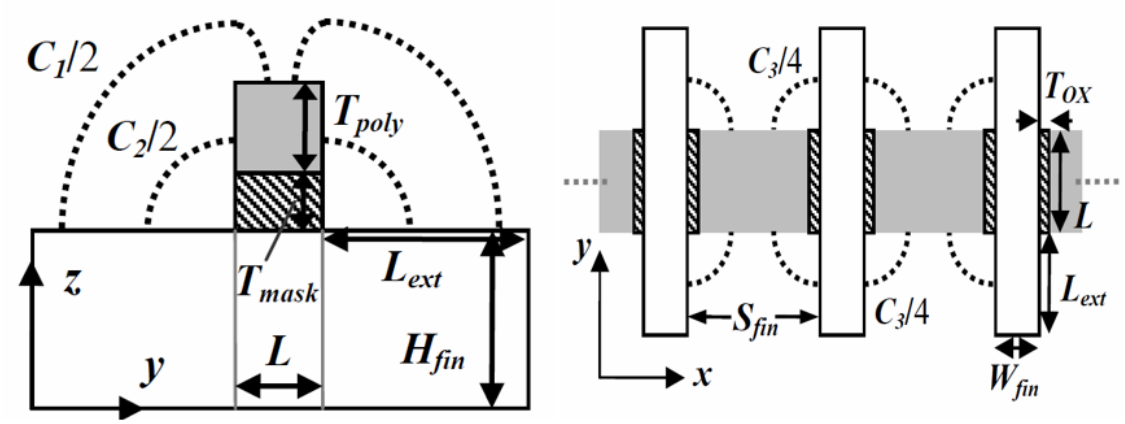

Figure 3.18: Cross-section of single fin(y-z plane) and multifin(x-y)plane[95]

The lines emitting from the top of polysilicon gate surface to the top S/D extension area (xy plane) are linked with C1. The capacitances due to the electric field flux from gate side walls are regarded as C2. C3 is caused by the coupling between one surface (y-z plane) of the fins and one surface (z-x plane) of polysilicon gates. By analyzing the device geometries shown in Fig. 3.18, C1, C2 and C3 can be expressed as:

$$C_1 = 2n\frac{(W_{fin} + S_{fin})\epsilon_{ox}}{\pi} ln\left(1 + \frac{L}{T_{poly} + T_{mask}}\right) \tag{3.8}$$

$$\begin{aligned} C_2 = \frac{2W_{C2}\epsilon_{ox}}{\pi} ln\left(\frac{T_{mask} + \eta T_{poly} + \sqrt{(\eta_1 T_{poly})^2 + 2T_{mask}\eta_1 T_{poly}}}{T_{mask}}\right) \\ + \frac{\eta_2 e^{-1} W_{C2}\epsilon_{ox}}{\pi} ln\left(\frac{\pi W_{C2}}{T_{mask}}\right) \end{aligned} \tag{3.9}$$

$$\begin{aligned} C_3 = \frac{2W_{C3}\epsilon_{ox}}{\pi} ln\left(\frac{T_{ox} + \eta_3 S_{fin}/2 + \sqrt{(\eta_3 S_{fin}/2)^2 + T_{ox}\eta_3 S_{fin}}}{T_{ox}}\right) \\ + \frac{\eta_4 e^{-1} W_{C3}\epsilon_{ox}}{\pi} ln\left(\frac{\pi W_{C3}}{T_{ox}}\right) \end{aligned} \tag{3.10}$$

In 3.9 and 3.10, W_{C2} and W_{C3} are equal to nW_{fin} and $2nH_{fin}$, respectively. The four geometry independent parameters, η_2, τ_1, η_4, τ_2 are all constant to account

for different dielectric materials (such as nitride, oxide or high-k). The values for these constants are $\eta_2 = 7.9$, $\tau_1 = 15$, $\eta_2 = 5$ and $\tau_1 = 30$ [96].

When channel doping is fluctuating then it also effects the cutoff frequency f_t through the transconductance. From the plot of f_t we see the cutoff frequency as weakly sensitive to doping variations till $10^{17}/cm^3$ [48]. It can be concluded when the channel doping values are lower, f_t is insensitive to the fluctuations. At high doping levels, f_t degrades due to g_m degradation[97].

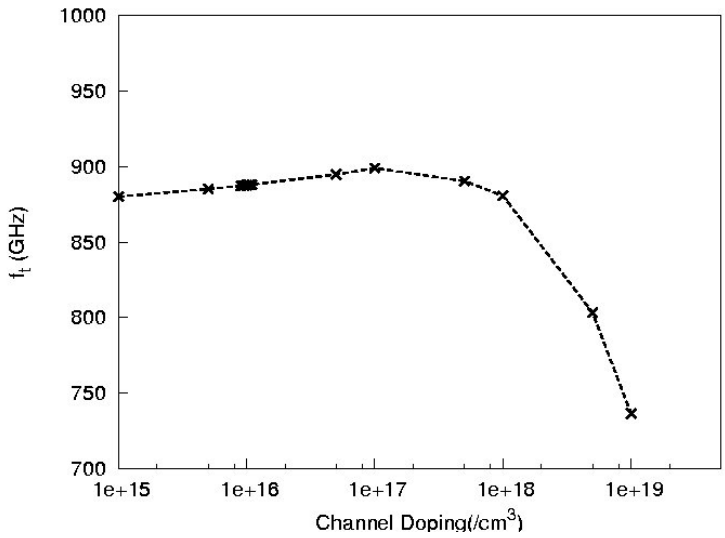

Figure 3.19: Cuttoff Frequency Variation f_t w.r.t. Channel Doping[97]

B. Lakshmi and R. Srinivasan [97] studied the effect of fin width variations to the cutoff frequency f_t. When W_{fin} is changed, we may either confront volume inversion or may not, contingent on the channel doping levels. At the point when the channel doping is $10^{16}/cm^3$ volume inversion isn't seen [98]. In this manner, the expansion in W_{fin} increases the current and thus increases g_m and f_t, this is due to the fact that mobility increases with increase in fin width. Figure 3.20 demonstrates this sort of conduct amongst f_t and W_{fin}. For the increased channel doping at around $1.5x10^{18}/cm^3$, volume inversion impact is seen making first f_t reduce and then increase with increasing W_{fin}. This is portrayed in fig. 3.21

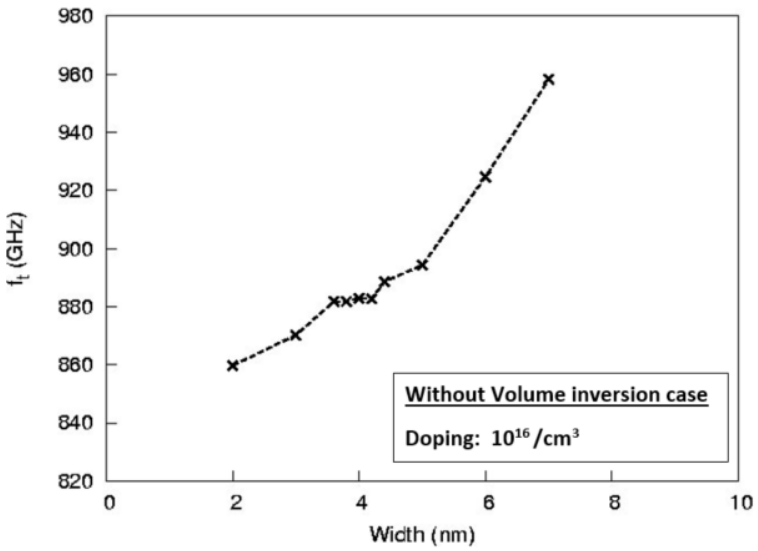

Figure 3.20: f_t vs fin variations without volume inversion in FinFETs [92]

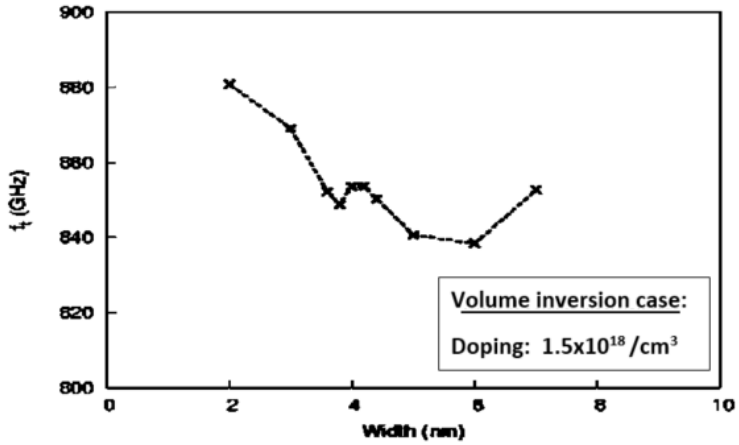

Figure 3.21: f_t vs fin variations with volume inversion in FinFETs [92]

Ref. [97] also discussed the cutoff frequency f_t with respect to the t_{ox} variation. Initially, the cutoff frequency increases almost linearly. Transconductance and gate capacitances control the cutoff frequency together.

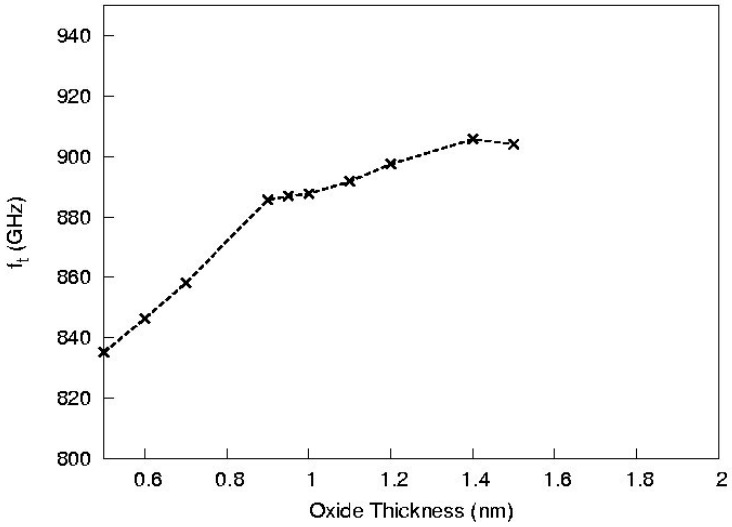

Figure 3.22: f_t vs oxide variations in FinFETs [92]

Workfunction variations are less influential on high frequency characteristics [16]. Therefore, f_t is expected to be, more or less, immune to gate electrode work function. Fig.3.23 shows f_t versus gate work function plot, and it can be noticed that f_t exhibits a flat behavior with respect to the work function.

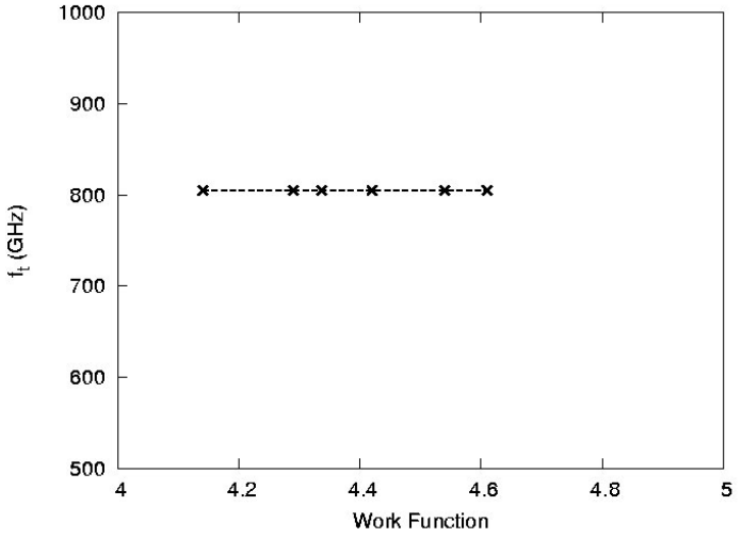

Figure 3.23: f_t vs workfunction variations in FinFETs [92]

In FinFETs, source/drain doping variations are lot more influential than channel doping. This is due to the fact, that increased source/drain doping results in reduced parasitic resistances, thus, increasing both the current and g_m, and resulting in increase in f_t.

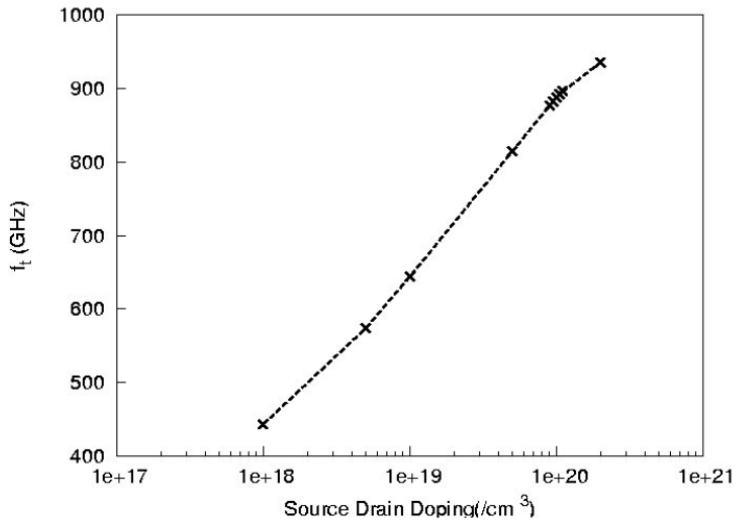

Figure 3.24: f_t vs Source Drain doping variations in FinFETs [92]

f_t sensitivity in response to different variations, was observed in this section. It is observed that W_{fin} ,t_{ox} and source/drain doping variations are very sensitive parameters, whereas, channel doping and workfunction variations are less sensitive parameters.

3.3 Summary

This chapter is dedicated to the variability and sensitivity analysis of FinFET devices. In this chapter, we have addressed possible process variations and their effects. In particular:

1. **RDF:** RDF is major source of variability in MOSFETs, but in FinFET, due to undoped channel, its effects are quite limited.

2. **LER:** Of the two types of LER,i.e., GER and FER. FER is more dominant, as it affect the FinFETs V_{th}.

3. **Fin width:** Decreasing the fin width, results in the decrease in on and off current. This is due to the change in threshold voltage with fin variations.

4. **Work Function variations:** Increase in the work function variations, results in the decrease in on current. This is again due to the increase in threshold voltage.

5. **Oxide thickness variations:** Reduction in the gate oxide, results in increase in threshold voltage.

6. **Source/Drain variations:** There can be two variation in the S/D region, one is the doping variation and the other is geometrical variations in the SDE.

The performance of FinFET is studied under two domains: DC variability and AC variability. Significant work has already been done on the DC variability of FinFET, while work on AC variability is still limited. This may be due to complexity of AC variability computation, as it requires large amount of computation resources and time.

For DC variability analysis, significant drain current degradation with the decrease in fin width. The threshold voltage is also affected by the process parameters, like, decrease in gate workfunction will decrease threshold voltage, hence, increasing the leakage current and power consumption of the device.

For AC variability analysis, we reviewed different capacitances and their effects. We also presented the cutoff frequency response to different variability sources. For AC variability, fin variations and source/drain doping were found to be dominant source of variations. Overall, we can see that fin variation is an important variation source in FinFETs.

In the coming chapters, we will focus on the modeling of the variability and sensitivity of FinFET device. The process variation, which affect the device performance need to be addressed properly and we address in particular the problem of AC variations that affect the AC performance of the device through parasitic resistances and capacitances, e.g., the increased parasitic resistances can affect the transconductance of the device.

Chapter 4

Modeling of Device Variability

In the previous chapter, we discussed the importance and impact of the process parameters on the device performance. The modeling of these variations in an adequate manner is also very important to understand all the aspects of device variability. For example, if we are modeling the RDF in FETs, models provide us with the essential information about electrical parameter fluctuations. The downscaling of device dimensions, the necessity of having 3D accurate solvers for the coupled transport/Poisson equation and atomistic-based simulators have grown significantly. Technological growth and continuos development in the CAD tools for the semiconductor device design based on the physical models has enabled the TCAD simulators to perform device simulations accurately with high speed and reliability using advance computer architecture, improved computational power and high memory capabilities and development of fast numerical algorithms including conceptually new simulation tools [99]. But, now very less effort has been put on the AC sensitivity analysis.

For example, the key tools for TCAD variability analysis proposed so far, stems from the idea of atomistic like simulations. The drift-diffusion based "atomistic" simulations provide significantly accurate and timely statistical results for nanoscale 3D devices accounting for variability, including random dopant distribution. This extends the applicability of the drift-diffusion transport approach to nanometer scale, and statistically varying structures, proving it again to be amazingly efficient, even outside of its formal region of validity [99]. If we look into the example of RDF, the first and foremost point for RDF analysis is to locate the position of the discrete random dopant in the device. This location of dopant is important because it has an increasing effect on the device behavior at the nanometer scale. In the case of LER modeling, it is important to define the statistical description of the gate interface and edges. Also, variations in process parameters are 3D in nature, therefore, they require full scale 3D simulations for the variability analysis. Being statistical in nature, another important aspect for modeling these variations

is that they require a large number of simulations of microscopically different devices. The idea is to simulate a statistically large enough set of device samples, with given statistical distribution, which provide us accurate results for the parameters characterizing the statistical distribution. This approach is exceedingly demanding from the computational standpoint. In [100], for RDF analysis, 5% accuracy in standard deviations was achieved for 200 MOSFET device samples but it required a huge amount of computational time. So an important requirement for simulation technique for process variation is such that it should be fast and efficient enough to handle a large number of devices. Furthermore, sensitivity or variability of AC parameters require even more simulation time and memory. Hence, the need for efficient tools is even increased.

This chapter is particularly dedicated to present a novel numerically efficient modeling of the device variability, understanding the device sensitivity arising from the variation in process variables.

First we will discuss the GF approach to variability modeling within conventional drift-diffusion model, including sensitivity of RDF and geometric variations. Then, the GFs approach to AC sensitivity modeling will be discussed in detail, since it represents the key methodology used throughout the present work.

4.1 Modeling Background of FET devices

The device modeling is of paramount interest for researchers around the world and many simulators have been established to efficiently model the device sensitivities. Turning to a statistical description of variations, in [101] and [102], the impact of RDF on the bulk MOSFETs was analyzed using the statistical fluctuation of the dopants. The approach used in [101] and [102] was also used for the simulations of the 3D structure in [103]. AdHoc "atomistic" simulation techniques were established in [104]. It is worth noting that, in this work, only 24 samples of the device were simulated due to the limited computational resources. Similar works were also carried out for 3D structures using atomistic approach, but with very limited number of randomizations in [105] and [100], to analyze variation in threshold voltage due to variations. In order to simulate a large set of device samples, computationally efficient simulators are required. The most efficient simulation technique is the GFs technique, which will be discussed in the next section.

4.2 Green's Function to Variability Modeling

In this thesis, we will be exploiting the GF method described in [106] and [107] to the impact of process variations and device sensitivity to possible technological parametric variations. Ref. [106] is focused on the noise based analysis of the bipolar devices through a physics-based device model by exploiting GFs approach.

GF is into the limelight for the noise analysis of electronic devices since 1966[108]. Recently used for sensitivity and variability analyses, GF based simulations [109] are broadly used particularly for ultra-scaled devices [9], since the simulation time of the system is reduced to a great extent especially when dealing with statistical variations. The GF based simulations were initially limited to DC variability of systems but recently have been extended for AC analysis from the group of Politecnico di Torino [110]. The Impedance Field Method (IFM), employed by commercial applications (Synopsis) to simulate the device fluctuations, is just an old-fashioned name for the same approach on the GF. It permits to assess the impact of physical parameter perturbations at the terminals of the device, but only for DC device analysis. The key advantage of GF is that they don't rely upon the source of variation, i.e., they can address any source of variations discussed in Chapter 3: GF must be computed once per bias, on the device with reference dimensions and doping.

Already in 1997, [111] proposed physics based model on the numerical solution of the Poisson and Continuity equations (drift diffusion model), which links the process variations and the DC response of the semiconductor device. In this context, two points have to be stressed concerning the expected outcome of physics-based models:

1. An efficient use of physical models based on the semiconductor equations for the optimization of the device parameters with respect to process variations. The basic requirement for these models should not be limited to electrical device performance computation, but it should also compute the gradient variation in response to the technological parameter variations, thus enabling the use of gradient-based, powerful optimization techniques.

2. Within the framework of yield estimate for random variations, physics-based models should efficiently provide not only the expected values for electrical device parameters, but also the self and joint probability distributions of the deviations between actual and expected values.

The gradient variation in the physical models of semiconductor device is termed as the sensitivity of device and can be expressed in terms of small change in any device performance parameter P with respect to the process variations σ(discussed in Chapter 3)

$$S_{\sigma}^{P} = \frac{\delta P}{\delta \sigma} \tag{4.1}$$

Computation of the device sensitivity by numerical differentiation requires a large amount of time and are with questionable accuracy. Similarly, the electrical responses can be estimated with the randomly distributed data using the direct analysis, i.e., repeating the device simulation for randomized input data. If the

variations are small, the statistical characterization of the electrical parameters could be obtained through the first-order approximation:

$$\Delta P = S_\sigma^P \Delta\sigma \tag{4.2}$$

where $\Delta\sigma$ is a random variable describing the small change in technological parameter with respect to its nominal value; ΔP is the slight change in device performance from P [111].

Donati et al. in [111] proposed an efficient technique exploiting the GFs ability for evaluation of monopolar device sensitivities. They estimated the overall sensitivity of the device as a volume integral of local sensitivities.

$$S_\sigma^P = \int_\Omega s_\sigma^P(\mathbf{r}) d\mathbf{r} \tag{4.3}$$

where Ω is the device volume. In [107], the local sensitivity $s_\sigma^P(\mathbf{r})$ is shown as the composition of the local perturbation source *f(**r**)* and of a GF *G(**r**)*.

$$s_\sigma^P(\mathbf{r}) = G(\mathbf{r}) f(\mathbf{r}) \tag{4.4}$$

What's more important is that the computation of this GF can be done with the *adjoint approach*, derived from the adjoint approach to sensitivity analyses of electrical systems [112]. To imply *adjoint technique* beyond monopolar devices, with the help of the application of *Branin's method*, the more *generalized adjoint approach* was introduced [113]. This *generalized adjoint approach* can be used to estimate the GF [110], avoiding the repeated analyses.

The computational advantages of a GF approach in the evaluation of the device sensitivity with respect to more than one technological or physical parameter will be discussed in later part of this chapter. We will start with discussion of Drift Diffusion modeling and how this novel GF approach can be exploited to drift diffusion model of semiconductor devices.

4.3 Drift Diffusion Modeling

Drift-diffusion model can yield an acceptable estimate of the device performances also in nano-scale devices, provided that equivalent transport parameters are suitably introduced into the model. The hole and electron current densities, Poisson equation and the continuity equation together forms the drift diffusion model. The Poisson equation of the system is given as:

$$\nabla^2\phi = -\frac{q}{\varepsilon}(p - n + N^+) \tag{4.5}$$

Now, the continuity equations for the carriers can be written as:

$$\frac{\delta n}{\delta t} = \frac{1}{q}\nabla J_n - U_n \tag{4.6}$$

$$\frac{\delta p}{\delta t} = \frac{1}{q}\nabla J_p - U_p \tag{4.7}$$

Here, ϕ is the potential, q is the electron charge, ε is the dielectric constant. Hole and electron concentrations are given by p and n, while N^+ is the ionized doping. Recombination rates are given as U_p and U_n for hole and electron respectively. J_p and J_n are the hole and electron current densities.

$$J_n = qn\mu_n\nabla_\varphi + qD_n\nabla n \tag{4.8}$$

$$J_p = qp\mu_p\nabla_\varphi + qD_p\nabla p \tag{4.9}$$

where μ_n and μ_p are the electron and hole mobilities. The diffusitivities for electron and hole are D_n and D_p.

4.3.1 Greens Function approach to Drift Diffusion Model

GF approach is applied here on the drift diffusion model already discussed above. The drift diffusion model is now converted into a compact form, highlighting boundary conditions as:

$$\mathbf{F}(\phi, n, p, \dot{n}, \dot{p}) = \mathbf{0} \tag{4.10}$$

$$\mathbf{b}(\phi, n, p, \dot{n}, \dot{p}, s_e) = \mathbf{0} \tag{4.11}$$

F and **b** represent the discretized equations representing discretized form of equations 4.5, 4.6 and 4.7. **F** is a nonlinear system of dimension 3×N, where N are the number of discretization nodes. $\dot{p}$ and $\dot{n}$ are the first derivative of the carriers with respect to the time i.e., $\frac{\partial x}{\partial t}$, here x= n, p, ϕ. Equation 4.11 shows the boundary conditions including the electrical sources external to the system. The set of discretized boundary condition of dimension 3×M, where M is the number of device terminals and is denoted through the system **b**=0.

Let's suppose this system is perturbed with very small variation: the variation is such that the system can be linearized around the working point. The working point solution can be represented as ϕ_0 , n_0 and p_0. Similarly, the linear response (assuming small perturbations) to the external perturbation can be expressed in terms of $\delta\phi$, δn and δp. By aggregating the different perturbations s and the corresponding variations to the system, the system can be expressed by:

$$\mathbf{F}(\phi_0 + \delta\phi, n_0 + \delta n, p_0 + \delta p, \delta\dot{n}, \delta\dot{p}) = \mathbf{s} \tag{4.12}$$

$$\mathbf{b}(\phi_0 + \delta\phi, n_0 + \delta n, p_0 + \delta p, \delta\dot{n}, \delta\dot{p}, \mathbf{s}_{e0}) = 0 \tag{4.13}$$

where, $\mathbf{s}$ represents the noise sources (due to parametric variations) exciting the system linearly.

It should be noted that the perturbation should be high enough to excite the device. But high perturbations, push the device beyond linearity. So, we have to keep the device perturbations small to excite the device linearly. The linearized system around the working point is:

$$\left.\frac{\partial F}{\partial \phi}\right|_0 \delta\phi + \left.\frac{\partial F}{\partial n}\right|_0 \delta n + \left.\frac{\partial F}{\partial p}\right|_0 \delta p + \left.\frac{\partial F}{\partial \dot{n}}\right|_0 \delta\dot{n} + \left.\frac{\partial F}{\partial \dot{p}}\right|_0 \delta\dot{p} = \mathbf{s} \tag{4.14}$$

$$\left.\frac{\partial b}{\partial \phi}\right|_0 \delta\phi + \left.\frac{\partial b}{\partial n}\right|_0 \delta n + \left.\frac{\partial b}{\partial p}\right|_0 \delta p + \left.\frac{\partial b}{\partial \dot{n}}\right|_0 \delta\dot{n} + \left.\frac{\partial b}{\partial \dot{p}}\right|_0 \delta\dot{p} = 0 \tag{4.15}$$

Systems defined by the equations 4.14 and 4.15 can be solved using a GF approach. The GFs can be expressed as $G_{\alpha,\beta}(r, r_1; t, t_1)(\alpha, \beta = \phi,\ n,\ p)$ for equation output α and input variable β , i.e., the response in the variable α to the unit source $\delta(r - r_1)\ \delta(t - t_1)$ injected in equation β. Here, we use the notation $\beta = (\phi,\ n,\ p)$ and $\mathrm{F}_\phi =$ *Poisson equation*, $F_n =$ *electron continuity equation and* $F_p =$ *hole continuity equation*. Now, we can finally calculate the fluctuations $\delta\alpha$ induced by the vector source s as the spatial and temporal convolution integrals:

$$\delta\alpha(\mathbf{r}, t) = \sum_{\beta=\phi,n,p} \int_\Omega \int_{-\infty}^{t} G_{\alpha,\beta}(\mathbf{r}, r_1; t, t_1)\ s_\beta(r_1, t_1) dt_1 dr_1 \tag{4.16}$$

where Ω is the system volume.

Hence, once all the GFs are computed, the sensitivities can be easily evaluated.

4.3.2 Advantages of Green's Function

The stand-out point of the proposed strategy in comparison to other approaches is that the allocation of the computational resources is very limited when using GF approach. For example, in [9], a full sensitivity analysis of an SRAM cell with around 1 million grid nodes was demonstrated. [9] analyzed the simulation time for 3D 6Transistor SRAM computing the sIFM (Statistical Impedance Field method exploiting GFs for device analysis). 1000 samples of randomly distributed doping with their total simulation time was estimated to be around 40 hours. It requires around 50% of 40 hours for the evaluation of DC solution and 46% was consumed for the evaluation of GF. The remaining 4% was consumed for computation of the linear responses to the 1000 deviations of doping from the nominal value. It can

be concluded that this method becomes more and more efficient with the increase in the number of randomizations in comparison to other approaches, e.g, atomistic approach which would require 1000 simulations.

In the GF approach the device sensitivity with respect to a parameter is expressed as a volume integral (or, in discretized form, as a node summation), whose integrand can be interpreted as a distributed parametric sensitivity. The knowledge of the spatial behavior of the sensitivity clearly allows deeper insight into which regions of the device display high or low sensitivity with respect to a given parameter and is, therefore, a valuable design tool. This unique capability of GFs approach is discussed in Chapter 6.

4.4 Application of Greens Function to Sensitivity of FinFET devices

GFs approach has been studied in many works like [114], [115], and [116]. In this section, we will discuss two different variations taken as an example to understand the approach of GF to sensitivity of FinFET. The two variables under consideration here will be RDF and Geometric variations. Keeping them separate because of the fact that Geometric variation requires remeshing as discussed in 4.4.2.

4.4.1 Sensitivity to RDF using Green's Function approach

IFM employed by commercial softwares (Synopsis) exploits GF approach [109]. In the IFM, the local doping fluctuations are presumed to be very small to permit the linearization of the system around the working point. IFM techniques can be utilized to calculate the terminal characteristic's fluctuations in consequence of RDF and also identifies the contributions of the dominant fluctuating location within the semiconductor device. This technique can be considered for optimizing and model RDF devices robust towards RDF.

In Synopsis [117], a large quantity of randomized doping profiles are generated via this method from average doping profile. The concentrations of acceptors and donors are randomized autonomously, presuming dopants to be uncorrelated spatially using Poisson distribution function. Therefore, the probability to find k dopants in the box of vertex i is:

$$P_i(k) = \frac{(N_i V_i)^k}{k!} e^{(-N_i V_i)} \tag{4.17}$$

where i is the vertex's index with volume V_i, and N_i is the average doping concentration pertaining to the same node. Due to RDF, a fluctuation of current at short circuited terminals is observed, by keeping the voltage at terminals constant. The doping distribution of the nominal device is denoted by N_i and each of random

doping realizations are denoted by N_v. If the fluctuations in doping profile $N_v(r) - N_i(r)$ is small, the current variation is found linearly, using equation as follows:

$$\delta I_c = \int_{\Omega} d^3 r G_{Ic}(r)[N_v(r) - N_i(r)] \tag{4.18}$$

where Ω is the device volume, the GF of current at terminal c is G_{Ic}. One device simulation is sufficient to acquire GF, and due to linearization, any change in terminal attributes for specified doping variation can be easily calculated from 4.18. This model has been adopted by [109]. It is also used by [118]. Wettstein et al. performed RDF analysis using the IFM employed by Synopsis and concluded that IFM technique is much faster, yet accurate, than conventional statistical methods.

4.4.2 Sensitivity to Geometric variations using Green's Function approach

In [119], Gnudi et al. introduced the sensitivity formulation for device design modeling using a linearized method. In their work they presented the variations in the electrical parameters with respect to geometrical fluctuations and proposed remeshing of the device for geometrical variations to conform to new device geometry. In [120], the idea was further developed and GF has been proposed and studied in detail for geometrical variations.

Contrary to dopant variations, for geometrical variations, it is important to remesh the device, due to change in the geometrical parameters. This remeshing results in the re-allocation of the node coordinates. First we re-write the discrete Drift-Diffusion like in 4.10 with explicit mode dependency:

$$F_{\phi}(\phi, n, p, x_i, y_i) = 0 \tag{4.19}$$

$$F_{n}(\phi, n, p, x_i, y_i) = 0 \tag{4.20}$$

$$F_{p}(\phi, n, p, x_i, y_i) = 0 \tag{4.21}$$

where ϕ ,n and p are the potential and carrier concentration in the device under study. Note, that $\{x_i, y_i\}$ are the node coordinates in a 2D device structure (3D generalization is straight-forward). Now, due to structural variations in device geometry, we force the proportional variations in the mesh of the device. This remeshing is possible for the small variations of the nodal coordinates. These new coordinates can be shown as:

$$x_i = x_i^0 + \delta x_i, \qquad y_i = y_i^0 + \delta y_i \tag{4.22}$$

where δx_i and δy_i are minor variations of nodal points such that the grid on the

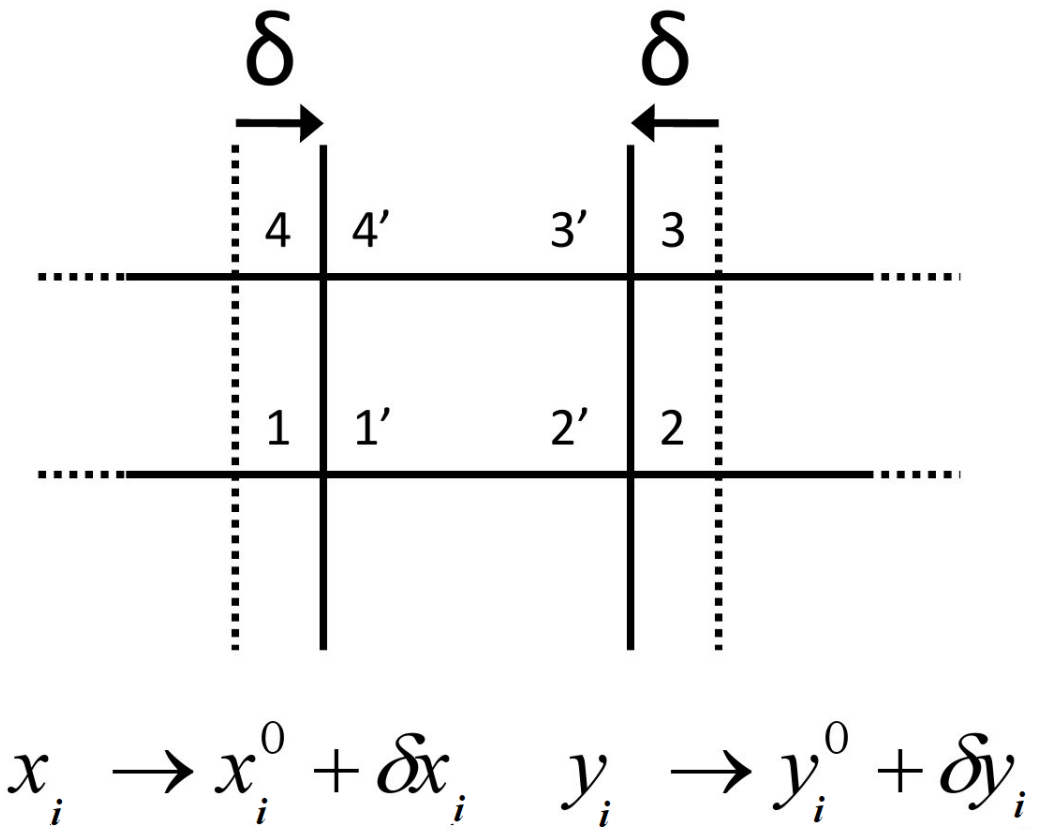

Figure 4.1: Variation in mesh points w.r.t. variation in geometry of the device

geometry stays valid. As an example, if there is fin width increment in a FinFET as parametric variation, then the nodes can be moved uniformly to mimic fin width variations. The resulting mesh is more stretched in the direction of geometry by varying the length of the region, recalculating the mesh keeping the connectivity of the old mesh intact. In response to the small geometric variations, the change in the physical parameters can be shown as:

$$\phi = \phi^0 + \delta\phi, \qquad n = n^0 + \delta n, \qquad p = p^0 + \delta p \tag{4.23}$$

here, $\delta\phi$, δn and δp shows the small change.
Now, we will rewrite the drift diffusion model with variations as:

$$F_\phi(\phi^0 + \delta\phi, n^0 + \delta n, p^0 + \delta p, x_i^0 + \delta x_i, y_i^0 + \delta y_i) = 0 \tag{4.24}$$

$$F_n(\phi^0 + \delta\phi, n^0 + \delta n, p^0 + \delta p, x_i^0 + \delta x_i, y_i^0 + \delta y_i) = 0 \tag{4.25}$$

$$F_p(\phi^0 + \delta\phi, n^0 + \delta n, p^0 + \delta p, x_i^0 + \delta x_i, y_i^0 + \delta y_i) = 0 \tag{4.26}$$

We will be focusing on the Poisson equation going forward, as it can be implemented easily in both the carrier continuity equations as well.

Here, we will use the same analysis carried out from Eq. 4.10-4.15 and will incorporate the variation source. Now, if we linearize the Poisson equation, we will get two terms:

$$\begin{aligned} & F_\phi(\phi^0, n^0, p^0, x_i^0, y_i^0) + ... && 1^{st} term \\ & \left.\frac{\partial F_\phi}{\partial \phi}\right|_0 \delta\phi + \left.\frac{\partial F_\phi}{\partial n}\right|_0 \delta n + \left.\frac{\partial F_\phi}{\partial p}\right|_0 \delta p + \left.\frac{\partial F_\phi}{\partial x_i}\right|_0 \delta x_i + \left.\frac{\partial F_\phi}{\partial y_i}\right|_0 \delta y_i = 0 && 2^{nd} term \end{aligned} \tag{4.27}$$

The first part in Eq. 4.27 is the equation of the system without any variation and is equals to zero for this case. While the second term is reassembled as:

$$\left.\frac{\partial F_\phi}{\partial \phi}\right|_0 \delta\phi + \left.\frac{\partial F_\phi}{\partial n}\right|_0 \delta n + \left.\frac{\partial F_\phi}{\partial p}\right|_0 \delta p = -\left.\frac{\partial F_\phi}{\partial x_i}\right|_0 \delta x_i + \left.\frac{\partial F_\phi}{\partial y_i}\right|_0 \delta y_i \tag{4.28}$$

The left hand side of Eq. 4.28 is the Poisson equation computed with the nominal values of the geometrical parameters and without any remeshing of the grid. While RHS represents the variations in the nominal physical values corresponding to the change in the grid of the device structure.

The general algorithm to be considered for the evaluation of variations can be as follows:

1. The solution of the system should be evaluated at the nominal values. The residual of the system is zero here
2. calculate the geometrical variations
3. remesh the grid to minimize geometry variations
4. with the new mesh points the residual will be at non-zero value and this variation, due to the geometrical variations in the system, can be considered as the same variation source s of Eq. 4.12 and 4.13

Hence, we have established that the perturbation in the coordinates can induce variations and can be calculated with the help of residual variations. Now, we can evaluate the impact of geometric variations at device contacts with the help of GF G_α where $\alpha = \{\phi, n, p\}$ is the terminal observable. At the working point, the GF is calculated, and then the same GF is used for the perturbed device.

$$\delta\alpha = -\int_{\Omega} G_{\alpha} F_{\phi} d\sigma = \sum_{i-node} G_{i,\alpha} F_{i,\alpha} A_i = G_{i,\alpha} \Delta RHS_i \tag{4.29}$$

akin to Eq. 4.16, here, Ω is the volume, A_i is the control area of the i_{th} node and ΔRHS_i is the residual of the node.

4.4.3 AC sensitivity analysis using Greens function approach

Enormous amount of efforts has been put on the optimization, modeling, fabrication and even on DC characterization of FinFET devices, but comparatively less efforts have been put on the AC characterization oriented to variability. Recently, GFs approach has been discussed in [121], where the GF methodology has been extended to the AC case. With inconsequential numerical effort with respect to the ordinary DC device simulation time, the sensitivity of the AC admittance martrix can be also evaluated. The test cases for this approach have already been reported in [121]. In this thesis work, we have exploited this methodology for the AC sensitivity analysis on the DG FinFET. Chapter 5 is also presenting the comparison of this approach to conventional incremental approach, where the variability analysis is performed by repeating the experiments, i.e, manually changing the parameter values, with emphasis on the comparison of single and multifin devices. Here in this section, we will review the modeling of AC sensitivity with the GFs approach. Furthermore, it can provide a viable tool to find and demonstrate possible correlations among various variations of various elements of the Y matrix. In this method, the small variations of the Y matrix elements are presented as a function of the process parameter fluctuations.

Preliminary background

The concept of GF approach to variability analysis, revolves around the concept that the physical parameter variations in the device should be small enough to excite the change in the terminal current and should not be large enough (for linearization). GF of the linearizaed model equations is used to provide the link between the internal device variations and the variations in the performance at the device terminals. The AC performance characterization is more complicated in comparison to the DC characterization. Due to the complexity of AC characterization in semiconductor devices, comparatively less efforts are being put on this topic. The complexity of AC variability is due to the fact that it comprises of three components:

- DC solution
- Small AC tone

- Small parameter variation

So, AC variability requires double linearization, one for the AC tone and the other for the parametric variation. The AC tone and the small parametric variation forces the perturbation in the system by a harmonic, small-amplitude input. In sensitivity analysis, the perturbation of the parameter $\Delta\sigma$ is time independent.

In the next section we will focus on AC sensitivity analysis and the GFs device modeling.

Numerical modeling of AC sensitivity analysis

The starting point for AC sensitivity analysis is the large-signal (LS) physics-based model in [114] allowing for harmonic balance–based multitone device simulation of electron devices in periodic or quasi-periodic conditions, including efficient GFs analysis capability. To the best of our knowledge, there are not any commercially tools available for AC characterization using GF method. This technique is exploited in our in-house simulator POLITO (not available commercially). The physical model (PM) is solved with given external applied sources (DC bias + AC or LS tones), yielding the currents flowing in each terminal. Denoting with i_n(t) the current in nth contact, it can be expressed in Fourier series as:

$$i_n(t) = \sum_k I_{n,k} e^{jw_k t}, \tag{4.30}$$

where $I_{n,k}$ is the kth harmonic amplitude, j=$\sqrt{-1}$ and ω_k is the kth harmonic (angular) frequency.

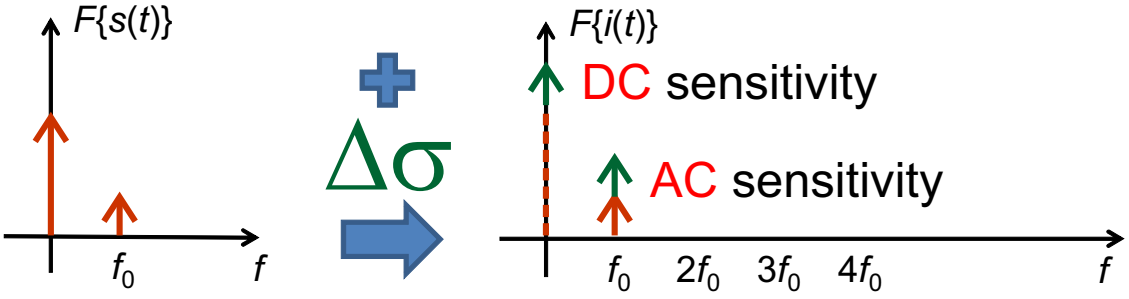

Figure 4.2: Schematic representation of the variability modeling approach. *s(t)* is a terminal applied voltage, *i(t)* the terminal current, *F* the Fourier transform [8].

As shown in Fig. 4.2, current can be represented by a discrete spectrum made of tones. Here, the simpler case with a single AC tone is shown, without any harmonics. This is because the variations are time-independent; hence the displacement frequency is set to zero and the perturbed system is characterized by the same frequency as of the WP.

In the particular case of AC analysis, external sources include DC bias + a small AC voltage tone $V_{j,1}$ at frequency ω_1 recursively applied at each terminal j. The AC tone is so small that the analysis can be limited to k = 0 (DC) and k = ±1 (AC) with no harmonic generation. This corresponds to little numerical overhead with respect to the DC solution: the terminal currents 4.30, also limited to k = 0,±1, are made of the DC component $I_{n,0}$ and of the AC amplitude $I_{n,1}$ ($I_{n,-1}$ is the $I^*_{n,+1}$). From this analysis, the *(n,j)* AC admittance matrix element is obtained, without any need of explicit model linearization:

$$Y_{n,j} = \frac{I_{n,1}}{V_{j,1}} \tag{4.31}$$

Turning to sensitivity analysis, a physical or technological parameter σ undergoes variations $\Delta\sigma$, while keeping the voltage sources at the terminals unchanged, i.e., terminals are effectively short circuited for variations. Short-circuit current variation $\Delta I_{n,1}$, induced by $\Delta\sigma$, is computed again from PM solution, following the GF approach in the LS case. Through the Harmoninc balance algorithm [110] [121]. The variation of the admittance matrix element $\Delta Y_{n,j}$ is simply

$$\Delta Y_{n,j} = \frac{\Delta I_{n,1}}{V_{j,1}} \tag{4.32}$$

Notice that the device, both the one with the nominal parameter σ and the one with variations, is solved with simultaneous DC and AC excitations: therefore, even if we are focused on the AC device response, it is worth noticing that the proposed GF approach allows for the simultaneous DC and AC variability analyses.

To calculate $\Delta I_{n,1}$,we review the perturbation analysis in the general harmonic case and then restrict to $k = 0,\pm1$. When a small local perturbation characterized by frequency ω is applied to a system, described by PM with static or periodic solution as in 4.30, a linearized analysis can be exploited, e.g., following the so-called SS-LS approach [110]. All perturbations, e.g., local sources $s_\alpha(r,t)$and the terminal current perturbation $\Delta i_n(t)$, can be expressed as a superposition of sideband components:

$$s_\alpha(r,t) = \sum_k S^+_{\alpha,k}(r)e^{j\omega^+_k t}; \quad \Delta i_n(t) = \sum_k \Delta I^+_{n,k} e^{j\omega^+_k t}, \tag{4.33}$$

where $\omega^+_k = \omega_k + \omega$ is the kth upper sideband with sideband (angular) frequency ω. According to the GF analysis applied to the linearized PM, the sideband components of the terminal current variations are related to the internal perturbation sources by a convolution integral[122]

$$\Delta I^+_{n,k} = \sum_\alpha \sum_l \int_\Omega \left(G^{(n)}_\alpha(r)\right)_{(k,l)} S^+_{\alpha,l}(r)dr, \tag{4.34}$$

where Ω is the device volume and $G_{\alpha}^{(n)}(r)$ is the conversion Green's function (CGF) corresponding to a unit source in position r and in the equation α of the PM. The pair *(k, l)* denotes conversion from a source at sideband l to the external current variation at sideband k. The graphical interpretation of the CGF method is presented in Fig. 4.3 (a) for a 3-terminal device example. Fig. 4.3 (b) shows the same, but in the frequency domain, highlighting the frequency conversion mechanism from a source at the l^{th} sideband to a terminal current variation at the kth sideband.

Turning to the particular case of the parametric sensitivity, notice that perturbations of physical or technological parameters are generally static; hence, we need to set $\omega = 0$. In this case, sidebands ω_k^+ collapse into the unperturbed spectrum ω_k, while sideband amplitudes $\Delta I_{n,k}^+$ collapse into variations of the phasors $\Delta I_{n,k}$. If we address in particular the AC sensitivity analysis, the harmonic indexes must be further limited to $k = 1$, $l = 0,\pm1$, simplifying the frequency spectrum and leading to the representation of Fig 4.3 (c), where the relevant elements of the CGF contributing to $\Delta I_{n,1}$, are shown. The same concept is more simple shown in Fig. 4.2 on the right.

We are left with the problem of characterizing the local perturbation sources $s_{\alpha}(r,t)$, linking them to parameter variations $\Delta\sigma$. Obviously, $\Delta\sigma$ causes a spatially distributed perturbation in the discretized PM equations: for instance, a geometric perturbation causes a variation of the discretization mesh [122], a doping variation determines a perturbation on the right-hand side of the Poisson equation and, as

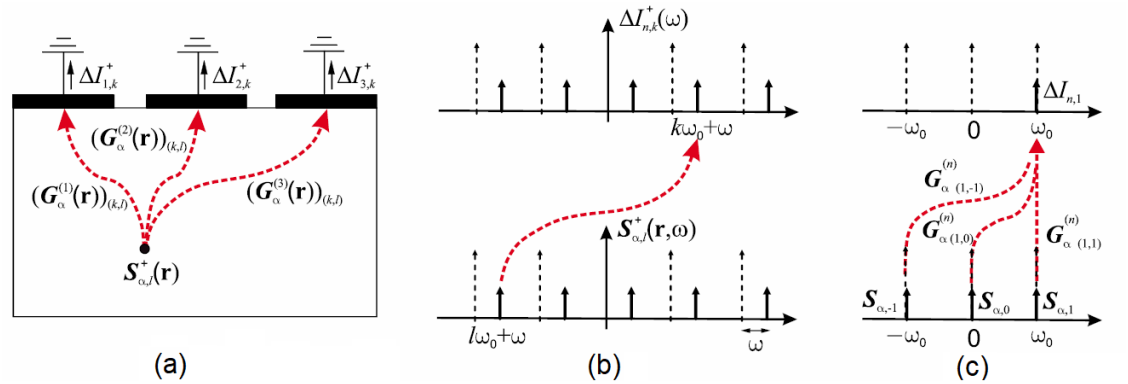

Figure 4.3: Schematic representation of the conversion Green's function (CGF) approach for sensitivity analysis. (a) graphical interpretation of the CGF operation. Local sources in equation α (Poisson, electron, or hole continuity) and lth sideband are propagated resulting in short-circuit variations of the terminal current at the kth sideband. (b) graphical interpretation in the frequency domain. Dashed lines represent the unperturbed solution, solid lines perturbations. (c) AC variability analysis obtained from B with $\omega = 0$, $k = 1$, and $l = 0,\pm1$. The relevant CGFs are the (1,−1), (1,0) and (1,1) elements

a consequence, a perturbation on the carrier mobilities that, in turn, imply a perturbation of continuity equations, etc. In other words, $\Delta\sigma$ induces a perturbation source $\Delta\sigma(\mathrm{r},\ \mathrm{t}) \propto \Delta\sigma$ appearing in the linearized PM model equations F_α (e.g., in the drift-diffusion model, α refers to either Poisson, electron, or hole continuity equations). In general, if the discretized α equations of PM are collected in the system:

$$F_\alpha(n, \varphi, p, \sigma) = 0, \tag{4.35}$$

the local source can be found by changing the only value of parameter σ without any variation in the internal solution or external applied sources:

$$s_\alpha(r,t) = F_\alpha(n_0, \varphi_0, p_0, \sigma_0 + \Delta\sigma) - F_\alpha(n_0, \varphi_0, p_0, \sigma_0) \simeq F_\alpha(n_0, \varphi_0, p_0, \sigma_0 + \Delta\sigma), \tag{4.36}$$

since $F_\alpha(n_0, \varphi_0, p_0, \sigma_0)$ is null when evaluated with the nominal internal solution n_0, φ_0 and p_0 and the nominal parameter σ_0. Notice that while variations of the parameter σ are static by definition, the induced local variation $s_\alpha(\mathrm{r},\ \mathrm{t})$ is in general time varying. In fact, the function F is periodic when calculated with the periodic solution n_0, φ_0 , p_0 : hence, the local source $F_\alpha(n_0, \varphi_0, p_0, \sigma_0 + \Delta\sigma)$ is in general also periodic, characterized by both DC and AC components, as represented in Fig. 4.3 (c). A particular case occurs only when F can be decomposed as

$$F_\alpha(n_0, \varphi_0, p_0, \sigma_0 + \Delta\sigma) = F_\alpha^{(a)}(n_0, \varphi_0, p_0) + F_\alpha^{(b)}(\sigma_0 + \Delta\sigma) \tag{4.37}$$

i.e., it does not contain mixed products or nonlinear functions of the physical parameter and of the electrical variables. Then, using the unperturbed solution $\mathrm{F}_\alpha^{(a)}(n_0, \varphi_0, p_0) + F^{(b)}(\sigma_0) = 0$, it turns out that the local source $\mathrm{s}_\alpha(r,t) = F^{(b)}(\sigma_0 + \Delta\sigma) - F^{(b)}(\sigma_0)$ contains only a DC component. This is a relevant case, which occurs, for example, when we consider the parameter σ to represent doping variations in the Poisson equation: since the net charge depends linearly on doping, the local source of the Poisson equation is purely static. For such variations, the only relevant term of the GF is the (1,0) element, converting DC local variations into AC terminal current variations (see again Fig. 4.3 (c)). On the contrary, geometric variations are usually taken into account by a deformation of the discretization mesh [122], i.e., $\Delta\sigma$ represents the variation of the nodal coordinates, see previous section 4.4.2. Nodal positions contribute in a nonlinear way to PM equations, usually discretized by means of the finite-boxes approach, hence leading to local sources that are in general fully periodic. Furthermore, in general, they are also mesh dependent.

4.5 Summary

This chapter is focused on the modeling of variability analysis. In the previous chapters, we focused on the understanding of the parametric variations, influencing the device performance. Proper modeling of the device is also very important to predict the device behavior before fabricating the devices commercially. In this chapter, we focused on modeling of device variability using GFs approach. We discussed the background of GFs and its application to DC sensitivity.

Following built-in examples of a commercial simulator (Synopsys), we described, how Gfs can be applied with success for variability analysis, e.g., in its application on the characterization of random dopant fluctuations and geometric variations. Although we presented the GF modeling approach, only for RDF and geometrical variations, it can be applied to all the variability sources described in chapter 3. GF is applicable to variability analysis of all parameters, with the condition that the effect of variations are small enough to be linearized.

In the last part of the chapter, we focused on the peculiar problem of AC sensitivity modeling which represents to core methodology of this work. We exploit the unique features of the POLITO in-house simulator for AC sensitivity analysis. This simulator circumvents the need of double linearization for AC variability analysis.

In the coming chapters, we will focus on AC variability analysis of FinFET device using POLITO in-house simulator. We also highlight the GFs validity and its comparison with conventional incremental, repeated AC analyses approach.

Chapter 5

AC variability analysis of DG FinFET

Device simulations can give physical insight for explaining the effects observed through measurements. As, we have developed the idea of variability impact on DC and AC performance of the device, in this chapter, we will use our in-house simulator to perform physics based variability analysis of DG FinFETs AC performance as the function of relevant variability sources. In previous chapters, we discussed different variability sources and their impact on the device performance and we also discussed modeling of device variability using GFs. We will now perform our analysis on the device performance. In addition to it, we will be using POLITO (presented in appendix A) exploiting the GFs approach and will compare the results of such an approach with an incremental approach both from POLITO, while all results have been also verified with Sentaurus Synopsys TCAD simulations.

In this chapter, we focus on the AC analysis of the single fin (hereafter SF) and double fin DG FinFET. For the validation of our GF approach, we performed AC performance simulations on Single fin DG FinFET and Double Fin DG FinFET.

5.1 Single Fin FinFET variability analysis and Green's Function validity

Importance of AC variability has already been well understood. In this section, we will focus on AC variability of SF DG FinFET and will also validate the GF approach. We compared the GF results with an incremental approach, where the variability analysis is performed by repeating the simulations, i.e., manually changing parameter values.

Physical simulations directly provide the Y matrix of the simulated device, including parasitics, intrinsic and dynamic elements. Despite simulations can be used as "virtual measurement" to extract and/or assess an equivalent circuit, in this

thesis, we have focused just on the elements of the Y matrix and their variations. Detailed comparison with circuit in Fig. 2.10 may be then used to grasp the correspondence of the real and imaginary parts of the Y matrix to circuit elements.

The physics based AC sensitivity analysis from POLITO has been applied first to the DG structure, shown in Fig. 5.1 representing a 2D cross section of a nanometer scale tri-gate FinFET: here, two gates are considered as short-circuited. The process variations which we have selected are relevant to AC analysis, i.e., fin width (hereafter WF), the gate/source(drain) distance (LDE) and the S/D doping (DOP). The reason for selection of these parameters is their direct influence on the parasitics of the FinFET device, hence, these geometrical parameters play a very important role in the overall RF device performance. With the aim of a possible development of small-signal high gain or of a low noise amplifier for small-cell applications, 60GHz of operating frequency is considered and the bias condition is V_{GS} = 0.6 V and V_{DS} = 1 V to result in 0.4 mA/mm of drain current, corresponding to a possible bias for a power amplifier in class AB.

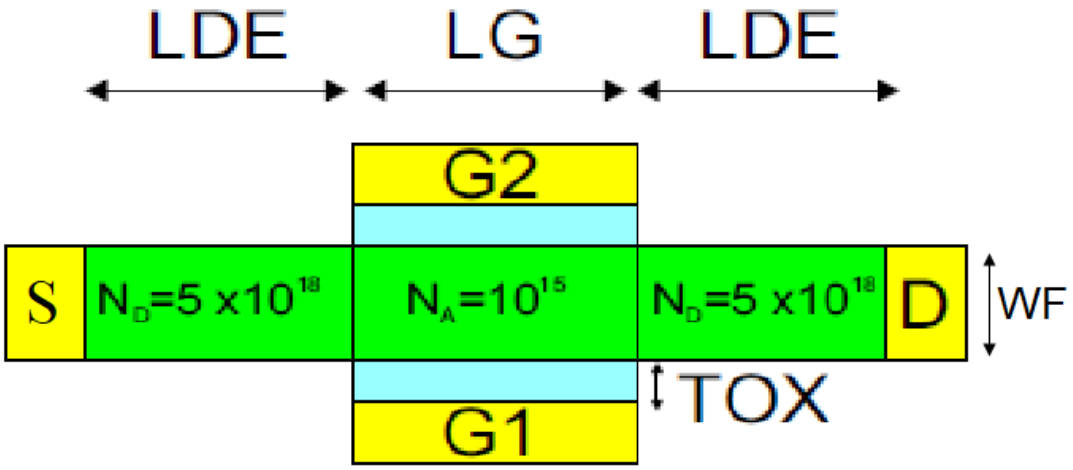

Figure 5.1: Single Fin DG FinFET structure and geometrical definitions. Green represents Si region, the light blue is SiO_2 and yellow represents ideal metal gate [8].

Table 5.1: Geometrical Parameters for DG FinFET device structure [8].

Parameter	**Dimensions (nm)**
Equivalent SiO_2 TOX	1
LG	54
LDE	54
WF	10

To study the impact of process parametric variations on the AC performance, we applied deterministic variations upto 20% of their nominal value, e.g., WF of 20% can result in device, with 8 nm or 12 nm of fin width. For the AC analysis of SG DG device, we will sum up the contributions of the two shorted gates in the Y parameters, e.g.,

$$\begin{aligned} Y_{G,D} &= Y_{G1,D} + Y_{G2,D} \\ Y_{G,G} &= Y_{G1,G1} + Y_{G1,G2} + Y_{G2,G1} + Y_{G2,G2} \end{aligned} \tag{5.1}$$

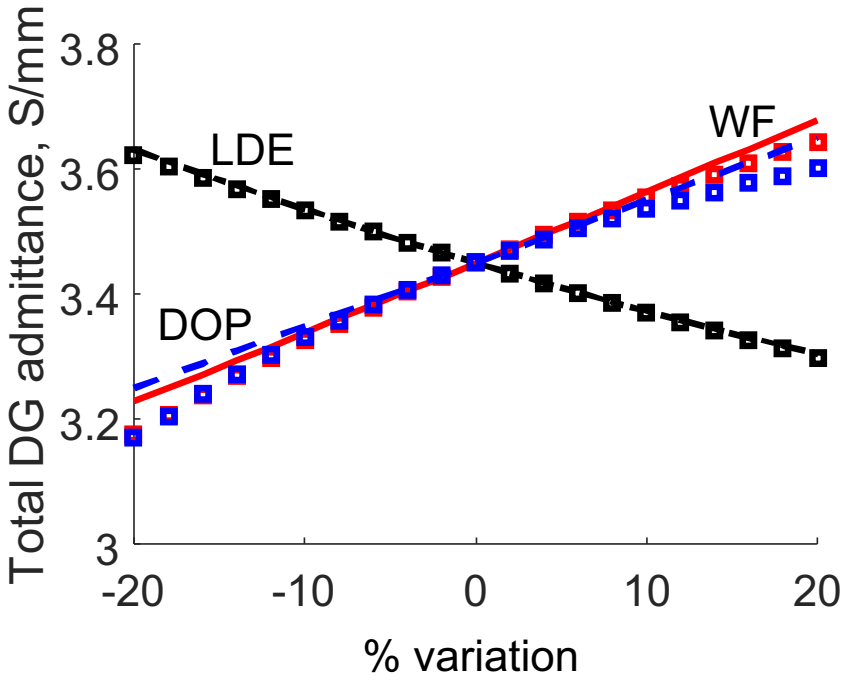

Figure 5.2: Real part of drain-gate admittance for single fin SG DG FinFET device vs. 20% parameter variations. Colors: red represents fin variations, black represents source/drain extension length variations and blue represents source/drain doping variations. GFs simulations are shown by solid lines and incremental approach is shown by symbols [8]

In Fig. 5.2, GF simulations are shown by solid lines and incremental approach is shown by symbols. Fig. 5.2 shows the real part of the drain-gate(DG) element of the admittance matrix Y plotted against percentage parameter variations, i.e., summing contributions of both gates, see eq. 5.1. The GF approach is showing significant accuracy in comparison to the incremental approach despite the reduction of simulation time. The drain-gate element is related to the total transconductance. It is evident that nearly exact tracking of the WF and DOP variations is observed. Around 10% variations are observed, suggesting that transconductance,

significantly depends on the parasitic resistance of the S/D region. Increasing either DOP or WF reduces the parasitic resistance: the admittance variations are linearly increasing with these variation parameters, with the near same slope. Opposite is observed for the LDE variations, i.e., with the increase in LDE variations, the transconductance is decreasing. This is due to the increase in the parasitic resistance of extensions. From Fig. 5.2, we can observe around 10% increase in DG element from its nominal value w.r.t. WF, which shows the significant sensitivity of device transconductance to the WF. The increasing effect on transconductance with the increase in doping is due to the availability of more carriers to constitute the flow of current.

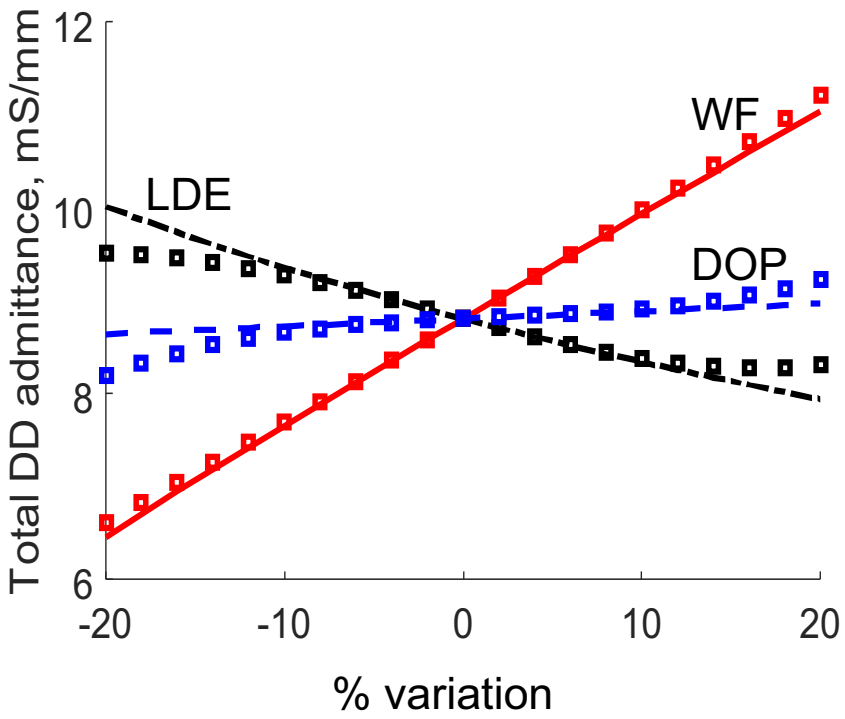

Figure 5.3: Real part of drain-drain admittance for single fin SG DG FinFET device vs. 20% parameter variations. Colors: red represents fin variations, black represents source/drain extension length variations and blue represents source/drain doping variations [8]

Fig. 5.3 shows the drain-drain(DD) element of the admittance matrix. We observe, the significant impact of 20% variations in relevant parameters. Drain-gate and drain-drain element follow the similar trend for all parameters, except that the magnitude of DD admittance variation is less marked as a function of DOP variations. The milder effect of doping variations can be explained by the fact that, on one side,it reduces parasitic resistance, but on the other side it increases SCE. Also from Fig. 5.2, we observe that increasing WF results in lower parasitic

resistance and higher on-current, while increasing LDE results in an increase in parasitic resistance. And these two, i.e., parasitic resistances and SCE have the opposite effect on the output conductance.

Turning to the capacitive components, we report the imaginary part of the Y matrix divided by the angular frequency, i.e., the capacitances. This is just the imaginary part of the Y matrix element normalized by ω and is not directly related to any of the capacitances of an equivalent circuit. Although, in a loose sense, GG capacitance is related to the C_{gs} of the equivalent circuit, they are not identical. In Fig. 5.4, the gate-gate GG capacitance is shown. The percent variation in response to 20% variations in the process parameters is limited to 3-4%. In-fact, the process variations considered here, mainly affect the parasitic capacitances, which are too small in comparison to the total gate capacitances. DOP and WF are closely related.

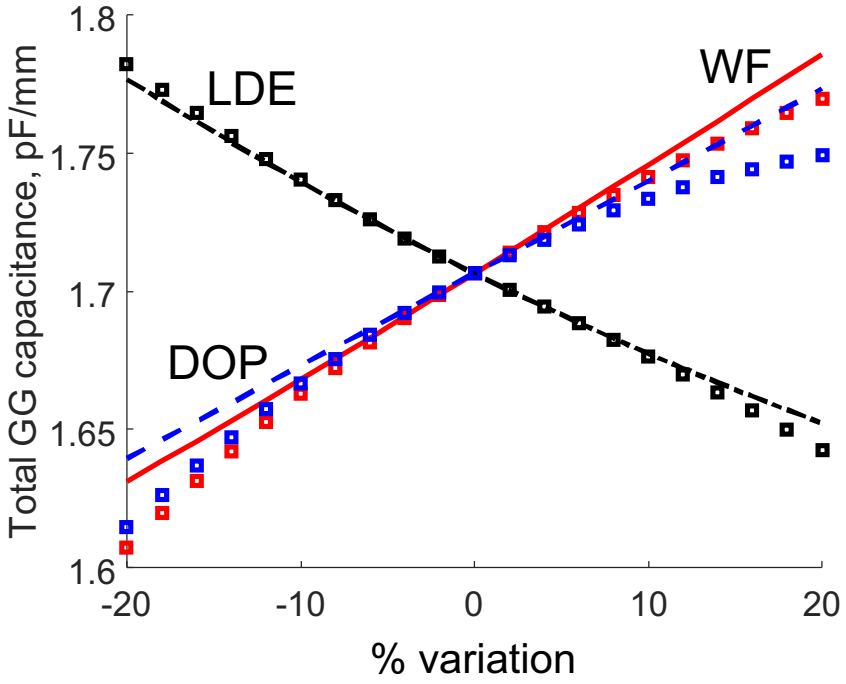

Figure 5.4: Imaginary part of gate-gate element for single fin SG DG FinFET device vs. 20% parameter variations [8].

Variations on drain-gate capacitances can be seen in the Fig. 5.2. The drain-gate element is less affected by the variations in comparison to the gate-gate capacitances.

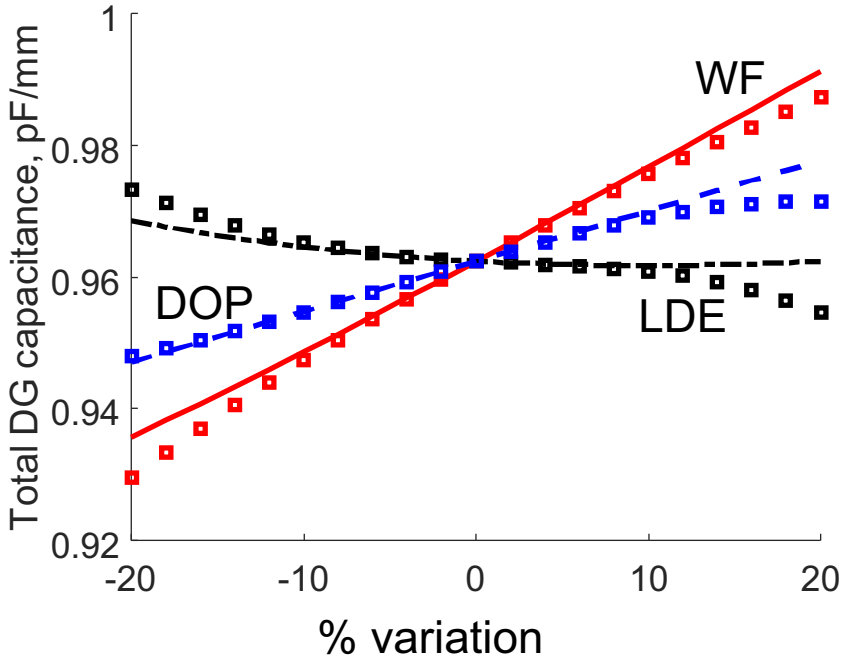

Figure 5.5: Imaginary part of drain-gate element for single fin SG DG FinFET device vs. 20% parameter variations [8].

Finally, the DD element response to WF, DOP and LDE variation is shown in Fig. 5.6, we can see that, DD capacitance is smaller in comparison to the capacitive variations discussed above, but they are the most affected by the variations. Also, WF is seen to be the most dominant parameter in comparison to the other variations for all capacitances, i.e., GG, DG and DD.

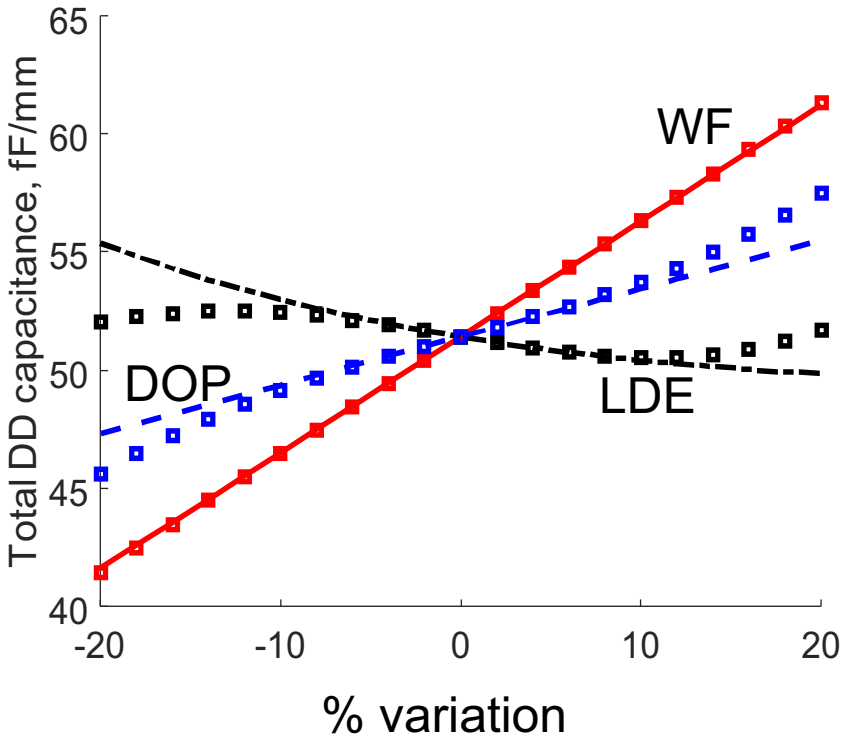

Figure 5.6: Imaginary part of drain-drain element for single fin SG DG FinFET device vs. 20% parameter variations [8].

Finally, from the Y parameters we extract the variations on the cutoff frequency resulting from the process variations. For cutoff frequency analysis, we limit our parametric variations to 10%. Fig. 5.7 show results: the cutoff frequency of the single fin is quite high because in a single fin FinFET, many capacitive parasitics are not considered. It is common practice to use the parameter H_{21} to extract the cut-off frequency. Hence, a direct small signal analysis of complex structures can crucially ease device design and circuit development. For the device shown in Fig. 5.1, we calculated the short circuit current gain H_{21} in order to calculate the cutoff frequency found at the intersection of unity gain point. The fine tuning was made by linear interpolation on the simulation data, which were on a discrete set of frequencies. We can see from the Fig. 5.7, that the spread of cutoff frequency is around 6 GHz. This can be due to the fact that cutoff frequency is more or less directly proportional to transconductance and inversely proportional to the gate capacitance; since the impact of both these parameters is similar,notice that frequency spread is reduced.

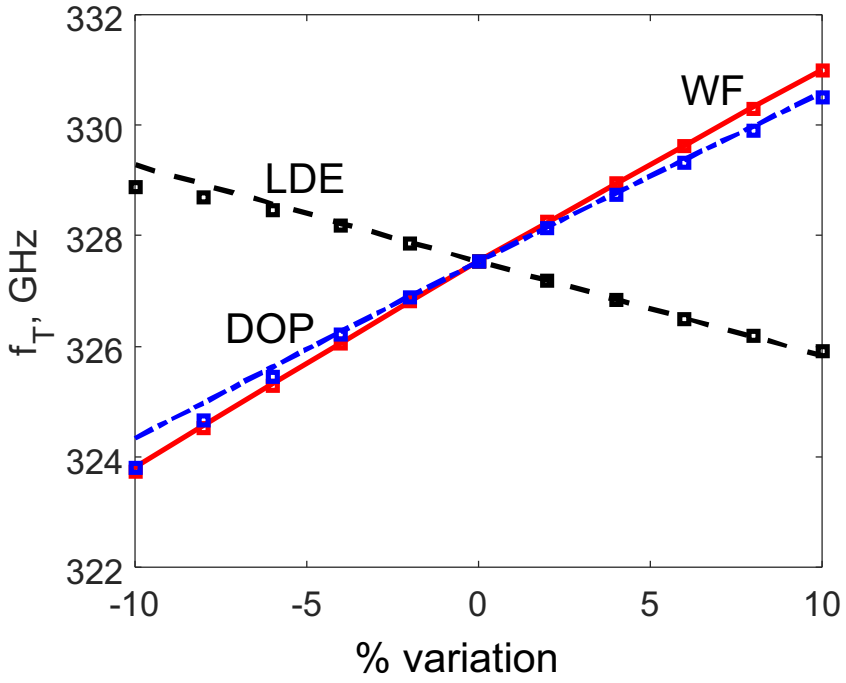

Figure 5.7: Cutoff frequency f_t of the single fin SG DG device vs parameter variations [8].

5.2 Bias dependent sensitivity analysis of SF DG FinFET

Device sensitivity may strongly depend on bias. Figures 5.8 and 5.9 show the admittance and capacitance sensitivities with varying V_{GS}. Here, we show the results as a function of bias and with a fixed 5% parameter variation. Fig. 5.8 (a), shows the real part of the Y matrix drain-gate element. It is remarkable that the sensitivity to parameters that purely affect parasitics (LDE and DOP) is approximately null until the device turns on, roughly around the threshold voltage $V_{GS} = 0.4$ V. On the contrary, WF is a global parameter, affecting both the intrinsic and extrinsic device behavior. In particular, it is known that the drain current turns out to be proportional to WF in subthreshold [123], while milder dependency is expected above the threshold. This is reflected in Fig. 5.8, showing that WF sensitivity is very high in subthreshold, i.e., around 10% for the 5% parameter variations in process parameters, then decreases, and finally roughly tracks DOP variations above the threshold. This further confirms that the WF sensitivity above threshold is mainly via the parasitic resistances. LDE sensitivity is also increasing with V_{GS}, despite its percent variations remain smaller than the others.

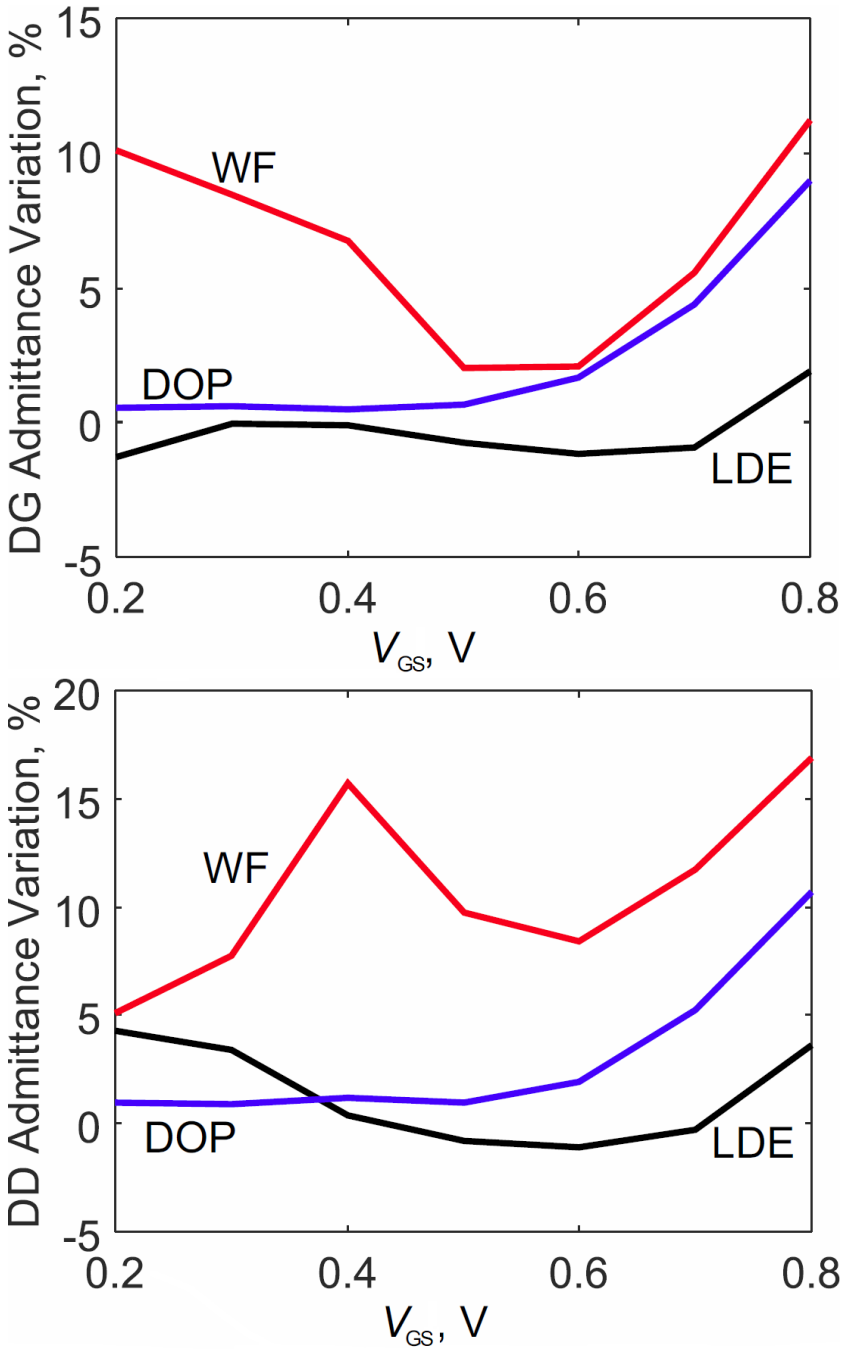

Figure 5.8: (**a**) Bias dependency of the Drain-Gate. (**b**) Drain-Drain admittances percentage variation, resulting from a 5% variation of DOP (blue lines), WF (red lines) and LDE (black lines). Frequency is 60 GHz [124].

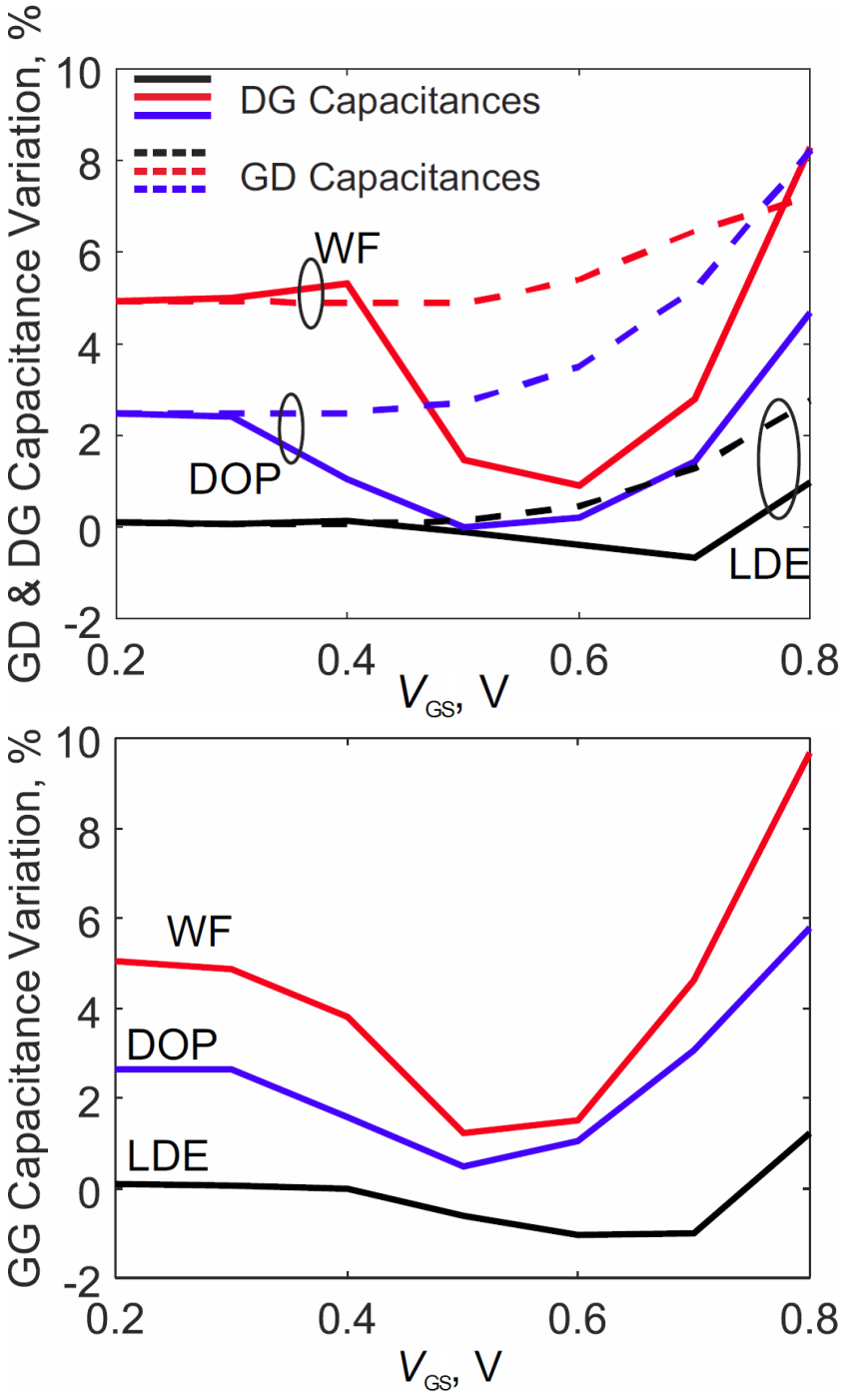

Figure 5.9: (**a**) Bias dependency of the Gate-Drain and Drain-Gate. (**b**) Gate-Gate capacitance percentage variation, resulting from a 5% variation of DOP (blue lines), WF (red lines) and LDE (black lines). Frequency is 60 GHz [124].

Turning to the drain output admittance shown in Fig. 5.8 (a), its variation

with respect to DOP is very similar to the drain-gate element, and the amount of variation is also the same; instead, the WF sensitivity here is extremely high, with a peak around the threshold. Interestingly, the sensitivity above threshold first decreases with V_{GS} and then increases again. Fig. 5.9 shows the capacitance percent variation vs the gate bias. Noticeably, below the threshold, the device is characterized by similar values of all capacitances, and their sensitivity towards each parameter is nearly the same. The WF sensitivity is roughly twice the DOP one, while LDE variations are negligible. Above the threshold, the drain-gate and gate-drain capacitances show markedly different behaviors: While C_{GD} sensitivity increases, the C_{DG} one roughly decreases, due to the fact that the charge in the drain depleted region tends to be "frozen" in saturated conditions, while at even higher gate bias, the spread due to the parasitic resistance is more significant.

5.3 Double-Fin FinFET variability analysis and Green's Function validity

AC performance of the device is heavily influenced by the fabrication of multiple FinFET devices together. In the previous section, we focused on the peculiar case of the SF FinFET device, stripped by pad oxides, for our analysis. Here, we focus on discussing the multifin FinFET, to have a more realistic view of FinFET AC performance. In multifin FinFETs, due to inter-fin capacitance, parasitics have higher influence on the device performance in comparison to the single-fin case. The capacitances in multifins, as compared to the single fin are expected to be higher, due to side-wall source and drain regions.

A double fin DG structure, 3D cross section is shown in Fig. 5.10, while, the cross-section in x-y plane shown in Fig. 5.11 was simulated in 2D for AC analysis. We will be manually (deterministic variations) varying: the fin width (WF), the gate/source(drain) distance (LDE) and the source/drain (S/D) doping (DOP), see Table. 5.1 for the exact definition and geometry. We will incorporate another important parameter fin separation hereafter (WS). Fin separation is the distance between the two fins fabricated together. This distance between the two fins should be carefully set to prevent inter fin coupling, which will deteriorate RF performance degradation.

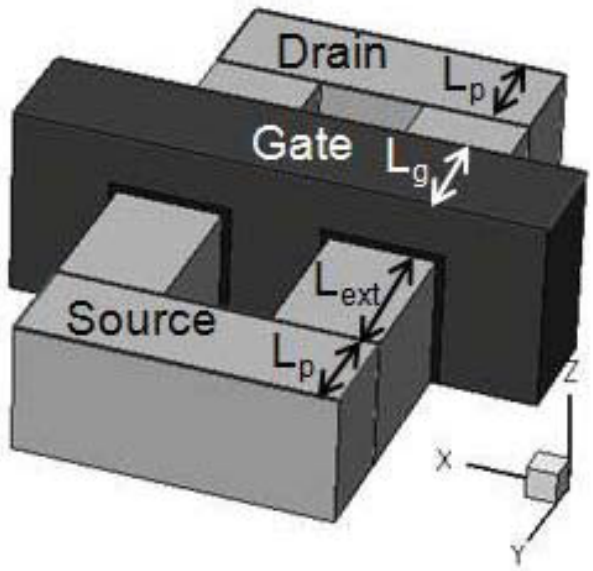

Figure 5.10: Double fin DG device (3D cross section) [43].

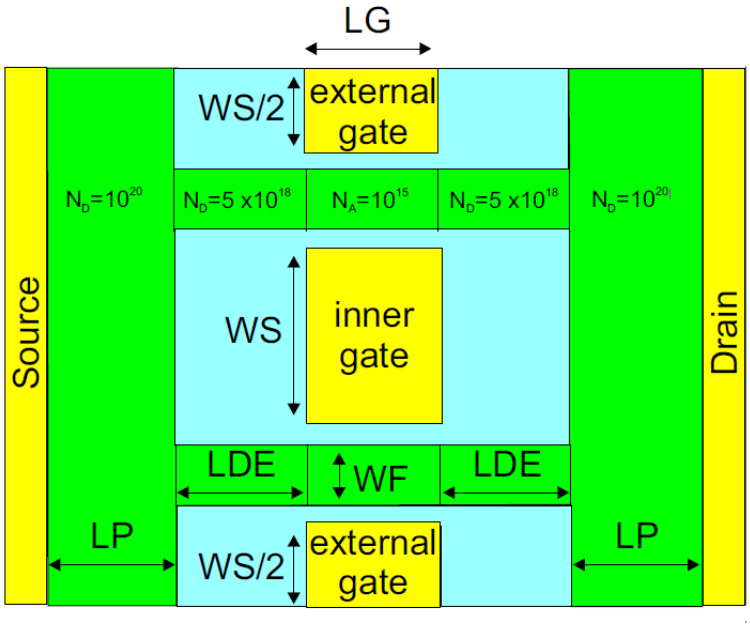

Figure 5.11: 2D cross section of multiFin DG FinFET structure and geometrical definitions. Green represents Si region, the light blue is SiO_2 and yellow represents ideal metal gate [8].

Table 5.2: Geometrical parameters for double fin DG FinFET device structure [8].

Parameter	**Dimensions (nm)**
Equivalent SiO_2 TOX	1
LG	54
LDE	54
WF	10
WS	36
LP	54

Turning to the variability analysis of the device in Fig. 5.11, globally capacitances of the double fin device are found to be higher than the ones of the stripped single fin case due to the sidewall source and drain regions. Comparing the total gate-gate and gate-drain capacitances of the multifin DG FinFET with the previous stripped device (scaled by an ideal factor of two), a rough estimate of 0.5 pF/mm for each side of the gate (source/drain) can be made: this amount adds to the drain-gate capacitance and double of it (source+drain) to the total gate-gate capacitance. While this is just a rough estimation found by comparison of the two devices and supported by trivial geometric scaling, the AC variability analysis from the physical simulator is exact in reproducing all parasitics, including edge and corner effects. In Fig. 5.12, we can observe, capacitive variations. It includes all fringing effects and their (possibly complicated) dependency on geometry. The same is true for variation analysis.

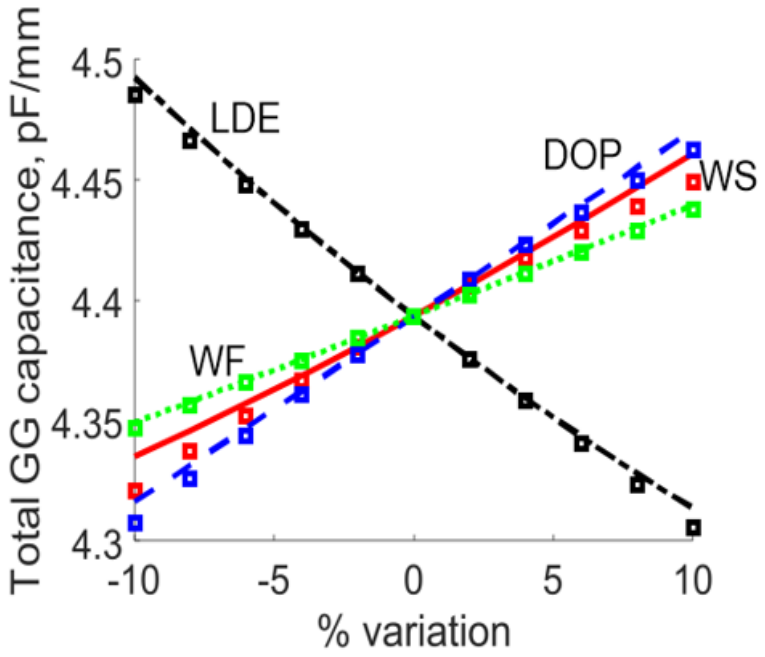

Figure 5.12: Gate-gate capacitance of the two fin DG device vs parameter variations.

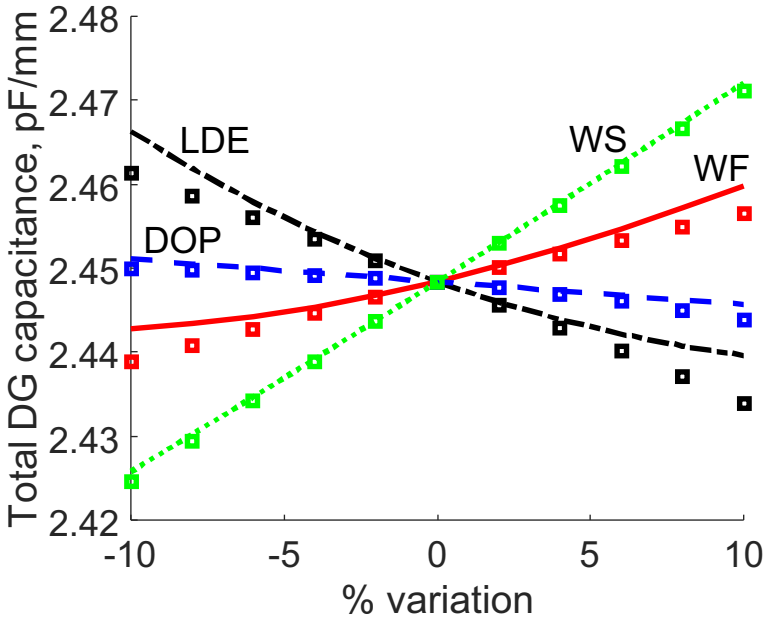

Figure 5.13: Drain-gate capacitance of the two fin DG device vs parameter variations [8].

Fig. 5.13, expresses the response of the drain-gate capacitances to the fin variations: unlike the case of the stripped device, it is evident that the two prominent parameters are fin separation and source-drain extensions in comparison to the single fin case.

Now, we will turn to variability response of real part of DG and DD element. Transconductance (drain-gate admittance) and output conductance (output conductance) are important parameters for device analog performance. From Fig. 5.14, we can see that transconductance is insensitive to fin separation. While, WF and DOP variations are more influential and around 5% variation in transconductance is observed for 10% parametric variation, also both WF and DOP follows the same trend, which again shows the dependency of transconductance on the parasitic resistances, i.e., increasing WF or DOP reduces parasitic resistances and the transconductance of the device increases. Opposite is true for the LDE, this is because increase in LDE results in the increase of parasitic resistance, therefore, transconductance decreases. It is also worth noting that the general trends for sensitivities is similar to SF FinFET.

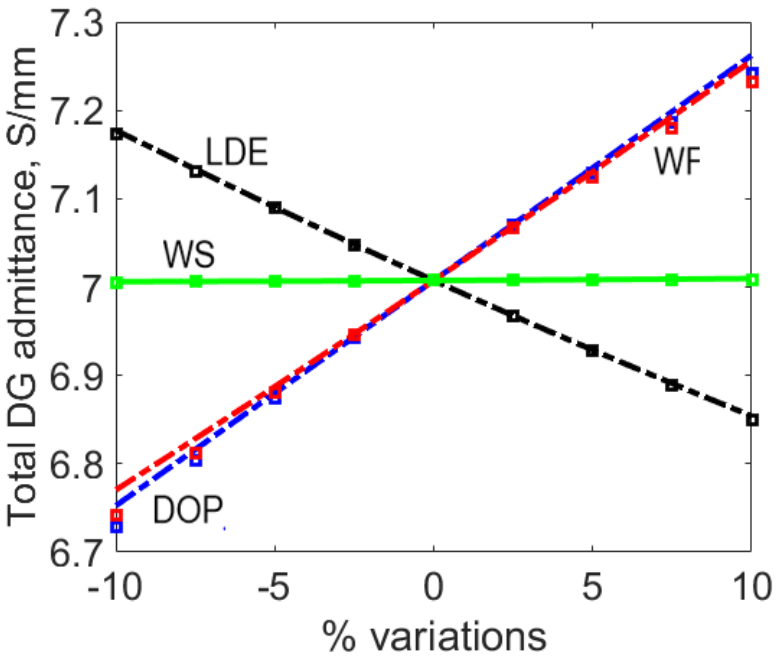

Figure 5.14: Drain-gate admittance of the two fin DG device vs parameter variations.

Now we turn to Fig. 5.15, which shows the sensitivity of output conductance to different parametric variations. We again see that DD element of admittance matrix is insensitive to WS. Generally, we have observed that the multifin structures improves the admittance matrix parameters but increases the overall capacitive

effects on the device. The general variability trend of all parameters is similar to real part of DG element. But, there is significant reduction in the magnitude of sensitivities to process parameters in comparison to the DG element. WF is the most dominant source of variation. The two opposite effects caused by DOP variations reduces the impact of DOP variation, i.e., increase in DOP reduces the parasitic resistances but increase the SCE effects (velocity saturation near drain side).

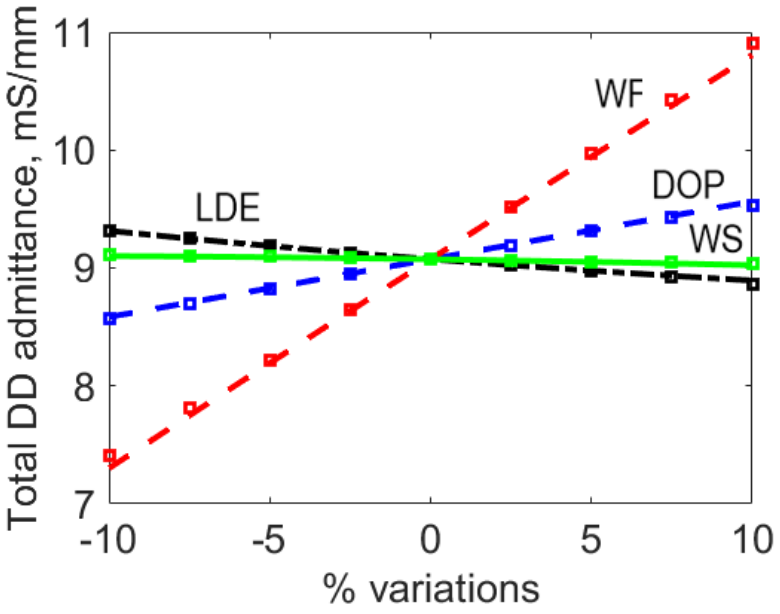

Figure 5.15: Drain-Drain admittance of the two fin DG device vs parameter variations.

Fig. 5.16 shows the cutoff frequency as a function of all parameters. Here the effect of WS is found to be close to that of WF and DOP, showing the complicated interconnection of the transconductance variations combined with the total gate capacitance, which increases with WF, WS and DOP and decreases with LDE.

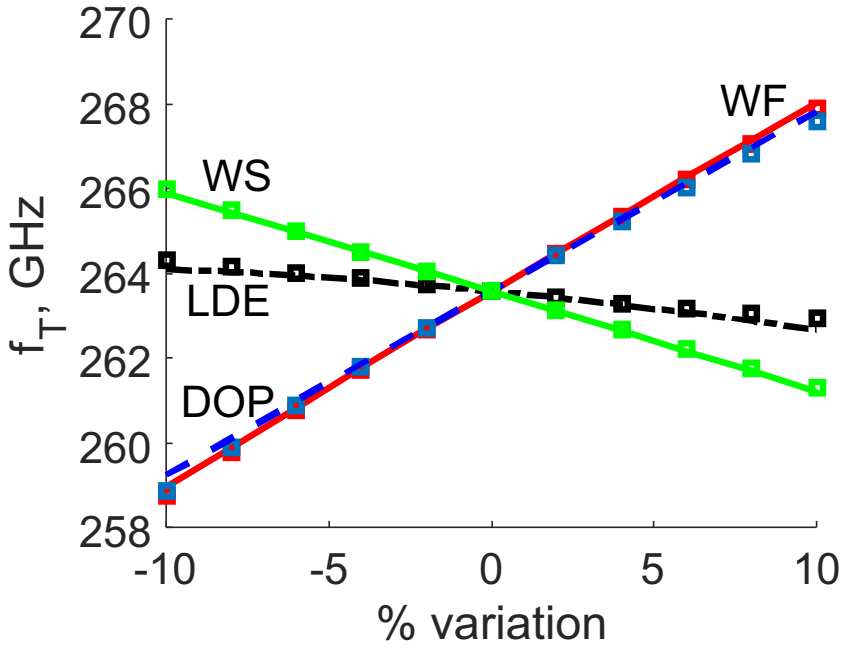

Figure 5.16: Cutoff frequency of the two fin DG device vs parameter variations [8].

Finally, if we compare the cutoff frequencies in both single fin and double fin case of DG FinFET. As expected, there is a significant reduction in the cutoff frequency: this is due to the significant increase in the gate-gate capacitances. The cutoff frequency for the case of device of Figs. 5.1 and 5.11 exposed to deterministic fin variations, is reducing by 60 GHz from single to double fin case, as can be seen in Fig. 5.17.

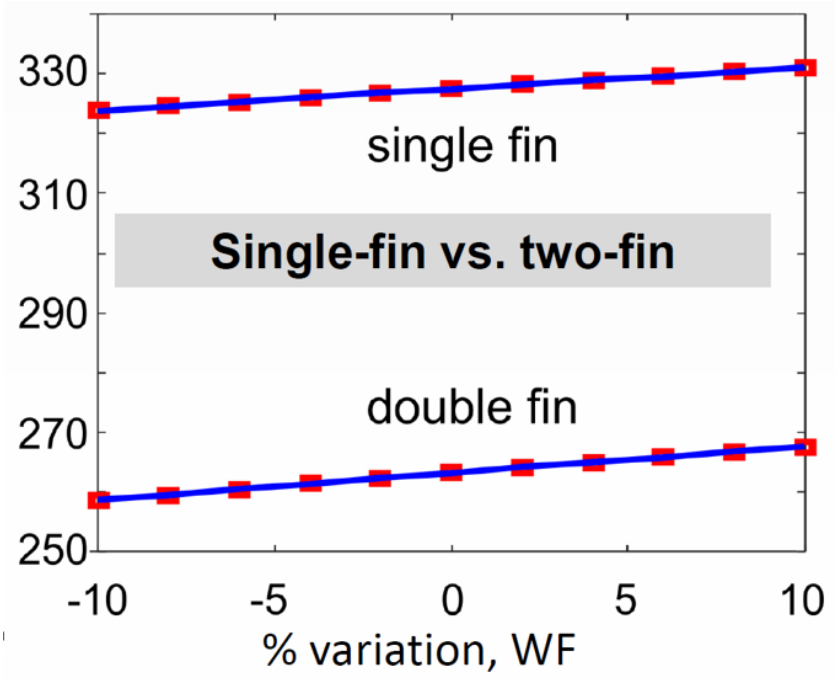

Figure 5.17: Comparison of Single Fin and Multi Fin FinFET's cutoff frequency w.r.t. Fin variations [125].

5.4 Summary

In this chapter, we focused on the application of GF approach to the AC sensitivity analysis. Studying, the AC performance of the single fin FinFET and double fin FinFET, we can conclude the dependence of device performance on the parasitic capacitances and resistances. We studied the effects of parametric variations on the parasitics and how they are degrading the most relevant RF figure of merits.

The single fin FinFET is stripped by pad oxides and hence doesn't include effects of many capacitances(like interfin capacitances). For AC analysis of double fin FinFET, we also studied the effect of fin separation variations and found it to be one of the dominant parameter affecting the AC performance of the device. The overall capacitances are found to be higher than the stripped single fin, due to the sidewall source and drain regions. Further, in the double fin case, it is evident that the two prominent parameters are fin separation and source-drain extensions in comparison to the single fin case. So we can conclude that due to inter-fin capacitance, parasitics have higher influence on the device performance of multifin FinFETs in comparison to the single-fin case.

We also found GF to be more numerically efficient than the conventional approaches. The overall simulation time for the FinFET ($\backsim$ 5700 nodes) analysis,

including 8 bias points and WF, DOP and LDE sampled over 11 values, is approximately 1 hour for a single frequency on a PC with 8 GB RAM and 2.9 GHz processor. The GF approach allows for a saving in simulation time around 5% to 10% with respect to the incremental simulations.

In the next chapter, we will turn our focus to the peculiar feature of our in-house simulator, which enables us to understand, study and pinpoint the regions of the device more sensitive to process variations.

Chapter 6

The Local Variability Source and its application to SF DG

In the previous chapter, we focused on the validation of GF and its application on the single and double fin FinFET. AC analysis of single fin FinFET was also performed in the previous chapter. In continuation to previous analysis, we will extend our AC investigation in single fin FinFET, with respect to the device region's sensitivity using *GF* and *LVS* techniques.

In this chapter, we will discuss the unique feature of GFs, which enables microscopic analysis of the device regions' most sensitive to the parameter variations. This capability of GF approach enables the identification of the parts of the device which contributes most to AC parameter variations. GF analysis is based on the convolution integral shown in Eq. 4.34, whose integrand function will be referred to as the LVS: such function ultimately provides the microscopic insight into the device regions most sensitive to parameter variations. These LVS are the product of CGF G_α and local variations s_α (α can be Poisson or hole/ electron continuity equation). Hence, we also discuss the behavior of GFs independently before turning to LVS. For geometric variations, s_α also depends on the mesh, remeshing of the mesh is required. So, we focus on the DOP variations which is relatively simple in comparison to geometric variations, since affect primarily Poisson equation only. For the understanding of FinFET device sensitivity, we consider the structure shown in Fig. 6.1.

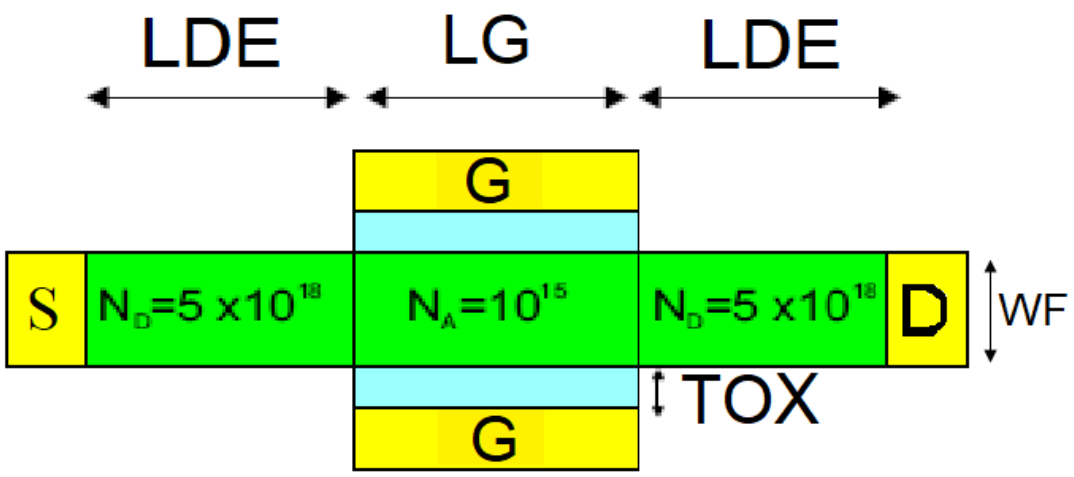

Figure 6.1: Single Fin FinFET Structure [124]

Similar structure was used for the SF DG device for AC analysis. The dimensions of the device are shown in Table. 5.1.

6.1 Green Functions for Doping Variations

Starting from the analysis of the GFs, we focus attention on the (1,0) element of the Poisson equation CGF, relating the DC parameter variations to the AC terminal current variations. In-fact, these are the ones used for the calculation of the LVS for doping variations. For doping variations s_α corresponds to a variation of charge density in the Poisson equation, hence $\alpha \cong \psi$. Doping variations are DC, hence the (1,0) element relates DC variations of doping to AC variations of terminal currents.

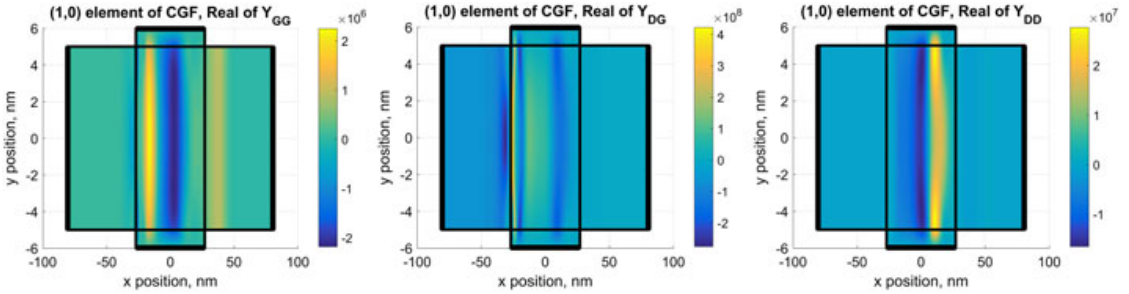

Figure 6.2: Real parts of the (1,0) element of the conversion Green's function (CGF) for the Poisson equation (A/cm). (1,0) elements relate DC parameter variations to AC terminal current variations. Frequency is 60 GHz [124]

Fig. 6.2 shows the real part of the (1,0) Poisson CGFs, for various elements of the Y matrix and bias $V_{GS} = 0.6$ V. Since we have always considered a symmetric gate bias condition, all CGF turn out to be symmetric along the y axis with respect to the midfin cross section. First, we notice that the CGF for Y_{DG} (Fig. 6.2, middle) dominates over the other components, showing a high sensitivity in the region between the gates. Peaks are present in the depleted region, where the variations of the Poisson equation make the local charge to vary abruptly. The peak is broader at the drain, encompassing part of the velocity saturated area. Concerning the dependency along y, it is especially high (in absolute value) in the bulk region, i.e., along the midfin area. Notice that Poisson GFs is not limited to the silicon region, but extends also in the oxides, hence allowing, besides doping variations, for the investigation of oxide geometry or permittivity variations, not considered here. The GF for the output conductance (Fig. 6.2, right) shows a similar behavior, although the peak at the source junction is negligible. Finally, the real part of the gate-gate admittance is negligible.

Turning to imaginary parts, see Fig. 6.3, the depleted region at the source dominates the gate capacitance (left), while the drain capacitances are most sensitive in the drain region near the channel(right). The drain-gate element (middle) has the highest sensitivity in the channel region between the 2 gates.

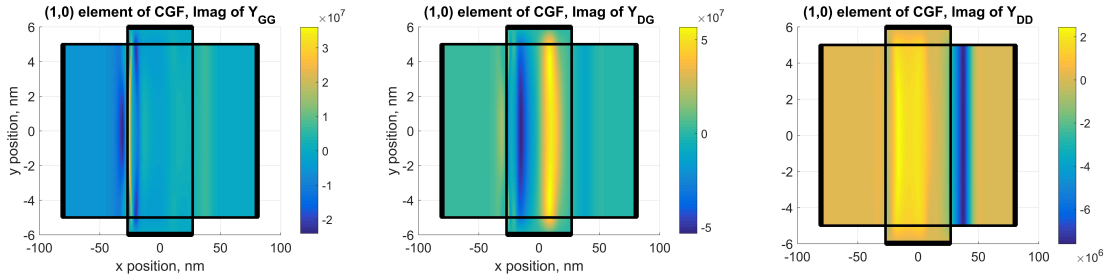

Figure 6.3: Imaginary parts of the (1,0) element of the CGF for the Poisson equation (A/cm). (1,0) elements relate DC parameter variations to AC terminal current variations. Frequency is 60 GHz[124].

To better compare the various components, the midfin cross sections of these 3 CGFs are compared in Fig. 6.4. Notice that, while the highest variation is in the channel region, a significant plateau is also present for the Y_{DG} element in the source parasitic region, i.e., $-32 \leqslant x \leqslant -22$, thus confirming that in this bias conditions, doping variations in the source extension play a significant role. Notice, though, that the same is not present in the drain region, where the velocity is saturated. Therefore, the sensitivity to source extension doping is expected to dominate the parasitic resistance. The midfin cross sections, Fig. 6.4, left, shows the significant plateau for the DG element. This is due to the fact that doping variation of 5% resulted in the decrease of parasitic resistance, which results in

an increase of transconductance, that is why we see the significant dependence of transconductance on doping variations, while the other two element, i.e., DD and GG, are less influential due to the increase in SCE, which compensates the impact of reduced parasitic resistances. Fig. 6.4, right, show that the drain region is insensitive to DOP variations, while we also notice a significant plateau in the source extension, corresponding to the effect of the source parasitic resistance on the Y matrix imaginary parts. Such effect is negligible only for the output capacitance (red dotted line). Overall, from GF analysis on the device region, we found that the region near the source and channel junction is more sensitive to the DOP variations for both real and imaginary parts of drain-gate element.

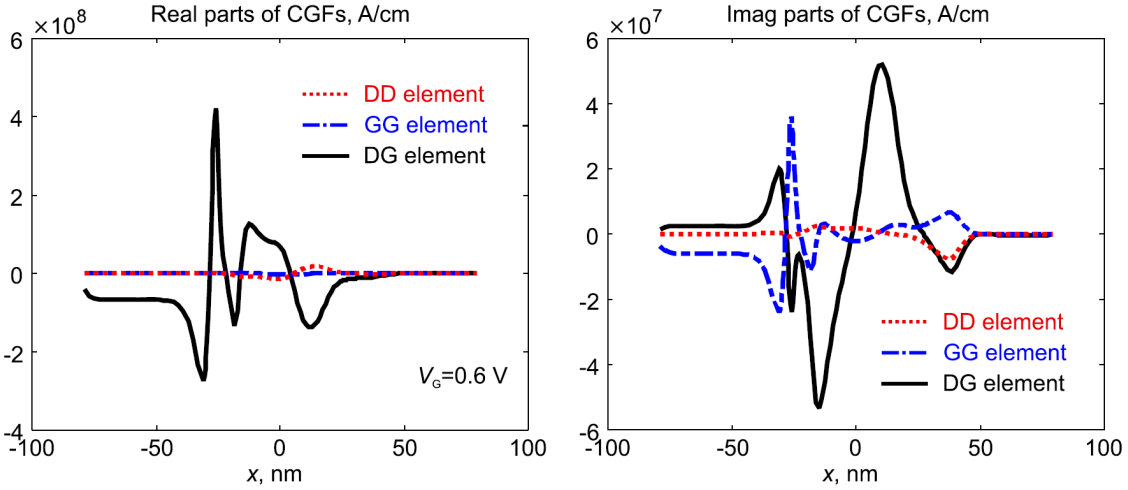

Figure 6.4: Midfin cross sections of some (1,0) elements of the conversion Green's function (CGF) for the Poisson equation (A/cm). Frequency is 60 GHz [124].

6.2 LVS and its insight on internal device sensitivity

We now turn to LVS, which is integrand of Eq. 4.34. LVS provide a more direct insight for DOP variations, which in particular affect Poisson equation via the total charge. Here, we present selected results concerning the effect of 5% (positive) S/D DOP variations. The overall behavior on the drain-gate element of the Y matrix is presented in Fig. 6.5. Notice that the doping is varied only in the extensions so that the LVS is identically null in the regions between the 2 gates. The cross sections for the real (left) and imaginary (right) parts show that the main contributions come from the source, while peaks are present in the doped regions overlapping the gates, due to the variations of the depleted region charge.

To better highlight the importance of the LVS analysis, Fig. 6.6 shows the midfin

cross sections of the LVS for admittance and capacitance parameters at various bias conditions. Here, the S/D DOP variation is again fixed to 5%. Notice that the drain-gate admittance sensitivity is dominated by the source extension, increasing significantly with bias. On the contrary, the output conductance is less dependent on the source doping and is concentrated in the drain depleted region. This region broadens slightly with increasing gate voltage, yielding a mild bias dependency. The imaginary parts, represented in the same Fig. 6.6, left, show interesting behaviors. First of all, notice that below threshold all capacitances show exactly the same sensitivity in the drain region, while only the gate capacitance (red dotted curves in Fig. 6.6, right) is affected by the source junction charge. With increasing bias, the gate-drain capacitance is nearly unchanged, showing lowest sensitivity to doping variations, and always limited to the drain depleted region, while the drain-gate and gate-gate capacitance sensitivity increases: noticeably, they remain correlated in the drain region, while in the source extension, the sensitivity of the gate capacitance is higher and increases significantly with the gate bias. These results suggest that the sensitivity of the drain-gate capacitance is lower than the gate-gate one.

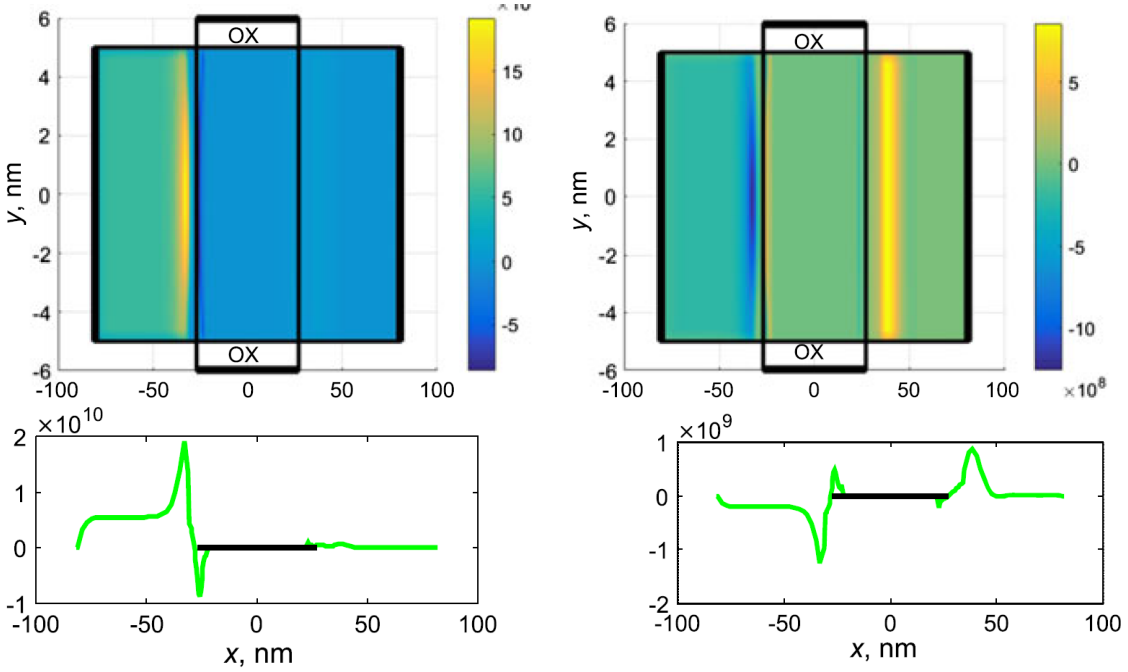

Figure 6.5: LVS for the drain-gate element of the Y matrix. Left: real part (admittance); right: imaginary part (capacitance). The cross sections represent the midfin behavior. Black lines show the position of the gate contacts. The LVS is non null in the extensions and in 5 nm of overlap region under the gate. Frequency is 60 GHz [124].

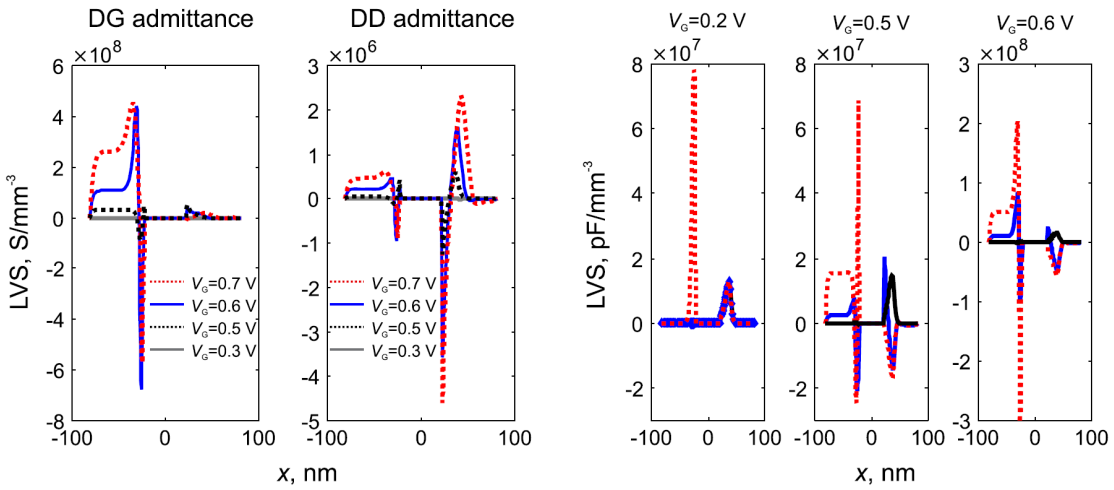

Figure 6.6: Midfin cross sections of some (1,0) elements of the LVS for S/D doping variations, showing regions where the variations are correlated. Red dashed lines: LVS for the gate-gate capacitance; blue lines: LVS for the drain-gate capacitance; black lines: LVS for the gate-drain capacitance. Frequency is 60 GHz [124].

To better understand the LVS ability to provide device insights, we are reporting the drain-gate element of Y matrix for double fin FinFET.

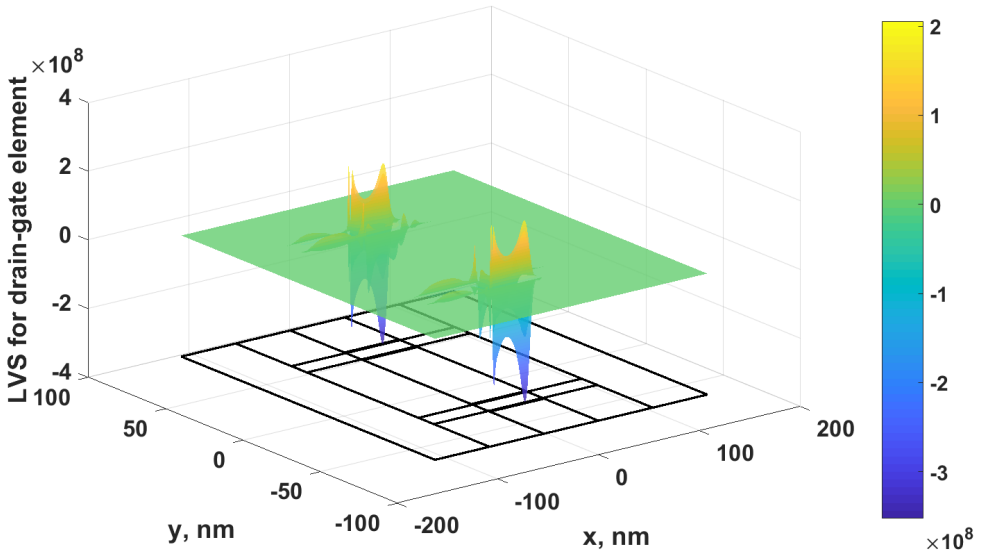

Figure 6.7: LVS for drain-gate element of Y-matrix for double fin FinFET.

In Fig. 6.8, we presented the zoomed view of two fins and interestingly, we observed that the two fins are not symmetrical. Although, the two fins are completely symmetrical geometrically and the gate contacts are ideal as well. While in

SF case, see Fig. 6.5, we can see the complete symmetrical behavior of two gates. This unwanted imbalance between the two gates can deteriorate the performance of the FinFET. It must be noted that in IG FinFETs, we intentionally apply different bias at gate terminals which is used to exploit backgating effect to tune the threshold voltage. Corner effects and sidewall capacitances can be the possible cause of the imbalanced between the two gates. This effect must be carefully studied, when fabricating multifin FinFET structures.

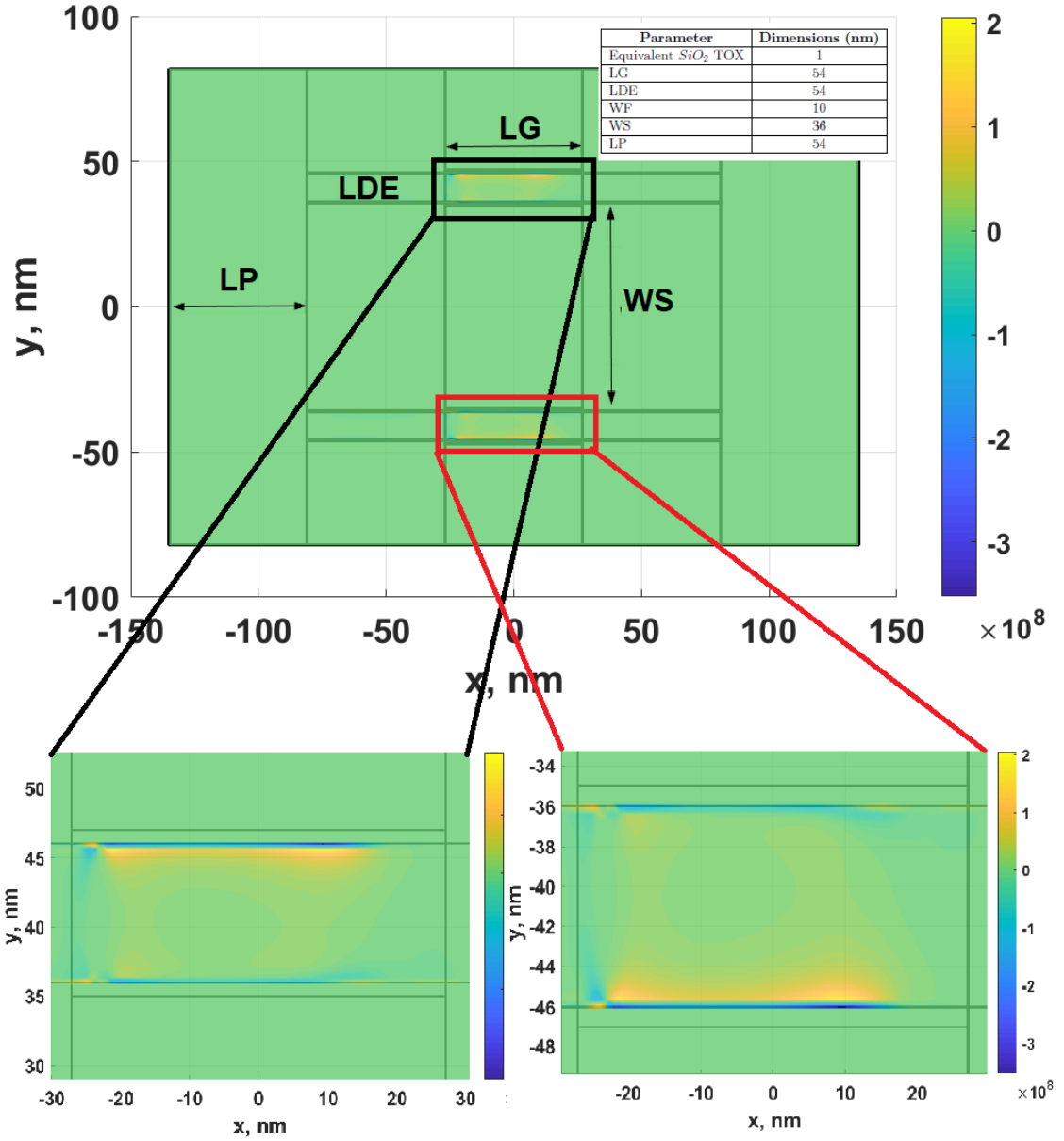

Figure 6.8: Zoomed LVS view of fin for drain-gate element of Y-matrix for double fin FinFET.

The GF approach yields a deep insight into the regions of the device most sensitive to the variations: In this section, both the GFs and the LVSs have been investigated and discussed. Apart from the depleted regions, the main source of variability is uniformly distributed in the source extension both for the drain-gate and gate-gate elements, while the drain extension is the region where variations of the feedback capacitance arise.

6.3 Summary

In this chapter, we extended our work about SF FinFET from previous chapter, discussing very unique physical insight of the device by the help GF based technique, which allows for a deeper understanding of the physical origin of variations, i.e., the regions of the device most sensitive to the uncertainty of various process variations (sources of variations). The variation of the Y matrix elements is presented as a function of the fin width, drain extension length, and source/drain doping. To achieve true understanding of the sources of variations, the behavior of the GFs and of the LVSs inside the device are also presented in this chapter. Apart form the depleted regions, the main source of variability is uniformly distributed in the source extension both for the drain-gate and gate-gate capacitive elements, especially below the threshold.

This analysis allows for a wide range of extensions and applications, including 3D and multifin device analysis at various bias condition, e.g., including the case of independently driven gates.

In the next chapter, we will turn our focus to IG DG FinFET, and will perform the sensitivity analysis on the AC parameters.

Chapter 7

Independent Gate DG FinFET simulation and senstivity Analysis

In this chapter, we will focus on a different variant of FinFET, i.e., the IG FinFET. In Chapter 5, we were focused on the AC analysis of SG FinFET and it's response to the process variations, while in this chapter, the focus will be on IG DG FinFET and its response to variability. We will also introduce the concept of *sensitivity charts* and its application on the IG FinFET.

7.1 Independent Gate FinFET

In independent gate structures, the two gates are not physically connected by the same metalization, but are kept apart [126]. Hence, the two gates are considered independent contacts, hereafter denoted G1 and G2, see Fig. 7.1. This characterization can be exploited to implement circuits with fewer transistors, e.g., G2 can be used as input, instead of an additional MOSFET, to reduce the number of transistors needed to implement different logic functions. The independent handling of the gates enables the designer to enhance the performance of a front gate G1, i.e., if the device is in ON condition: the back gate G2 can be tuned to increase the drive current or, if the device is in OFF state, the back gate G2 can be tuned to increase threshold voltage, hence reducing the leakage current.

We performed AC simulations on single fin DG FinFET with independent gates and as in chapter 5, compare the GF with the incremental approach for validation. We will also compare the IG and SG cases to better understand the peculiarity of the AC performance of IG based FinFETs in response to the process variations.

We simulate the structure shown in Fig. 7.1 whose geometries are similar to the one defined in Table. 7.1.

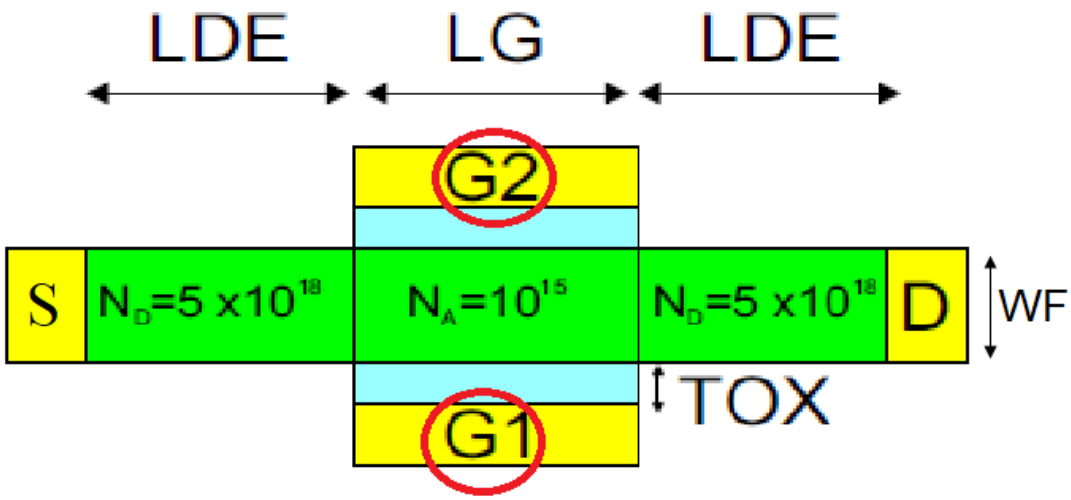

Figure 7.1: Single fin DG FinFET structure highlighting the two gate terminals. Green represents Si region, the light blue is SiO_2 and yellow represents ideal metal gate [127, 33].

Table 7.1: Geometrical Parameters for IG FinFET device structure [33].

Parameter	**Dimensions (nm)**
Equivalent SiO_2 TOX	1
LG	54
LDE	54
WF	10

When reporting the results hereafter, solid lines represents the GF simulations of the SG FinFET and circle symbol represent the incremental simulations for SG FinFET. For the IG case, we consider first slight unbalance between the two gate voltages, while maintaining a similar overall drain current in both the SG and IG cases. In such a way, we can focus the attention on the mere effect of the unbalance of the two gates, while the drain DC current is kept unchanged. We chose the gate voltages as: V_{GS} = 0.65 V and will be hereafter denoted as the Higher voltage Gate (GH), whereas the other gate has V_{GS} = 0.55 V and will be denoted as the Lower-voltage Gate (GL). The bias conditions for SG case are similar to ones discussed in chapter 5, i.e., V_{GS}= 0.6 V. The color representation for variations are similar to the ones discussed in chapter 5, i.e., Black: LDE , Blue: DOP and Red: WF. The corresponding symbol representation for IG case will defined with the plots. GL and GH for the GF simulations are represented as: dashed lines and dashed-dot lines respectively. Similarly, for the incremental analysis, GL and GH are represented by symbols (diamonds and triangles respectively).

From Fig. 7.2, we can see the DG element of Y matrix and the response to different parametric variations for SG and IG case. We have already discussed the transconductance response to SG in chapter 5 and as expected, we find nearly same tracking for the WF and the DOP case for all cases. The trend for LDE is opposite to other variations as expected. Notice that the transconductance for the IG case is dissimilar for (D,GH) and (D,GL) elements. The difference in transconductance contribution shows its bias dependency. We obviously notice that the lower the gate bias, the lower the transconductance. Despite the absolute value is different, variations are not strongly affected by bias, since the slope of the curves is practically constant: in fact curves corresponding to each parameter variation are roughly parallel both in the IG and SG case; only a slight decrease in the sensitivity is observed in the (D,GL) element as a function of DOP and WF suggesting a bias dependency.

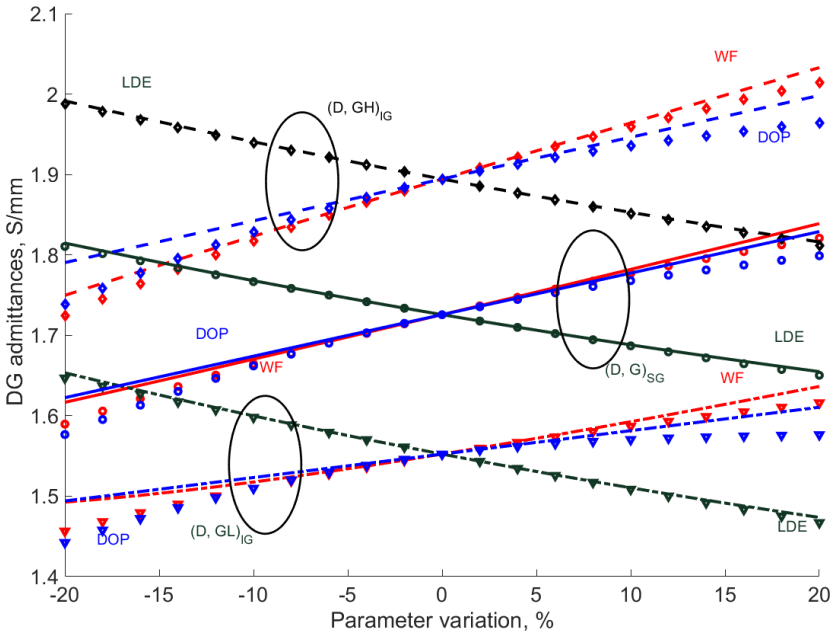

Figure 7.2: Drain-Gate (DG) admittance element of the Y matrix in response to % parameter variations (black: LDE; red: WF; blue: DOP).Element $(DG)_{SG}$ in SG bias: solid lines (GF) and circles (incremental). Element $(D,GL)_{IG}$ in IG bias: dashed lines (GF) and diamonds (incremental). Element $(D,GH)_{IG}$ in IG bias: dash-dot lines (GF) and triangles (incremental) [127].

Fig. 7.3 depicts the sensitivities to process variations of the DG capacitance. The corresponding magnitude of DG capacitance for both (D,GH) and (D,GL) elements is different, thus, showing the bias dependency. Contrary to the previous case, though, the (D,GH) element exhibits a stronger sensitivity towards parameter variations with respect to the (D,GL) element, and similar to the SG case.

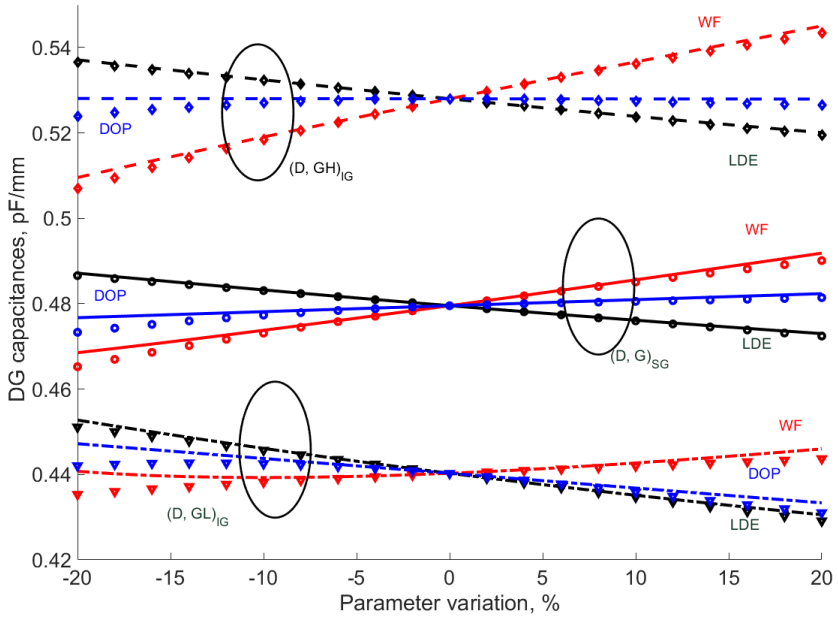

Figure 7.3: Drain-Gate (DG) capacitive element of the Y matrix in response to % parameter variations (black: LDE; red: WF; blue: DOP).Element $(DG)_{SG}$ in SG bias: solid lines (GF) and circles (incremental). Element $(D, GL)_{IG}$ in IG bias: dashed lines (GF) and diamonds (incremental). Element $(D, GH)_{IG}$ in IG bias: dash-dot lines (GF) and triangles (incremental) [127].

From the plot in Fig. 7.4, we can see that drain admittances are not changing with the change in bias and IG and SG exhibits more or less the same trend in response to parametric variations, which shows that drain admittances are independent of the gate biases and are dominated by parasitic elements rather than the gate biases.

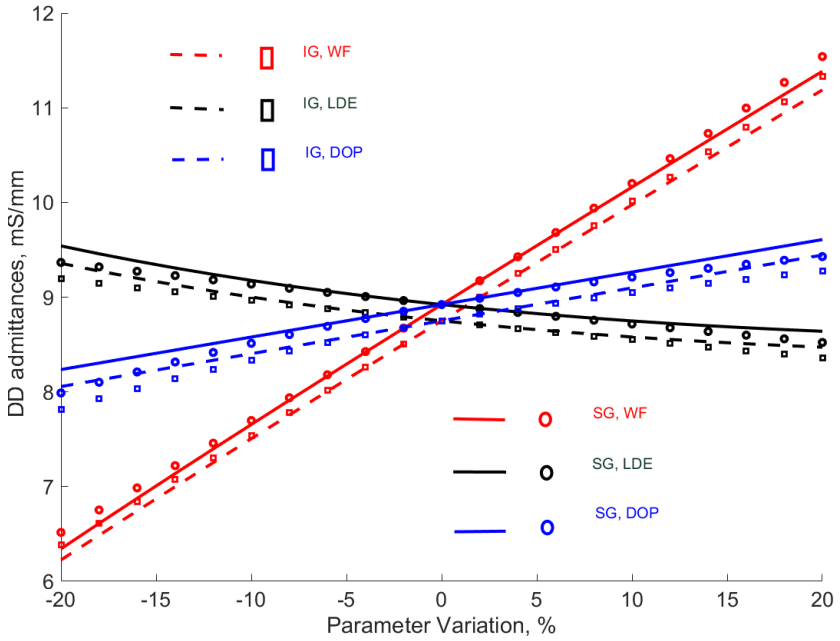

Figure 7.4: Drain-Drain (DD) admittance in response to % parameter variations (black: LDE; red: WF; blue: DOP) [127].

Now, we will discuss the gate capacitances for both the devices. Fig. 7.5 shows the diagonal capacitive elements, i.e., for SG case (G,G) and for IG case (GL,GL) and (GH,GH). The response to parameter variations is complicated. Sensitivity to LDE is same for all cases. While for WF variations, we observed different response for (GL,GL) and (GH,GH) elements and both of these elements are different to gate-gate capacitances of the SG case. Variations with respect to DOP are similar for the (GH,GH) element in the IG case and (G,G) element in the SG case, while (GL,GL) differs. These results also show the bias dependency of gate-gate capacitances.

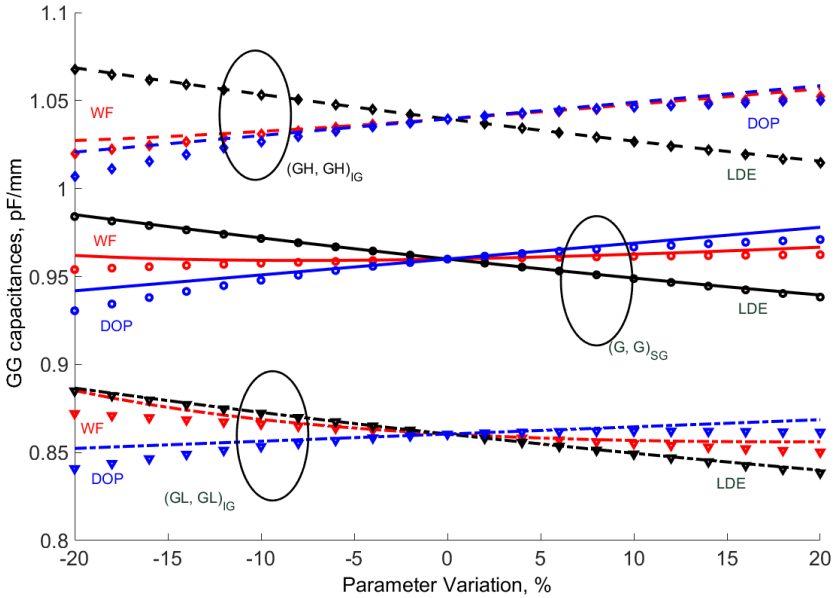

Figure 7.5: Diagonal element of the Gate-Gate (GG) capacitances in response to % parameter variations (black: LDE; red: WF; blue: DOP). Element $(GG)_{SG}$ in SG bias condition: solid lines (GF) and circles (incremental). Element $(GL, GL)_{IG}$ in IG bias: dashed lines (GF) and diamonds (incremental). Element $(GH, GH)_{IG}$ in IG bias: dash-dot lines (GF) and triangles (incremental) [127].

To present the clearer picture and a better idea about the complex behavior of the diagonal elements of the gate-gate capacitances, we present in Fig. 7.6, the percentage variation in GG capacitance with the individual parameters. If we look at the left most side of Fig. 7.6, we can see high percent sensitivity to lower gate bias, i.e., $(GL, GL)_{IG}$ element has higher sensitivity to parameter variations in comparison to the gate terminal with higher bias. While the LDE, as discussed above have similar sensitivity in all the three cases.

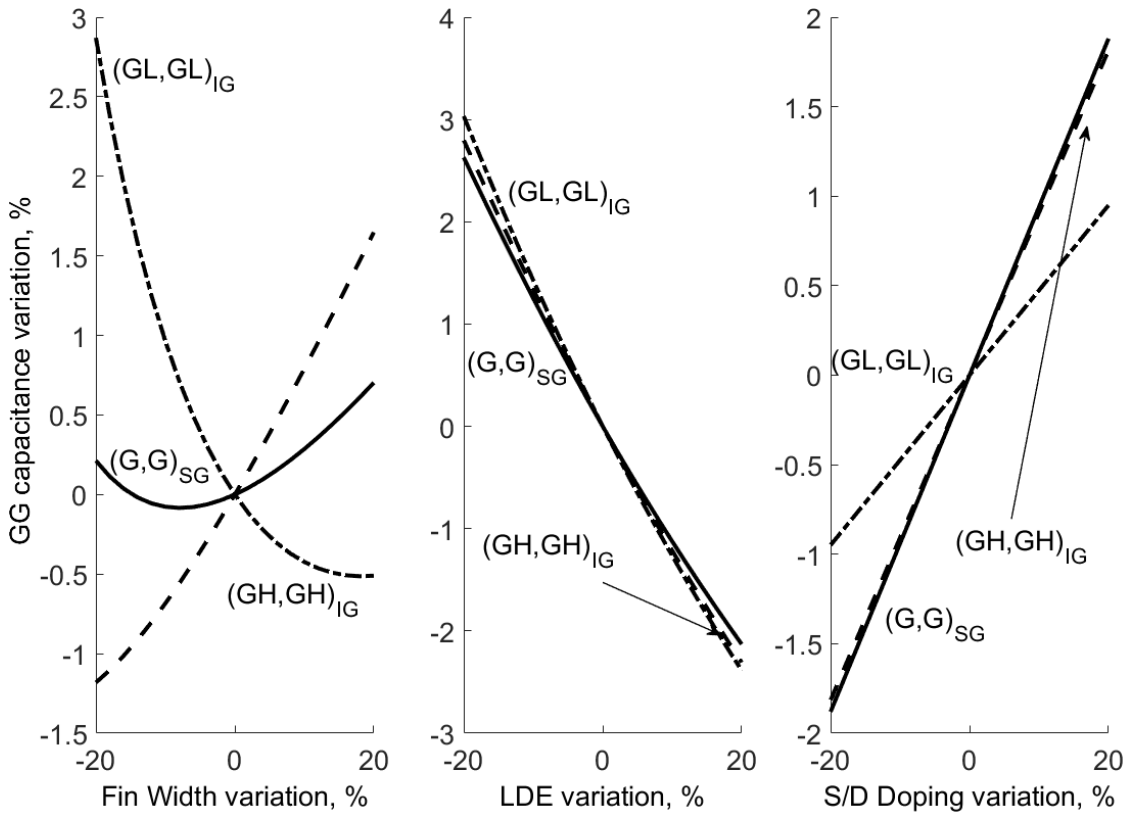

Figure 7.6: Percentage variations of the diagonal GG capacitances. Left: WF variations; middle: LDE variations; right: DOP variations. Solid lines $(G,G)_{SG}$; dashed lines $(GH,GH)_{IG}$; dash-dot lines; $(GL,GL)_{IG}$ [127].

It is important to notice that in independent gate cse an extra term of the Y matrix is represented by the mutual gate capacitances between the GL and GH contact. This element also plays a significant role, affecting the feedback capacitances of RF stages. Fig. 7.7 shows the sensitivity of such parameters. The off-diagonal capacitances are lower in magnitude in comparison to the diagonal gate-gate capacitances, but they are more sensitive to variations, i.e., they are varying from 20-50% of their nominal value with respect to process variations. So, it can be concluded that the designers of RF analog stages using IG FinFETs should be careful and keep the variation in mutual capacitances in check.

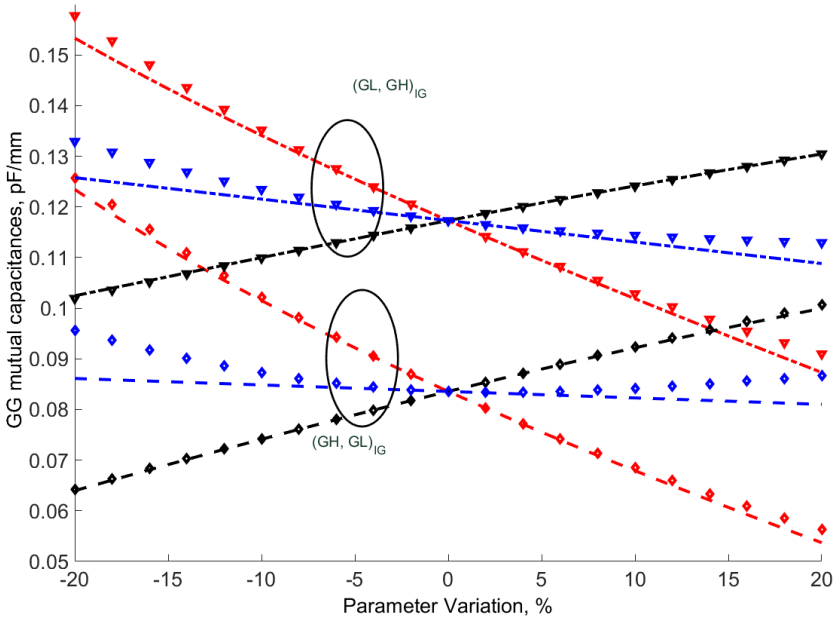

Figure 7.7: Off-diagonal elements of the GG capacitances in the IG case as a function of parameter variations (black: LDE; red: WF; blue: DOP). Element $((GH, GL)_{IG}$: dashed lines (GF) and diamonds (incremental). Element $(GL, GH)_{IG}$: dash-dot lines (GF) and triangles (incremental) [127].

The analysis carried out so far, enlightens the fact that parameters such as Drain-Drain admittances are immune to change in bias at terminals and are more susceptible to parasitics of the device. Other parameters, such as, diagonal GG elements show strong dependency on bias conditions. The transconductance may be more sensitive to gate oxide variations in the IG case, and this parameter is also influenced by the biasing voltage. In IG case, gate mutual capacitances have sensitivity of around 20-50% parameter variations. The GF approach shows a great amount of accuracy upto 20% of variations and also for this case simulation time is reduced by 95%, in comparison to the incremental approach.

7.2 RF Sensitivity Analysis using Sensitivity Charts

After developing the background of RF variability in both IG and SG cases, in this section, we will introduce the concept of *sensitivity charts*. As, we have seen in the previous section, comparing results for different devices, structures and bias may become cumbersome, therefore, calling for a flexible tool for a global assessment of device variability. We will present *sensitivity charts* as a flexible tool to provide a global view of the device sensitivity in response to the variations in process parameters. *Sensitivity charts* enables the designer to directly compare the

relative importance of different variability sources. It also allows the link from the stand-alone device uncertainties to the circuit parameter spread and may be helpful in the identification of compact device sensitivity models.

7.2.1 Concept of Sensitivity Charts

The variations in the Y matrix with respect to the parametric variations have been already developed in this thesis. The parameter variations influence the $Y_{i,j}$ matrix elements, thus degrading the performance of device and these two parameters can easily be related with the help of *relative sensitivities*. These *relative sensitivities* enables the direct comparison of both P and $Y_{i,j}$. More precisely the *relative sensitivities* $S_{Y_{i,j}}$ of the $Y_{i,j}$ with respect to the variations of the parameter P, is defined as:

$$S_{Y_{i,j}} = \frac{\partial Y_{i,j}}{\partial P}.\frac{P_0}{Y_{0_{i,j}}} \approx \frac{\frac{\delta Y_{i,j}.100}{Y_{0_{i,j}}}}{\frac{\delta P.100}{P_0}} \tag{7.1}$$

where $Y_{i,j}$ is the *(i,j)*-th element of the AC admittance matrix. Without the influence of parameter variations, i.e., P_0, $Y_{i,j}$ will be $Y_{0_{i,j}}$. We can see from equation 7.1, that the relative sensitivities of the device can be expressed in terms of percent variations in the Y parameters in response to the percent variations in the process parameters P. The advantage of $S_{Y_{i,j}}$ is that being a relative value, it can be compared to other variations directly. Furthermore, $S_{Y_{i,j}}$ can be plotted as a function of device bias, yielding sensitivity charts and maps, that can be directly used in circuit design. Notice also that in the general case of a polynomial dependency $Y_{i,j} = kP^{\alpha}$, straightforward algebra from 7.1 yields $S_{Y_{i,j}} = \alpha$. Hence, sensitivities can also help in the identification of compact sensitivity models.

7.2.2 Sensitivity chart analysis of IG DG FinFET

After understanding the concept of sensitivity charts and their capability of providing the direct comparison of percent variations in both P and $Y_{i,j}$. We will turn our focus on extraction of the sensitivity charts.

Here in this section, we will use the similar structure and geometries discussed above in Fig. 5.1 and Table. 5.1. For our analysis, we now take WF, LDE, DOP, the gate length (LG) and the thickness of the front (OX1) and back (OX2) gate oxides, separately.

The front gate bias $V_{G1,S}$ has been varied from OFF state to full inversion of the front channel, i.e., from 0 to 1 V. The back-gate bias VG2 varies from = 0.2 V to -0.4 V: in fact, to avoid accumulation state,the VG2 values lower than -0.4 are avoided, while values higher than 0.2 V would drive the back channel in inversion state. Both these device states are avoided to exploit the VG2 for back-gating

effects only. To keep the device in saturation, 1 V at drain voltage is applied and the frequency is set to 60 GHz.

In Fig. 7.8, FinFET's drain current and transconductance (real part of $Y_{D,G1}$) in response to bias variations at back gate terminals are shown. We notice from the results that the threshold voltage is varying from 0.4 to 0.6 V, which is also inline with an approximated estimation through the theoretical expression in [128]:

$$\Delta V_{th} = -r\Delta V_{G2,S}; r \approx \frac{\frac{\epsilon_{Si}}{\epsilon_{OX}} OX1}{\frac{\epsilon_{Si}}{\epsilon_{OX}} OX2 + WF} \approx \frac{3}{13} \tag{7.2}$$

where $\frac{\epsilon_{Si}}{\epsilon_{OX}} \approx 3$ (OX1 and OX2 are here equivalent oxide thickness for SiO_2, definte high K dielectrics are used for silicon).

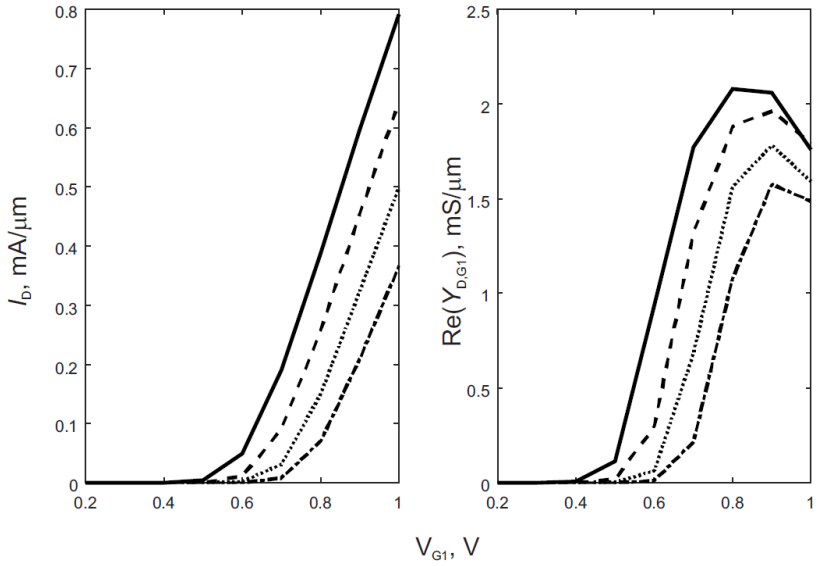

Figure 7.8: Drain current and transconductance versus V_{G1}. Solid: VG2 = 0.2 V. Dash: VG2 = 0: V. Dot: VG2 = -0.2 V. Dash-Dot: VG2 = -0.4 V. [33]

If we look at Fig. 7.9, as a general trend we can observe higher sensitivities near the threshold voltage. If we look at the plot, we can see a higher magnitude of percent sensitivity between 0.4 to 0.6 V. As it is in the case of the middle plot of Fig. 7.9. WF sensitivity is very strong in comparison to the other parameters. We can also observe that as the VG2 is decreasing, the sensitivity to VG1 bias is increasing. Overall for LG/DOP and LDE we can conclude that they are very less important in comparison to the other parameters.Also, we can clearly observe higher OX1 sensitivities and the highest sensitivity is near the threshold voltage. Larger OX1 will result in lower gate capacitances and the drain current will be reduced too, which can be seen here by negative OX1 sensitivities. While, if the OX2 will increase, it will reduce the back gating effect, hence the transconductance

will increase which can be seen by positive sensitivities. While on the right side of Fig. 7.9, for both parameters, we can see sensitivities are not very effective below the threshold, while above threshold, sensitivities are more relevant and increase in VG1, which may be due to the combined effect of parasitics and SCE. Further, no dispersion of the variations is the key feature when the parameter is insensitive to VG2, i.e., backgating.

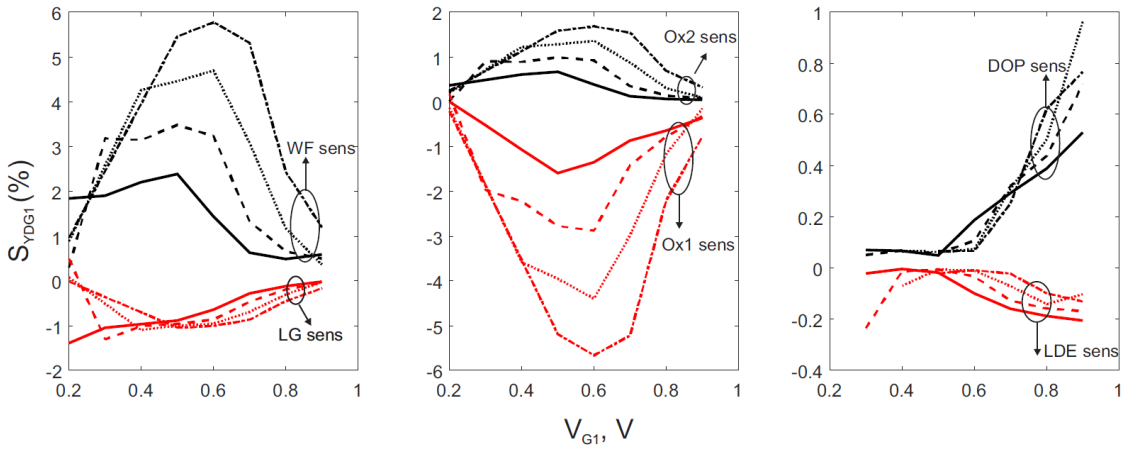

Figure 7.9: Sensitivity chart of the real part of the (D,G1) element of the admittance matrix. The percentage variation of $Y_{D,G1}$ corresponding to a unit (positive) percentage variation of each parameter P is plotted against gate bias. Solid: VG2 = 0.2 V. Dash: VG2 = 0 V. Dot: VG2 = -0.2 V. Dash-Dot: VG2 = -0.4 V. [33]

The sensitivity chart for the real part of the DD element of Y matrix, related to the output conductance of the device, is reported. We can observe the higher sensitivities for fin variations from Fig. 7.10. Higher sensitivity to WF and OX1, can be seen as an effect of velocity saturation and feedback capacitances. This velocity saturation results from the increase of electric field near the drain side. For LDE sensitivities, we can observe, the sensitivity reducing from positive to negative values, while OX1 and OX2 shows similar trends of the DG1 sensitivity charts.

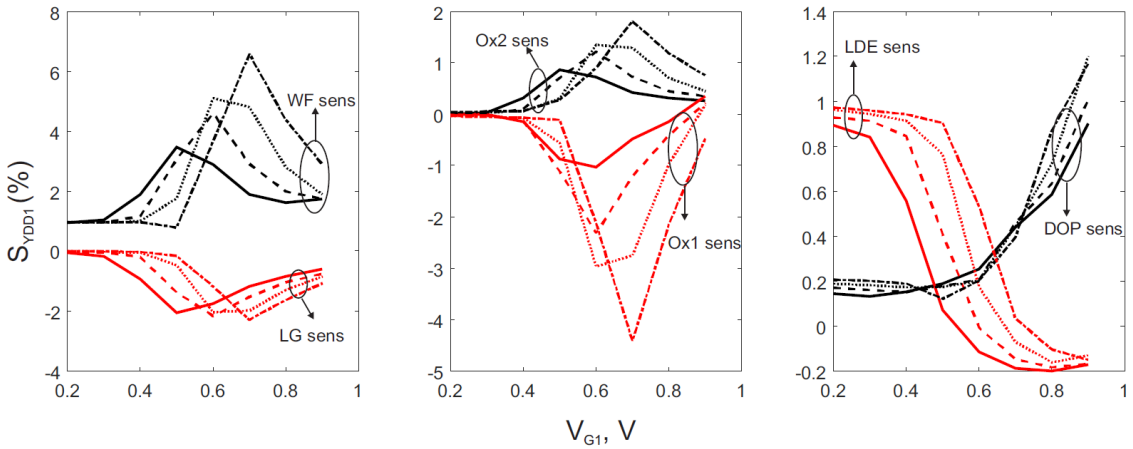

Figure 7.10: Sensitivity chart of the real part of the (D,D) element of the admittance matrix. Solid: VG2 = 0.2 V. Dash: VG2 = 0 V. Dot: VG2 = -0.2 V. Dash-Dot: VG2 = -0.4 V. [33]

Now, lets have a look at imaginary parts of the GG elements, In Fig. 7.11, as a general trend we can observe that, sensitivities are independent of the back-gate voltage. This is due to the fact that, the sensitivities are changing in Fig. 7.11 in response to the change in VG2. LG sensitivity is most influential of all and WF is also effective in comparison to the other sensitivities. Dependency on LG is almost linear before and after the threshold. While WF sensitivity changes from negative to positive with an increase in VG2 bias and shows more or less the inverse square root of fin variations. DOP and LDE sensitivity shows more or less similar trends of sensitivities to that of DG1 sensitivities.

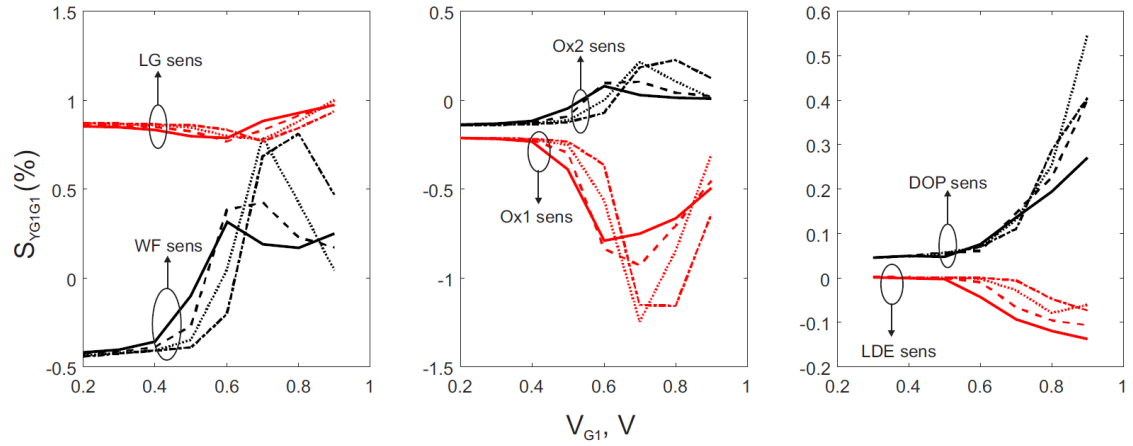

Figure 7.11: Sensitivity chart of the imaginary part of the (G1,G1) element of the admittance matrix. Solid: VG2 = 0.2 V. Dash: VG2 = 0 V. Dot: VG2 = -0.2 V. Dash-Dot: VG2 = -0.4 V. [33]

Fig. 7.12 shows the sensitivities for the VG1 voltage and we can observe that LG sensitivity is very high in comparison to other parameters and dependency is almost linear for LG. These sensitivities are not much affected by VG2 bias, i.e., all lines are quite coincident. Even below the threshold, we can see very low dependency on the VG2 Overall the sensitivities are very small for all parameters in this case.

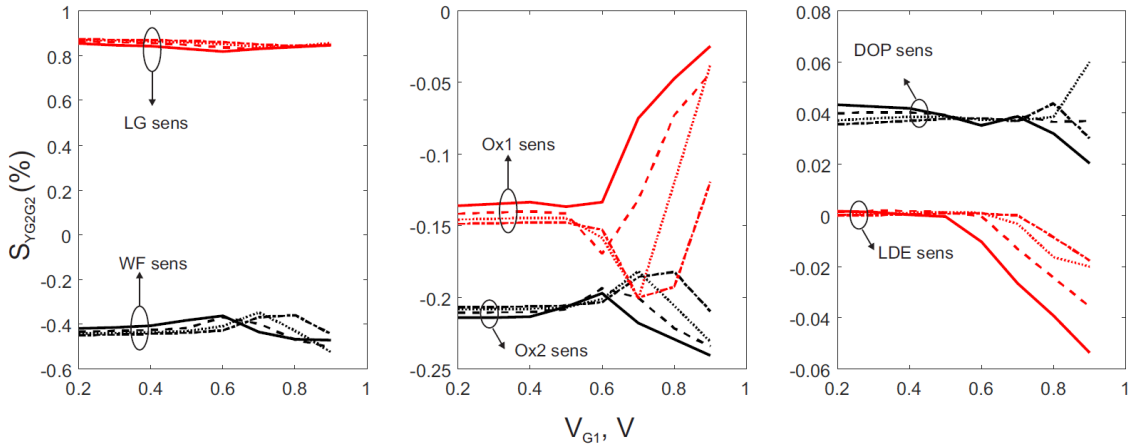

Figure 7.12: Sensitivity chart of the imaginary part of the (G2,G2) element of the admittance matrix. Solid: VG2 = 0.2 V. Dash: VG2 = 0 V. Dot: VG2 = -0.2 V. Dash-Dot: VG2 = -0.4 V. [33]

In Fig. 7.13, we are showing the sensitivity of imaginary part of the DD element, and Fig. 7.13 depicts that the sensitivities are increasing above the threshold for all parameters. Below the threshold, sensitivities are linear with respect to WF and show square root dependency with respect to DOP. Also for the other four parameters, i.e., LG, OX1, OX2,and LDE show negligible sensitivities below the threshold and are also independent of back gating voltage.

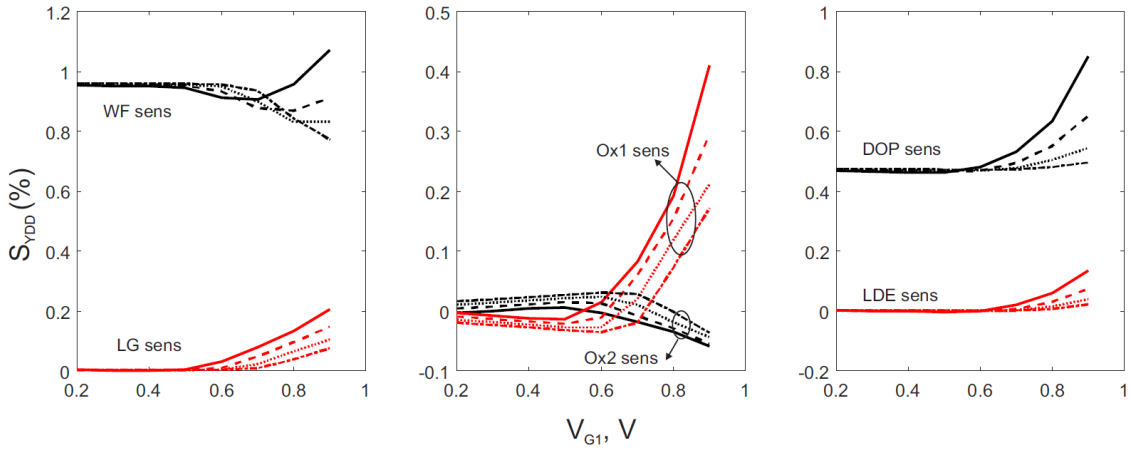

Figure 7.13: Sensitivity chart of the imaginary part of the (D,D) element of the admittance matrix. Solid: VG2 = 0.2 V. Dash: VG2 = 0 V. Dot: VG2 = -0.2 V. Dash-Dot: VG2 = -0.4 V. [33]

Overall, we can conclude that, variations are more limited to real parts in comparison to the imaginary parts, and show less dependency on the back-gate voltage: this clearly reflects the fact that the capacitances are more tightly related to geometry. We can also conclude that the capacitances (imaginary part) are less sensitive below the threshold and the sensitivities increases above the threshold voltage. We also found that Y parameters dominated by parasitics are loosely affected by the gate bias, while the sensitivity of (D,G1) element is highly affected by the gate bias. We also found from our sensitivity charts that the sensitivity of (D,D) element is high in response to fin variations with varying bias. Overall, WF and oxide variations are the critical source of variations, when the DG FinFET is used as an IG FinFET exploiting the back gating effects.

7.3 Summary

This chapter was dedicated to the IG version of FinFETs, where the voltage applied at both the gate terminals is not symmetrical, i.e., the gates are isolated physically. This chapter is divided into two parts.

First, we have shown on the comparison of IG and SG devices, in terms of their AC performance to show their peculiarity in terms of sensitivity. IG and SG cases had different sensitivities of the AC parameters. We found that the DD elements have similar sensitivity to parameter variations, which shows that its dependence on parasitic elements rather than the bias applied at gate terminals. While, in the case of DG element (both admittance and capacitance), we see different sensitivities to parametric variations, thus, showing the bias dependency. While GG capacitance have very complicated behavior but is mainly dependent on gate bias. In the

case of mutual gate capacitances, the element values are smaller than the diagonal case, their sensitivity to variations is extremely strong, i.e., from 20 to 50%. Fin variations are quite dominant in comparison to other parameters. The imbalance gate bias brings mutual capacitances into account which can affect the feedback capacitances.

In the second part of the chapter, we expressed the AC behavior of the IG FinFET in terms of the *sensitivity charts*. These results can be useful in successful design of analog stages of electronic circuits. We found *sensitivity chart* as an important tool for the AC characteristics with concurrent parametric variation and gate bias dependency. We showed the tuning of the threshold voltage capability of the back gate, i.e., reducing the back gate voltage results in the increase in threshold voltage. We also observed form the sensitivity charts that transconductance and output conductance are dependent on gate biases. While the capacitances are independent of the back gating effects. Generally, all parameters dominated by device parasitics (geometric dependency) are not influenced by the gate biases especially below the threshold. While we also observed that WF and OX variations are most critical in RF applications exploiting back-gating effects and they need to be carefully studied before the final stages of the device fabrication.

In the next chapter, we will show the application of sensitivity charts to mixers exploiting IG variants of DG FinFET.

Chapter 8

RF mixer optimization exploiting Sensitivity Charts

The gate terminals of an IG FinFET can be driven individually and independently, which adds to a dimension of applications. IG FinFET have been proposed for many applications, such as novel high speed circuit modules and implementation of different logic gates [129] [130]. In Ref. [131], Reddy et al. implemented different RF mixer topologies using MOSFETs, SG FinFET and IG FinFET for a power-area product comparison and conclude that IG FinFETs offers good performance above 40 GHz, while below 40 GHz, SG FinFETs can be seen as a better option. This opens up interesting possibilities for circuit applications using multigate technologies to mixers. In IG FinFETs, we can supply the RF and LO (Local Oscillator) signals selectively to each of the gates. These IG FinFETs also offer inherently the gate isolation and easier matching with respect to single gate devices. This feature of IG FinFETs has driven significant interest in developing mixer circuits. Commercial manufacturers of electronic devices, like Motorola, NXP Semiconductors, and Hitachi, have already used multigate devices for mixer and amplifiers. While, starting from analog applications based on III-V technologies, in multigate devices like HEMTs, the gates are in "*series*", i.e., the overall drain current is same, in IG FinFETs, the drain current can be modulated with the use of back gating effects. The mixer topology based on multigate FinFET is, therefore, different than the traditional ones.

8.1 Mixer design

We used the IG FinFET structure already introduced in Chapter 7. The mixer topology used here is shown in Fig. 8.1 [128]. The idea behind the mixer is following the usual CMOS mixer design where g_m time modulation is used to produce the desired mixing. The two gates of IG FinFET are biased such that the front gate

should be in inversion and the back gate should be strong enough to modulate the g_m of the front gate. An RF signal at the frequency of 60 GHz is applied to the front gate and the LO signal is applied to the back gate. This LO signal modulates the channel transconductance turning the device from ON to OFF condition to achieve the frequency conversion, while keeping the back gate channel off.

We used the GFs approach to investigate the mixer sensitivity. First, DC simulations are used to investigate the FinFET behavior subject to back-gating, showing that the LO signal must be a square wave limited between V_{G2} = - 0.4 V (lower values would drive the backchannel into accumulation) and V_{G2} = 0.2 V (higher values would turn-on the back-channel). AC simulations are then used to extract the nominal value of the mixer gain with varying front gate bias. The LO frequency is supposed close enough to the RF one to neglect dispersion in the down-conversion.

Here, a preliminary analysis is carried out with a quasi-static approach like usually done for CMOS applications. This investigation may be considered as the preliminary step towards more accurate multi-frequency Harmonic Balance based analysis.

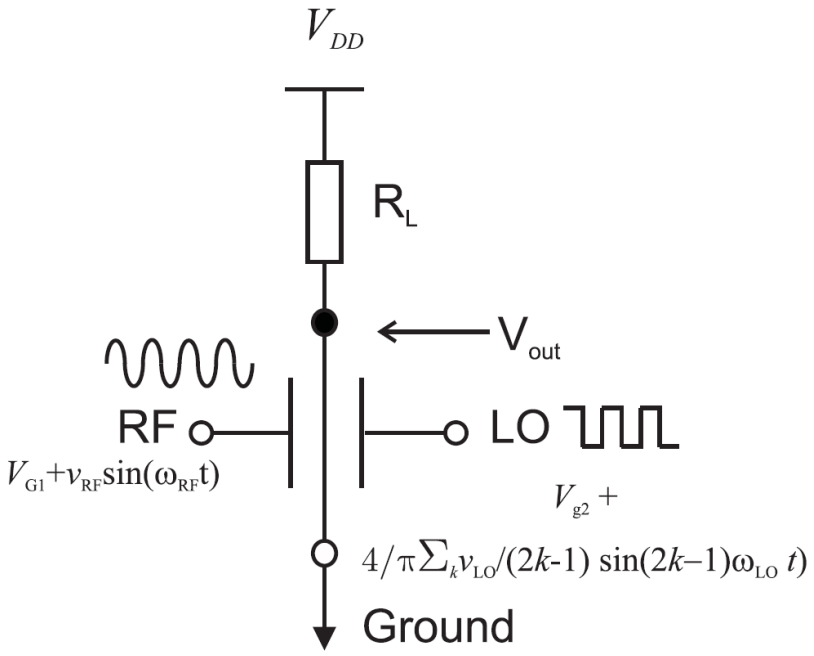

Figure 8.1: Mixer topology for a IG DG FinFET [128]

Defining the largest and the smallest values of the device transconductance with varying LO:

$$\begin{aligned} y^+ &= Re(Y_{D,G1}(V_{G1}, V_{G2} = 0.2, V_D)) \\ y^- &= Re(Y_{D,G1}(V_{G1}, V_{G2} = -0.4, V_D)) \end{aligned} \tag{8.1}$$

the conversion gain G_c of the mixer is given by [128]:

$$G_c = \frac{R_L}{4}(y^+ - y^-) = \frac{R_L}{4}\Delta y \tag{8.2}$$

where R_L is the mixer load, as shown in Fig. 8.1.

Now, as we can see from Eq. 8.2, we can maximize the conversion gain by maximizing the Δy. In Fig. 8.2 , we plot the transconductance response for the different front gate voltages. We found that the Δy is largest between the front gate bias of 0.6 to 0.8 V. In the FinFET mixer stage, parallel fingers must be used to enhance the output power. Assuming a stage with 200 fingers, i.e. a total width of 10 μ m, and RL = 500 Ω [128], the conversion gain is found to be 1.3 dB for V_{G1} = 0.6 V, 5.8 dB for V_{G1} = 0.7 V and 1.85 dB for V_{G1} = 0.8 V.

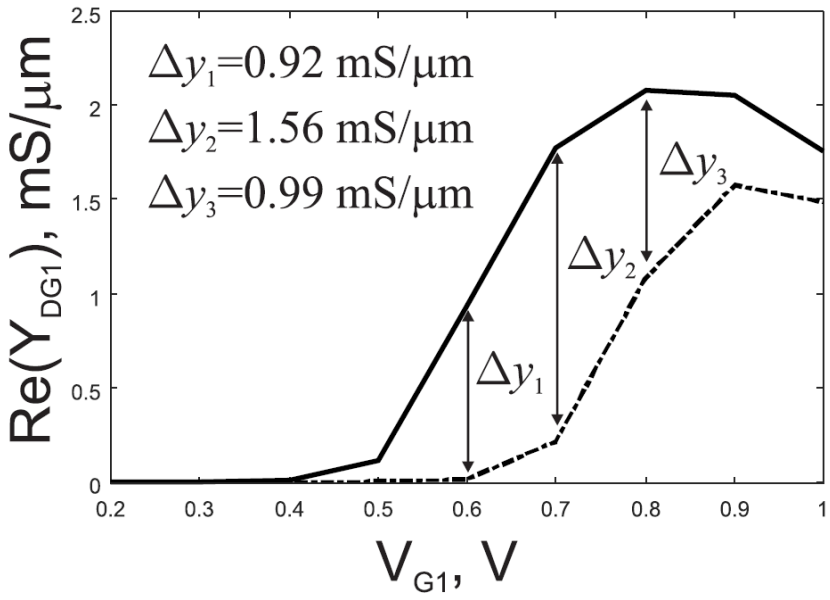

Figure 8.2: Real part of the (D,G1) i.e. quasi-static g_m element of the Y matrix. Solid: V_{G2} = 0.2 V; Dash-dot:V_{G2} = -0.4 V [132].

8.2 Mixer variability-aware design

Like any other MOSFET devices, mixer is also prone to variability and in this section, we will focus on variability analysis of the mixer stage. We will study the impact of all relevant parameters already shown in the previous Chapter 5, i.e., WF, OX1, OX2, DOP, LG and LDE. We will exploit the *sensitivity charts* analysis presented in section 7.2.2, as a flexible tool to provide a global view of the mixer sensitivity in response to the variations in process parameters.

If a mixer stage is affected by any parametric variation, then the induced variation in conversion gain mixer is given by the expression:

$$\delta G_c = \frac{R_L}{4}(\delta y^+ - \delta y^-) \tag{8.3}$$

where δy^+ *and* δy^- are the variation in the transconductance of the device due to process parameter variations. The relative sensitivities of y^+ and y^- is given by:

$$\begin{aligned} S^+ &= S_{Re(Y_{D,G1})}(V_{G1}, V_{G2} = 0.2, V_D) \\ S^- &= S_{Re(Y_{D,G1})}(V_{G1}, V_{G2} = -0.4, V_D) \end{aligned} \tag{8.4}$$

these relative sensitivities were already reported in Fig. 7.9, we shall now take with the largest and lowest value of the LO signal i.e., $V_{G2,S} = V_{G2}$= 0.2 and -0.4 V. Converting the relative sensitivities into absolute variations:

$$\begin{aligned} \delta y^+ &= S^+ y^+ \frac{\delta P}{P_0} \\ \delta y^- &= S^- y^- \frac{\delta P}{P_0} \end{aligned} \tag{8.5}$$

the mixer conversion gain is shown to be affected by variability:

$$\delta G_c = \frac{R_L}{4}(S^+ y^+ - S^- y^-).\frac{\delta P}{P_0} \tag{8.6}$$

In realistic technologies, variations are random processes. Assuming random variations of a parameter P characterized by zero average and a normal distribution with variance σ_P^2, the conversion gain also has a normal distribution, with variance.

$$\sigma_{GC}^2 = K_{G_c}\langle \delta G_c, \delta G_c \rangle = K_{G_c}\langle (S^+ y^+ - S^- y^-)\delta P, (S^+ y^+ - S^- y^-)\delta P \rangle \tag{8.7}$$

where, $K_{G_c} = (\frac{R_L}{(4P_0)})^2$. Finally,

$$\sigma_{G_C}^2 = K_{G_c}(S^+ y^+ - S^- y^-)^2 \sigma_P^2 \tag{8.8}$$

It is worth noting that the variations y^+ and y^- both corresponds to variations of the same parameter P. Since, they are fully correlated and as shown in Eq. 8.8, if the signs of the two sensitivities, i.e., $S^+ y^+$ *and* $S^- y^-$ are same, then the cancellation in $\sigma_{G_C}^2$ can occur. On the basis of this deduction, we can optimize the mixer conversion gain.

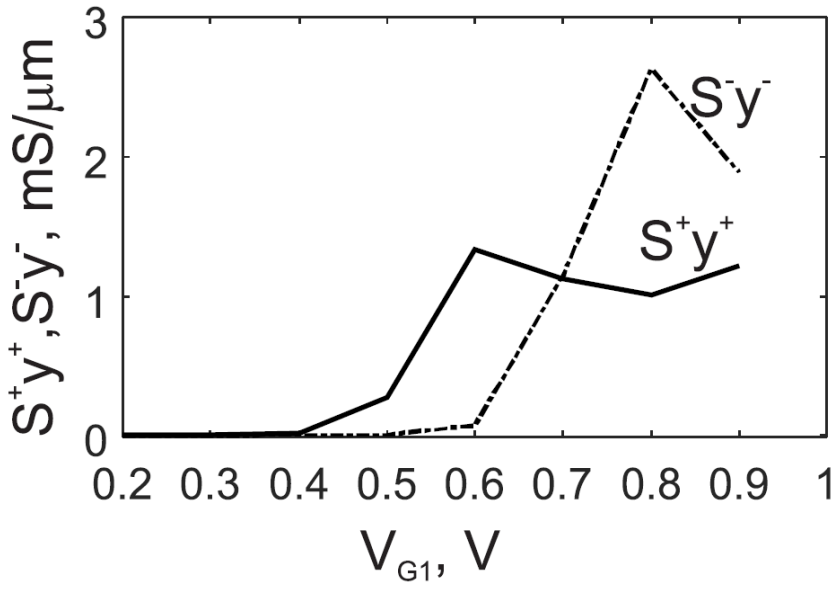

Figure 8.3: Variation S^+ y^+ (solid) and S^- y^- (dash-dot) for fin width variations.

Looking back to the conclusions from section 7.2.2 and Fig. 7.9, the most dominant parameter, in IG device is WF. So, keeping in mind WF, we can use the sensitivity charts to extract S^+ *and* S^- performance of the mixer to optimize the mixer gain.

In the plot shown in Fig. 8.3, we can see the sensitivity chart for two back gate voltages, i.e., V_{G2}. At V_{G2}= 0.7 V, we can see that sesitvities are coincident,hence allowing for nearly exact cancellation in eq. 8.8. So at that point we can say the sensitivities to variation will be close to zero. While if we look at 0.6 and 0.8 V, the sensitivity to variations is large and we can only see partial cancellation, while, overall device performance will be more prone to process variations. For, 10% variations fin variations, at 0.6 V 14 % and at 0.8 V 16% conversion gain variance was observed, while approximately 0 variance was observed at 0.7 V.

Overall, we found that, at V_{G1}=0.7, we had minimum sensitivity to fin variations and maximum conversion gain. Hence, we can say that an optimum condition is identified both for conversion gain and for maximum immunity for variations.

8.3 Summary

In this chapter, we focused on the application on IG FinFETs. We discussed the application of IG FinFETs in mixers. We discussed, how mixers can be implemented with the help of individual and independently driven gate voltages. This mixer topology is found to be extremely attractive due to its compactness and high conversion gain. This mixer design concept, exploiting the dual gates operating

individually, of FinFET need to be validated in terms of RF performances and their robustness toward technology variations. We have shown that the sensitivity towards physical parameters can impair the successful design of the stage, but a careful choice of the operating conditions leads instead to a concurrent maximization of the conversion gain and minimization of its variability. This immunity is achieved even when a non-balance technology is chosen. Notice also that in balanced mixers exploiting more than one device, variations from different devices are *not correlated*, hence variability is still a problem. This further demonstrates that IG mixers are extremely attractive for RF applications.

We exploit IG FinFETs capability of having two different biases at the gates and used it as a Mixer, by applying RF signal at the front gate and LO signal at the back gate. With fin variations as dominant source of RF variability, 10% WF deterministic variation were applied and we found that, at around 0.7 V at the front gate terminal, we get the maximum conversion gain and minimum sensitivity to process variations.

In the next chapter, we will conclude this thesis with the concluding remarks.

Chapter 9

Conclusion

This chapter is divided in two parts. In the first part we will conclude this work, while in the second part, we will discuss possible future works in this field.

9.1 Concluding Remarks

The presented research carried out as a part of doctoral dissertation thesis addresses the modeling aspects of FinFET variability. Unlike several on-going activities that mainly contribute to the modeling and thus the derivation of several variability parameters to better understand the DC electrical properties in FinFET devices; our contribution targets the AC sensitivity of FinFET devices towards variations of the main parameters, especially the ones affecting the device parasitics. We presented a model to estimate the device response to different process variations. We exploit an extremely efficient, yet accurate, simulation approach based on GFs, allowing for considerable simulation time saving with respect to the variability analysis based on incremental approach. The variations of Y admittance matrix has been shown as a function of all the relevant parameters. For validation, the results from the GF approach were compared to those from the much more computationally intensive incremental analysis, i.e., by repeatedly solving the DC + AC equations with varying parameters. It saves around 95% in simulation time for 20% parametric variations.

For the single fin FinFET, the role of the source resistance has been highlighted especially for the drain-gate and gate-gate elements, yielding a strong correlation between the variations of the fin width and of the doping. The contrary is true for the extensions' length. While the physical properties of the extensions are not significant, below the threshold, the fin width sensitivity is never negligible and is especially high in the subthreshold condition. The applicability of the proposed model to a double fin FinFET was also studied and validated. In the case of

double fin, in addition to the variability impacts of the single fin case, the gate-source (drain) capacitances shows significant dependency on the LDE. In double fin case, fin width separation becomes another dominant source of variation related to inter fin coupling.

Moreover, the proposed model for simulating variations, i.e., GF approach, highlights the regions of the device most sensitive to the variations: hence LVSs have been investigated and discussed. Apart from the depleted regions, the main source of variability is uniformly distributed in the source extension both for the drain-gate and gate-gate elements, while the drain extension is the region where variations of the feedback capacitance arise.

Simulations were performed on the IG version of DG FinFET as well. Same in-house simulator(POLITO) was used for this analysis, which results in a significant amount of reduction in simulation time and shows very good accuracy to around 20% of variations. The comparison of SG and IG variants in response to the parameters variations with asymmetrical gate voltages (for IG case), enlightens the fact that the parameters such as Drain-Drain admittances are more immune to change in bias at terminals and are more susceptible, while the capacitive elements, such as, GG elements (both *diagonal* and *off-diagonal*), shows a strong dependency on the gate biases.

POLITO in-house simulator was also used to extract the sensitivity charts for the IG FinFET. These sensitivity charts relate the percent variation in Y parameters to percent variation in physical parameter. We found that Y parameters prone to parasitics variations are immune to the varying gate bias, while the sensitivity of transconductance and output conductance is most affected by varying gate bias. FinFET parasitic capacitances are mostly geometrical, thus are immune to a difference in gate bias.

For RF applications, fin width and oxide thickness can be seen as critical parameters and are required to be addressed properly, when the backgating effect is used. Mixers can be seen as one of the possible application of IG version of FinFET. The sensitivity analysis of mixer, before its implementation, aids to the successful design of the mixer. With the help of *sensitivity charts*, we found that operating the mixer at the optimized front gate voltage can result in increased conversion gain and reduced variability. At the optimized bias, the net effect of parameter variations is canceled, due to correlated variations. For 10% fin variations, instead. gate front voltage different from the optimum one result in upto 16%, variance in conversion gain. While at optimum bias, approximately 0 variance in conversion gain was observed. Hence, we can conclude that we can exploit sensitivity analysis for the optimization of RF stages in terms of robustness to process variations.

9.2 Future work

This thesis can be extended in the following directions:

- We limited our work to most relevant variations, but other sources of variations can also be incorporated to study the variations, e.g., thermal variations
- In this work, we analyzed the variations individually and studied their impact on the FinFET device, multiple parametric variations can be applied to collectively study the effect of variations and globally optimize the device performance.
- Other possible variants of FinFET transistors, such as novel materials III-V group (InGaAs) or GAA, can also be used for variability analysis for implementation of FinFETs.
- Enhancing the capabilities of our in-house simulator POLITO to implement the GF approach on 3D FinFET structure.

Appendix A

Appendix

A.1 POLITO in-house simulator

There are many commercial software available for variability analysis of FET devices, e.g., Synopsis Sentaurus. These commercial applications are generalized tools to simulate the device. There are peculiar requirements, which are difficult to perform (require hectic efforts) with these commercial applications. For example, if I had to change the charge on a single node, it would be difficult to do in commercial application. This modification can be easily performed in our in-house simulator. Also, there are many other data, which we want to alter but we don't have access to these informations in commercial tools.

Independent simulation software provides us with complete access to the simulation files, which leads the research groups to the development of their own simulation software. With continuous efforts of the Microwave research group in Politecnico di Torino, a powerful tool for LS physical analysis, including variations have been developed. The development of tool started back in 2004 and continuous efforts has been put to improve the tool reliability and efficiency. The code is at present time restricted and not available as open-source. Hence, details of the implementations are not reported.

The main characteristics of this simulation tool is the implementation of a small and large signal solver using the Harmonic Balance (HB). The Harmonic Balance technique is applied to the discretized physics-based model to determine the LS steady-state solution, and a generalization of the circuit SS–LS HB analysis is exploited to determine, from physics-based models, the device conversion matrix. The present approach directly generalizes the classical Green's function approach and the related impedance field method (IFM). The evaluation of GF is carried out with the help of Branin's method, to avoid the heavy computational burden due to large number of back substitutions.

FEM graphical user interface (GUI) allows for domain geometry, mesh description, and computes mode to the Matlab workspace. Once the structure's geometry

have been created, we can load them from the GUI and start the simulation.

The mesh generator *Rectmesh* is a simple 2D mesh-generator included in the in-house code *POLITO* which allows to create a triangular mesh after dividing the domain in rectangular elements. After dividing the total domain in rectangular region, the user must set a division number for the direction x and y for every region.

The in-house simulator implements the 2D Drift-Diffusion model, in Matlab, with a box discretization to ground the device. The solution of the system is evaluated through the iterative Newton method which allows to calculate an approximation of the non linear system solution only if it's possible to calculate the function and its Jacobian in all the domain.

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