A Unified Approach for Performance Degradation Analysis from Transistor to Gate Level

International Journal of Electrical and Computer Engineering (IJECE)
Vol. 8, No. 1, February 2018, pp. 412 – 420
ISSN: 2088-8708, DOI: 10.11591/ijece.v8i1.pp412-420

A Unified Approach for Performance Degradation Analysis from Transistor to Gate Level

Izhar Hussain, Marco Vacca, Fabrizio Riente, and Mariagrazia Graziano
Department of Electronics and Telecommunications , Politecnico di Torino, Italy

Article Info

Article history:
Received: Jul 25, 2017
Revised: Nov 9, 2017
Accepted: Dec 1, 2017

Keyword:
Scaling Process
Emerging Technologies
Web-based Services
Education
Fifth keyword

ABSTRACT

In this paper, we present an extensive analysis of the performance degradation in MOSFET based circuits. The physical effects that we consider are the random dopant fluctuation (RDF), the oxide thickness fluctuation (OTF) and the Hot-carrier-Instability (HCI). The work that we propose is based on two main key points: First, the performance degradation is studied considering BULK, Silicon-On-Insulator (SOI) and Double Gate (DG) MOSFET technologies. The analysis considers technology nodes from 45nm to 11nm. For the HCI effect we consider also the time-dependent evolution of the parameters of the circuit. Second, the analysis is performed from transistor level to gate level. Models are used to evaluate the variation of transistors key parameters, and how these variation affects performance at gate level as well.The work here presented was obtained using TAMTAMS Web, an open and publicly available framework for analysis of circuits based on transistors. The use of TAMTAMS Web greatly increases the value of this work, given that the analysis can be easily extended and improved in both complexity and depth.

Corresponding Author:
Izhar Hussain
Department of Electronics and Telecommunications ,
Politecnico di Torino, Italy
ihussain899@gmail.com

1. INTRODUCTION

The MOSFET transistor has proven to be a very robust device. As testified by the ITRS Roadmap [1], its size has been reduced from micrometers to nanometers over the course of the last four decades. The extraordinary development of electronics is due mainly to this continuous physical scaling. Nowadays commercial devices employs transistors that have a size of few tenth of nanometers [2]. A single chip can house billions of transistors [3]. Scaling at such a fast pace eventually leads to increased variability and reliability issues, that pose a unique challenge for circuit lifetime estimation [4].

1.1. State of the art analysis

Variations can be categorized into two main types, depending on their source of origin; process- induced variation and intrinsic fluctuations [5]. Intrinsic variability and reliability such as Oxide Thickness Fluctuation (OTF) and Random Dopant Fluctuation (RDF), are induced by charges and geometrical fluctuations at atomic scale level. These variations and reliability issues are unique to device structure and their effects may be different for different CMOS devices. On the other hand, process-induced variations are caused by defects during silicon fabrication, which may be particular to a process in a foundry. In addition, transistor performance not only depends upon static process variations, but transistors parameters also start to degrade over time. This individual device degradation, named aging, affects the circuit performance metrics over a period of time. These effects are, as an example, Negative Bias Temperature Instability (NBTI), Hot-carrier-Instability (HCI) and Time Dependent Dielectric Breakdown (TDDB) [6][7][8]. Such performance limiting mechanisms are being investigated since three decades, but they are more pronounced in the nano-scale regime now and are inevitable for design consideration as the equivalent oxide thickness scales down as low as 5 Angstrom in the future [9]. These intrinsic variations and aging parameters are limited by fundamental

device physics, making it one of the ultimate bottleneck for CMOS design process and continual technology scaling. As the device size approaches to atomic dimensions,the intrinsic variability and reliability considerations have become integral part of CMOS circuit design by the technologists. The most notable change that these effects have on a transistor is a shift in the value of threshold voltage (V_{th}) and mobility (μ). As a consequence, reliability issues leads to performance degradation and eventually to the failure of devices. While the effects of variations on a single transistor are well known and studied, it is more difficult to understand their impact at logic gate level. In [10] a reliability analysis was performed on a static RAM memory.

Transistor with planar and simpler structures have been extensively studied over the past decades. Reliability analysis of complex structures and advances devices has also been presented in literature. For example, the work presented in [11] focuses on junctionless Fet transistors, while in [12] authors analyze sub-20 nm asymmetric DG devices. In [13] Shashi Kant Dargar performed degradation analysis of GaN Based Thin Film Transistors. Finally, given that many technologies are currently studied as possible MOSFET replacement, reliability analysis has been conducted also on emerging technologies. For example in [14] authors studies effect of device variables on surface potential and threshold voltage in Double gate graphene FET (DG-GNRFET). Instead in [15] authors focus on carbon nanotube FETs.

1.2. Motivation of the work

The aim of this paper is to analyze in a coherent way the impact of reliability on the transistor's performance. Particularly, we are interested to analyze the performance degradation due to the Oxide Thickness Fluctuation (OTF), Random Dopant Fluctuation (RDF) and Hot-carrier-Instability (HCI). The novelty of our approach is that we consider and evaluate the effect of these issues starting from the transistor level up to gate level together.

- The E. Maricau [7] and Yu Cao [4][9] models are used for the Oxide Thickness Fluctuation (OTF), Random Dopant Fluctuation (RDF) and Hot-carrier-Instability (HCI), to evaluate the variation of threshold voltage (V_{th}) and mobility (μ). The consequent change in the drive current (I_{on}) are evaluated.
- The variation of V_{th}, μ and I_{on} has been analyzed considering three different types of MOSFETs: BULK, Silicon-On-Insulator (SOI) and Double Gate (DG) considering the technology scaling. Technology nodes from 45nm to 11nm are studied.
- For the HCI effect [7][9], both the trend with technology scaling and the time-dependent evolution are studied.
- A model to estimate the performance of standard logic gates, both in terms of timing and dynamic power, was developed. The model takes into account the variation of the parameters of transistors, therefore it is possible to evaluate the impact of reliability at logic gate level.
- Using a NAND gate as a testbench, the variation of timing and dynamic power considering both the technology scaling and the time dependent analysis (for the HCI effect) are carried on. The analysis is repeated for all the three types of transistors.

2. SIMULATION TOOL

Among the performance estimation tools, MASTAR is the best-known [16]. It is used by the International Roadmap for Semiconductors [1] to forecast future transistors performance. Unfortunately, MASTAR limits the analysis at the device level. To explore system level parameters, another tool named BACPAC [17] can be used. It includes a large set of analytical models to estimate and predict the performance of future VLSI circuits. However, both these tools present some limitations. They are restricted to one abstraction level, that can be the device, the gate or system level. Moreover, they are focused on MOSFET technology and do not consider emerging devices. To overcome these limitations and enable the performance estimation of electronic circuits from device to system level, we developed TAMTAMS (Torino Assessment of Mos Technology and Advanced perforMance of System Calculator). TAMTAMS is a web-based tool, presented in [18], that combines the device level analysis available in MASTAR with the system level analysis provided by BACPAC. TAMTAMS is developed by the VLSI group at Politecnico di Torino and it is constantly evolving. Currently, it is used as teaching tool in the master level course Integrated System Technology for the Electronics Engineering Master degree held at Politecnico di Torino.

TAMTAMS includes many models and technologies. Its flexibility and modularity eases the extension of new modules and new technologies. At the time of writing, CMOS technology is fully supported. It includes BULK, SOI and double gate (DG) devices. Within digital electronic circuits, three abstraction level can be identified: i) device level, ii) gate level, iii) system level. The TAMTAMS structure is summarized in Fig. 1. It is built considering this three-layered

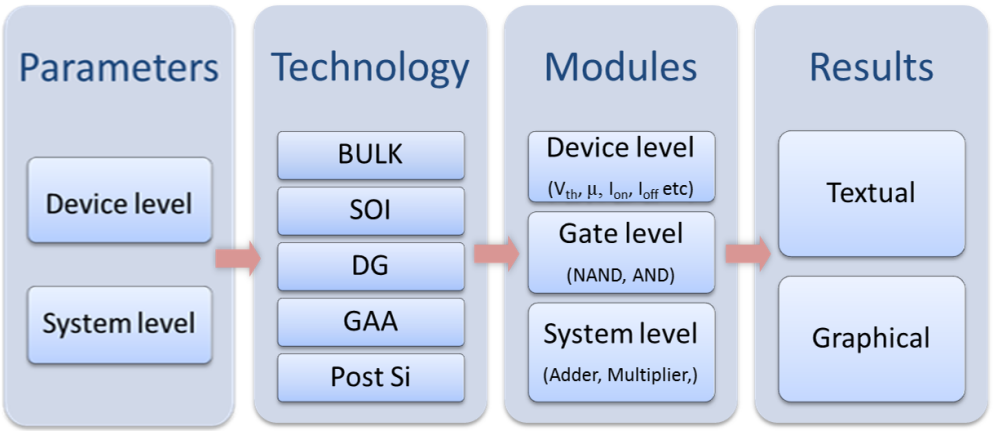

Figure 1. TAMTAMS analysis flow. Three kind of analysis are possible: device level, gate level and system level. Device and system level parameters are used according to the kind of investigation selected by the user. Computed results are reported in a textual or graphical form.

structure. In the lowest level of abstraction, device level models can be found. To this category belong threshold voltage, mobility and current models. Implemented models are specific for the selected technology (BULK, SOI, DG). The physical characteristics of a transistor, such as gate length, the gate oxide thickness, etc.., are grouped in the device parameters. Moving to a higher level of abstraction, a gate level analysis can be executed. Here NAND/AND, Flip-Flop models are available. The analysis starts from device level modules, whose results are used by gate level models.

System level analysis is based on a set of technology independent parameters. They can be the total number of transistors, the percentage of memory and logic within a digital circuit. Another important feature is that TAMTAMS automatically solves and keep track of all the module dependencies. According to the analysis selected by the user, the dependency tree is analyzed and the proper models are solved. Computed results are reported in a textual or graphical form. Thus, data can also be post-processed by using external tools.

In addition, TAMTAMS supports parametric analysis, i.e. device or system level parameters can be varied to understand their impact at different abstraction levels. Indeed, this approach has been exploited in paper to analyze the effect of threshold voltage degradation with time.

3. TRANSISTOR PERFORMANCE DEGRADATION

3.1. Description of Models

This work focuses on the prediction of performance degradation as the technology scales down, both at transistor level as well at circuit level. Predictive technology models for reliability aware transistor to circuit design analysis were considered. The models are scalable with wide range of technologies and process variations [7][4][9]. Variation in threshold voltage V_{th} and carrier mobility μ at device level provides the basis for the performance degradation analysis at circuit level. In the next sections, static and time-dependent models are described before presenting the obtained results.

3.1.1. Static variability model

The primary intrinsic variations are Random Dopant Fluctuation (RDF) and Oxide Thickness Fluctuation (OTF).

The RDF phenomena arises due to variation of impurity concentration during ion implantation process. RDF is more pronounced in smaller transistors as the technology scales down. Because of lower doping concentration, addition or deletion of a few impurity atoms can significantly change transistor properties, especially the V_{th}. The physics based model, as stated in [4] is given by:

$$\Delta V_{th(RDF)} = \frac{q}{C_{INV}} \sqrt{\frac{N_{ch} W_{dep}}{3WL}} \times 1.2 \quad (1)$$

where W, L, N_{ch}, W_{dep} are the channel width, channel length, channel doping and depletion width, respectively. A more explicit expression is obtained by expanding the W_{dep} term and ignoring other second order terms. Equation 1

becomes:

$$\Delta V_{th(RDF)} = C_1 \frac{q}{\sqrt{3WL}} \frac{t_{oxe}}{\varepsilon_{ox}} \left(\frac{2\varepsilon_{Si} N_{ch}}{q} \right)^{1/4} \tag{2}$$

where C_1 is a fitting parameter accounting for surface potential. The other parameters, $t_{oxe}, \varepsilon_{Si}, \varepsilon_{ox}$ and q are the equivalent oxide thickness, permittivity of silicon, permittivity of the oxide layer, and elementary charge, respectively. The above equation suggests that RDF induced variation is directly proportional to t_{oxe} and ${N_{ch}}^{0.25}$.

The OTF phenomena arises due to surface roughness between silicon and gate oxide interface at atomistic level. As V_{th} is directly proportional to gate oxide thickness T_{ox}, any fluctuation in oxide thickness leads to change in V_{th}. This effect is even more highlighted when the gate oxide thickness approaches atomic dimensions [4]. The threshold voltage variation due to oxide thickness fluctuation can be expressed as:

$$\Delta V_{th(OTF)} = C_4 \frac{\sqrt{qN_{ch}\varepsilon_{Si}}q}{\varepsilon_{ox}} \frac{\lambda}{\sqrt{2WL}} \Delta H, \tag{3}$$

where C_4 is the only fitting parameter. ΔH represents the minimum possible magnitude of OTF, that is the height of one silicon atom layer which is equal to 2.71 Å. The correlation length λ of OTF typically ranges between 1-3nm, as reported in [4].

3.1.2. Time-dependent reliability model

As mentioned, many effects can degrade the device performance over time. In the following, the Hot-Carrier-Instability (HCI) aging mechanism and its corresponding model are described. HCI manifests itself as an increase in the threshold voltage V_{th} and carrier mobility μ, especially for the NMOS transistor [9][6][7]. The HCI model is based on the classical Reaction-Diffusion (R-D) model [6]. HCI mechanism can be physically described as generation of charges at the $Si - SiO_2$ interface. HCI model shows power law dependence with time t. As reported in [7][9], analytical model for shift in V_{th} and μ as a function of stress, operating condition and device parameters can be expressed as:

$$\Delta V_{th(HCI)} = A[(V_{gs} - V_{th})K_v]^{n_x + 1/n_x} (\frac{n_x t}{L})^{\frac{1}{1+n_x}}, \tag{4}$$

where

$$K_v = exp(\frac{E_{ox}}{E_o}) exp(\frac{-\phi_t}{q\lambda E_m})(\frac{-E_a}{KT}), E_m = \frac{V_{ds} - V_{dsat}}{l}, l = 0.2(T_{ox})^{0.33}(Xj)^{0.5},$$

$$V_{dsat} = \frac{L_{eff} E_{sat}(V_{gs} - V_{th})}{L_{eff} E_{sat} + (V_{gs} - V_{th})}, E_{ox} = \frac{V_{gs} - V_{th}}{T_{ox}}, C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}, V_t = \frac{KT}{q}.$$

The increase in concentration of interface charge N_{it} also result in increase of mobility μ. The mobility degradation is given by:

$$\mu = \frac{\mu_e ff}{(1 + \alpha N_{it})^m}, \alpha = 5, m = 1.6, \tag{5}$$

Default values of the technology independent model coefficients as stated in [7][9] are shown in Table 1.

Table 1. HCI Model parameters

A	1.5e-5	vsat (m/s)	1e5
n_x	1.21	Φ_t (eV)	3.7
q (C)	1.6e-19	E_0 (V/m)	0.71e8
$\lambda(m)$	7.8e-9	Θ (V)	0.95
E_a	- 0.06	K (J/k)	1.38e-23

where n_x, E_0, E_a and A are process parameters, ϕ_{it} is the critical electron energy for generating an interface trap, E_m is maximum channel electric field which occurs at the drain end of the channel, l is the pinch off length, λ is hot electrons mean free path, E_{ox} is electrical field across oxide, V_t is the thermal voltage at room temperature and t is stress time given in seconds [7] [9]. These performance degradation models have been integrated in TAMTAMS.

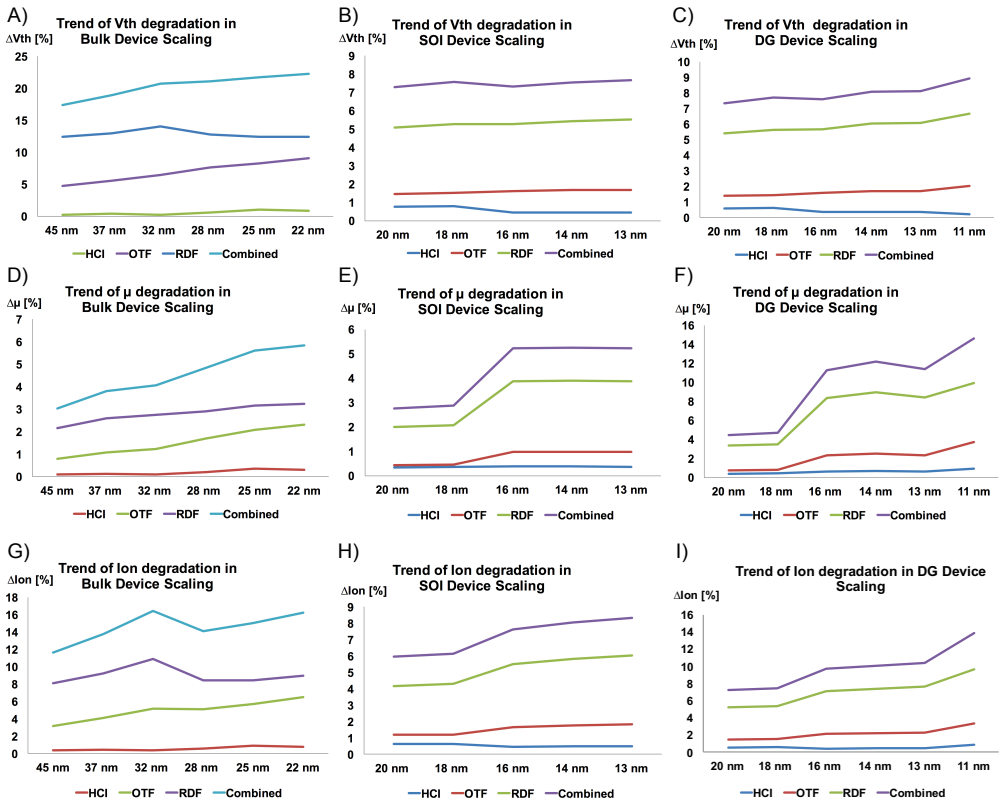

Figure 2. Trend of V_{th} , μ and I_{on} degradation on BULK, SOI and DG device scaling. A) Thresold voltage, D) Mobility and G) Drive current percentage degradation for BULK technology. B) Thresold voltage, E) Mobility and H) Drive current percentage degradation for SOI technology. C) Thresold voltage, F) Mobility and I) Drive current percentage degradation for DG technology. For each case, the variation considering HCI, OTF and RDF are reported alongside to the combined effect of all these contributions together.

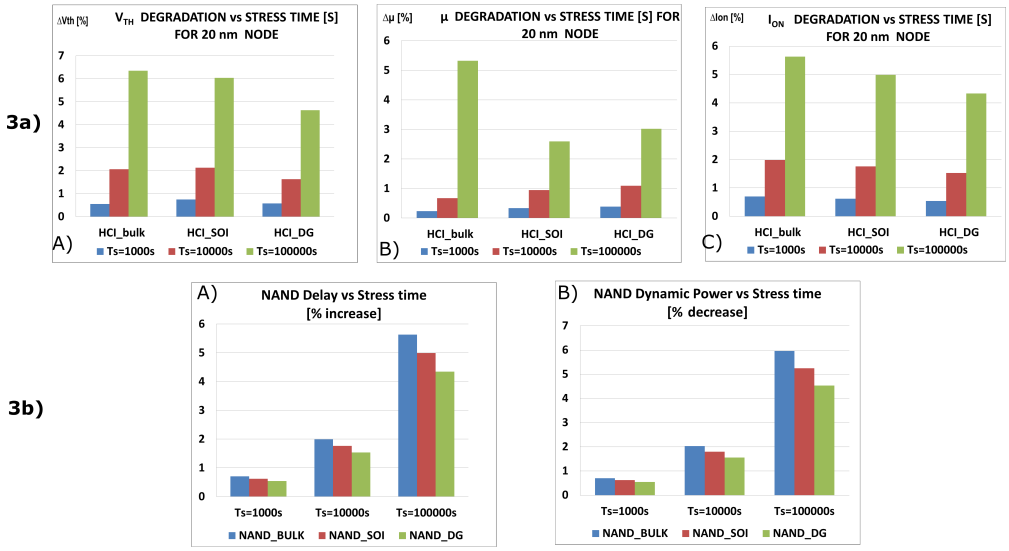

Figure 3. a)First Row: HCI induced performance degradation vs stress time for LOP 20 nm node for 3 different technologies. A) Threshold voltage, B) Mobility and C) Drive current percentage degradation. 3. b) Second Row: NAND2 gate time delay and dynamic power percentage degradation as a function of stress time 't' for LOP 20 nm BULK, SOI and DG technologies. A) Delay variation. B) Dynamic power variation.

3.2. Results (Device level)

In this section we discuss and analyze the performance degradation at device level relating to three different types of technologies, i.e. BULK, SOI and DG. The choice of different technologies not only contribute to different structures but also follow their scaling trend, e.g. the first node of LOP BULK technology analyzed is 45 nm and last node of LOP DG technology scales down to 11 nm. Two kind of analysis are considered: First analysis considers technology scaling across multiple types of transistors and nodes. Second one is a parametric analysis that focuses on one technology node and studies the variation in transistor's parameters like V_{th} , μ and I_{on} with time.

Fig. 2 shows the scaling trend for OTF, RDF and HCI induced degradation for Low operating Power (LOP) BULK, SOI and DG transistor technologies. It is to be noted that both static and dynamic models are analyzed together, because according to Alam [19] spatial and dynamic variations should be considered within the same framework. In Fig. 2, technologies are listed column-wise with BULK technology in Fig. 2.A-D-G, SOI in Fig. 2.B-E-H and DG in Fig. 2.C-F-I. The shift in V_{th} , μ and I_{on} are plotted in rows with V_{th} in the first row, μ in the second row and I_{on} third row. All variations are shown in relative units (%) and represent how much each quantity (V_{th}, μ and I_{on}) varies comparing to their nominal values. For each case, the variation considering HCI, OTF and RDF are reported alongside the combined effect of all these contributions together. The larger picture bring in some interesting observations. Relative variations are maximum for BULK technology nodes. As expected, the scaling trend increases within the framework of same technology for all the three types of devices. Considering static models, RDF remains the major source of V_{th}, μ and I_{on} variability, as indicated by [4], with maximum V_{th} relative increase recorded as 12% for first node , i.e. LOP BULK 45 nm node (Fig. 2A), and maximum relative decrease in μ and I_{on} recorded as 9% for the last node, i.e. LOP 11nm DG technology node (Fig. 2F and 2I). Considering time-dependent model,it is interesting to note that HCI induced degradation is larger for SOI devices than DG. The reason is, in DG case the carriers flow close to the center of the device where the potential fluctuations introduced by the trapped charges are relatively small, resulting in a lower variability compared the SOI device where the transport occurs close to the top interface and device is more affected by potential fluctuations [20].

Fig. 3.a) depicts the variations of V_{th}, μ and I_{on} at room temperature with increasing time. Fig. 3.a) shows HCI induced time-dependent variations V_{th}, μ and I_{on} remains below 1% for all the nodes under consideration, for a period of 10^3 stress seconds. It can be seen in Fig. 3.a) that as the devices are exposed to longer period of stress time t_s , from 10^3 to 10^5 the degradation becomes more severe. Fig. 3.a) shows the performance degradation as function of stress time t_s, considering LOP 20 nm as reference node for all the three technologies. BULK devices are more affected as compare to the other two. For BULK, degradation in V_{th} is 0.5% at $t_s = 10^3$, it increases to 2% at $t_s = 10^4$, and it reaches 6.35% at $t_s = 10^5$ (Fig. 3a.A). Similarly, maximum degradation in V_{th} of 6.04% and 4.63% are recorded for SOI and DG technology respectively at $t_s = 10^5$ (Fig. 3a.A). According to Alam [19], time-induced variation can be larger than the nominal degradation by more than 34% in 3 years lifetime. It has been observed that nominal shift remains near constant throughout different technologies. This is mainly due to relaxed oxide scaling but relative magnitude of V_{th} variation increases with technology scaling.

4. FROM DEVICE LEVEL TO GATE LEVEL

After detailed analysis of degradation of performance metrics at device level arising from intrinsic fluctuation and charge trapping, we have observed how the primary performance parameters like V_{th} and μ are affected. In the following, we consider their impact at gate level.

4.1. Description of NAND gate model

Reliability aware gate level analysis is interesting in a way that NAND gate is considered as universal building block for all high level CMOS circuits. Since the threshold voltage directly affects the delay of a digital gate, the operating frequency of the gate degrades, which in-turn affect the dynamic power consumption [21]. Mathematically putting:

$$\tau = f(V_{th}), Frequency, F = 1/\tau, Dynamic\ Power, P_{dyn} = f(F).$$

The delay analysis of the NAND gate is implemented exploiting the Elmore Delay model [22], considering its easy implementation and optimistic results. Here, the shift in V_{th} is translated into an increase in resistance that affects the time delay. On the other hand, the dynamic power consumption for NAND2 gate is estimated considering the probabilistic model that can be expressed as:

$$Dynamic\ Power, P_{dyn} = \frac{1}{2}\ f\ C\ \alpha\ V_{dd}^2 \qquad [W],$$

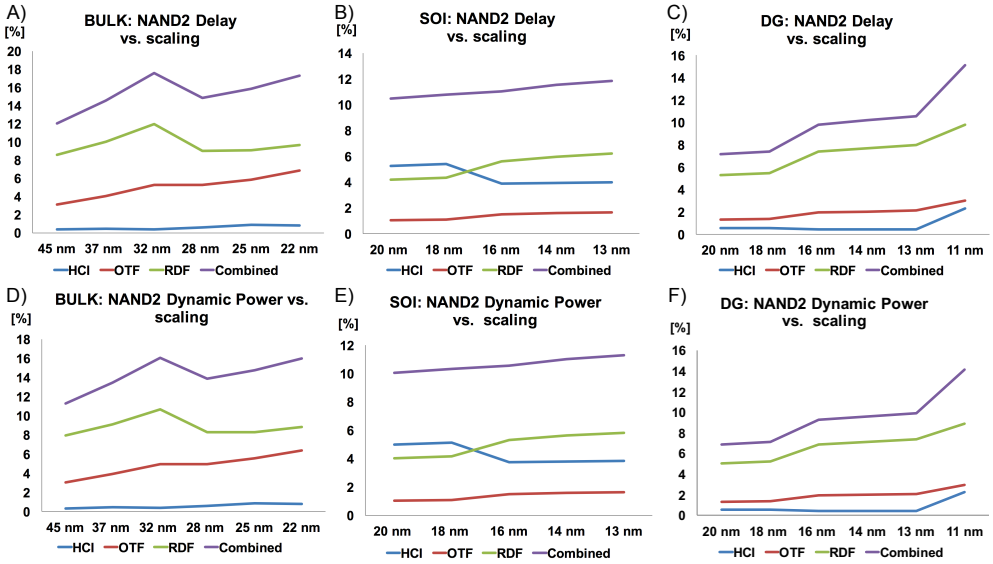

Figure 4. NAND2 gate time delay and dynamic power percentage variation trend with BULK, SOI and DG scaling. A) and D) depicts respectively delay and dynamic power variation for BULK technology. B) and E) depicts respectively delay and dynamic power variation for SOI technology. C) and F) depicts respectively delay and dynamic power variation for DG technology.

where α is the switching activity, f is the frequency and C is the total capacitance. In order to get simplified analysis, two assumptions were made: i) The input probability is always considered as 0.5 . ii) The computation of the switching activity for every single node is based on a probabilistic model. Further details on the model are not reported for space reasons. Considering reliability degradation, we assume all other parameters in above equation are unaffected by shift in V_{th}; thus P_{dyn} becomes the function of $frequency$ only. The frequency change $[\Delta F/F]$ in a circuit is measured as a direct measure of the degradation, which is proportional to V_{th} change under HCI [21].

4.2. Results (Gate level)

Fig. 4 shows degradation scaling trend of time delay and dynamic power for 2-input NAND gate. Gate delay increases due to the variation, while maximum dynamic power decrease accordingly. It is possible to observe a projection of the results analyzed at device level. BULK transistor based NAND gate is more exposed to static and dynamic degradation when compared to the other technologies (see Fig. 4.A and Fig. 4.D). The change in V_{th} directly affects the time delay in a digital gate [21], so the effect is more monotonic with the trend of V_{th} degradation scaling plots. Dynamic power degradation trend is similar to the delay, because dynamic power depends upon the operating frequency which is the inverse of critical path delay. As at device level analysis, RDF is contributing the major part of total degradation. In Fig. 4, it is interesting to see that HCI induced degradation is higher for SOI technology [20], with maximum time delay and dynamic power degradation reported as 5.3 % and 5.11 % respectively for LOP 18 nm node at stress time $t_s = 10^3$ (Fig. 4B and 4E), as compared to [0.56%, 0.56%] for same LOP 18 nm DG technology (Fig.4C and 4E). This shows, how the relative degradation is affected not only due to scaling of transistors, but with device structure as well [20].

Temporal shift of gate level performance degradation parameters are shown in Fig. 3b.A) (delay) and Fig. 3b.B) (maximum dynamic power). Degradation in dynamic power is the replication of time delay plots as expected, with the former plotted as % decrease. HCI induced degradation increases with increase in stress time, validating the accuracy of integrated modules. Maximum relative variation estimated for time delay is 5.5 % for 20 nm LOP BULK technology as compared to 5 and 4.3 % for SOI and DG technologies (Fig. 3.bA). In order to mitigate the impact of HCI induced variations at gate level, V_{dd} tuning and PMOS sizing are the most effective techniques. The authors in [23] shows that as much as 12 % oversizing of gate is needed across five years of operations.

5. CONCLUSIONS

In this paper we have presented a detailed analysis of MOSFET performance degradation considering the effects of Oxide Thickness Fluctuation (OTF), Random Dopant Fluctuation (RDF) and Hot-carrier-Instability (HCI).

The work here described is unique in its genre because it does a coherent analysis from transistor to circuit level. The analysis is carried on considering several types of transistor, considering the technology scaling and for the HCI effect, considering also the time evolution. The work was carried on under the TAMTAMS framework, an open tool designed to help researchers and student to understand technologies based on transistors.

As a future work, we are extending our analysis to system level by introducing digital circuits like adders, multipliers,FPGA, ALU , FIR filter models and different other chip layouts in the analysis as well. Secondly, additional effects that degrades the performance of transistors, like NBTI and electromigration would be interesting to analyze. We are also adding more models to the tool and more technologies, extending the analysis to emerging technologies and Post-Si devices.

REFERENCES

[1] "International Technology Roadmap of Semiconductors," 2015, http://www.itrs2.net/.
[2] C. H. Jan, F. Al-amoody, H. Y. Chang, T. Chang, Y. W. Chen, N. Dias, W. Hafez, D. Ingerly, M. Jang, E. Karl, S. K. Y. Shi, K. Komeyli, H. Kilambi, A. Kumar, K. Byon, C. G. Lee, J. Lee, T. Leo, P. C. Liu, N. Nidhi, R. Olacvaw, C. Petersburg, K. Phoa, C. Prasad, C. Quincy, R. Ramaswamy, T. Rana, L. Rockford, A. Subramaniam, C. Tsai, P. Vandervoorn, L. Yang, A. Zainuddin, and P. Bai, "A 14 nm soc platform technology featuring 2nd generation tri-gate transistors, 70 nm gate pitch, 52 nm metal pitch, and 0.0499 um2 sram cells, optimized for low power, high performance and high density soc products," in *2015 Symposium on VLSI Technology (VLSI Technology)*, June 2015, pp. T12–T13.
[3] NVIDIA. [Online]. Available: http://www.nvidia.com/object/gpu-architecture.html
[4] J. Velamala, C. Wang, R. Zheng, Y. Ye, and Y. Cao, *Intrinsic variability and reliability in nano-CMOS*, 4th ed., 2011, vol. 35, pp. 353–367.
[5] K. Bernstein, D. J. Frank, A. E. Gattiker, W. Haensch, B. L. Ji, S. R. Nassif, E. J. Nowak, D. J. Pearson, and N. J. Rohrer, "High-performance cmos variability in the 65-nm regime and beyond," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 433–449, July 2006.
[6] H. Kufluoglu and M. A. Alam, "A geometrical unification of the theories of nbti and hci time-exponents and its implications for ultra-scaled planar and surround-gate mosfets," in *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, Dec 2004, pp. 113–116.
[7] E. Maricau, P. D. Wit, and G. Gielen, "An analytical model for hot carrier degradation in nanoscale cmos suitable for the simulation of degradation in analog ic applications," *Microelectronics Reliability*, vol. 48, no. 89, pp. 1576 – 1580, 2008, 19th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2008).
[8] C. Zhuo, K. Chopra, D. Sylvester, and D. Blaauw, "Process variation and temperature-aware full chip oxide breakdown reliability analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 9, pp. 1321–1334, Sept 2011.
[9] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, "Compact modeling and simulation of circuit reliability for 65-nm cmos technology," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 4, pp. 509–517, Dec 2007.
[10] Y. Wang, S. Cotofana, and L. Fang, "Analysis of the impact of spatial and temporal variations on the stability of {SRAM} arrays and the mitigation technique using independent-gate devices," *Journal of Parallel and Distributed Computing*, vol. 74, no. 6, pp. 2521 – 2529, 2014, computing with Future Nanotechnology. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0743731513001354
[11] Riyadi, M. A, Sukawati, I. D, Prakoso, Teguh, and Darjat, "Influence of gate material and process on junctionless fet subthreshold performance," *International Journal of Electrical and Computer Engineering*, vol. vol.6, 2016.
[12] Jung, H. Kee, Dimitrijev, and Sima, "The impact of tunneling on the subthreshold swing in sub-20 nm asymmetric double gate mosfets," *International Journal of Electrical and Computer Engineering*, vol. vol.6, 2016.
[13] Dargar, S. Kant, Srivastava, JK, Bharti, Santosh, Nyati, and Abha, "Performance evaluation of gan based thin film transistor using tcad simulation," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. vol.7, pp. 144–151, 2017.
[14] B. Mehrdel, A. A. Aziz, Ghadiri, and M. Hossein, "Effect of device variables on surface potential and threshold voltage in dg- gnrfet," *International Journal of Electrical and Computer Engineering*, vol. vol. 5, 2015.
[15] B. Srinivasu and K. Sridharan, "Reliability analysis of full adder in schottky barrier carbon nanotube fet technology," in *14th IEEE International Conference on Nanotechnology*, Aug 2014, pp. 274–277.
[16] ST-Microelectronics, "MASTAR (Model for Assesment of CMOS Technologies And Roadmaps)," available on ITRS website.

[17] D. Sylvester and K. Keutzer, "System Level Performance Modeling with BACPAC, Berkeley Advanced Chip Performance Calculator," *proc. of IEEE SLIP*, pp. 109–114, 1999.
[18] F. Riente, I. Hussain, M. R. Roch, and M. Vacca, "Understanding cmos technology through tamtams web," *IEEE Transactions on Emerging Topics in Computing*, vol. 4, no. 3, pp. 392–403, July 2016.
[19] K. Kang, S. P. Park, K. Roy, and M. A. Alam, "Estimation of statistical variation in temporal nbti degradation and its impact on lifetime circuit performance," in *2007 IEEE/ACM International Conference on Computer-Aided Design*, Nov 2007, pp. 730–734.
[20] B. Cheng, A. R. Brown, S. Roy, and A. Asenov, "Pbti/nbti-related variability in tb-soi and dg mosfets," *IEEE Electron Device Letters*, vol. 31, no. 5, pp. 408 – 410, May 2010.
[21] R. Reis, Y. Cao, and G. Wirth, *Circuit Design for Reliability*. Springer New York, 2016.
[22] R. Gupta, B. Tutuianu, and L. T. Pileggi, "The elmore delay as a bound for rc trees with generalized input signals," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 1, pp. 95–104, Jan 1997.
[23] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and minimization of pmos nbti effect for robust nanometer design," in *2006 43rd ACM/IEEE Design Automation Conference*, July 2006, pp. 1047–1052.

BIOGRAPHIES OF AUTHORS

Izhar Hussain received his B.Sc. degree in Electronics Engineering from UET Peshawar, Pakistan in 2008. He received his M.Sc. degree in Nanotechnologies for ICTs in October 2014 from Politecnico di Torino, Italy and enrolled in the same university as Ph.D. student in November 2014. Since then, he has been active in research activities with VLSI group in the Department of Electronics and Telecommunications, Politecnico di Torino. His research area includes Modelling and Characterization of CMOS nano-transistors and emerging devices.

Marco Vacca Marco Vacca received the Dr.Eng. degree in electronics engineering from the Politecnico di Torino, Turin, Italy, in 2008. In 2013, he got the Ph.D. degree in electronics and communication engineering. He is currently working as an Assistant Professor in the Politecnico di Torino. Since 2010, he has been teaching Design of Digital Circuits and Power Electronics. His research interests include quantum-dot cellular automata and others beyond-CMOS technologies.

Fabrizio Riente received the M.Sc. (Hons.) (magna cum laude) degree in electronics engineering from the Politecnico di Torino, in 2012, where he is currently pursuing the Ph.D. degree with the Department of Elec-tronics and Telecommunications. His primary research interests are device modeling, circuit design for nanocomputing, with a particular interest in magnetic QCA, and silicon nanowire technologies. His interest also covers the development of EDA tool for emerging technologies, with the main focus on the physical design.

Mariagrazia Graziano received the Dr.Eng. and the PhD degrees in Electronics Engineering from the Politecnico di Torino, Italy, in 1997 and 2001, respectively. Since 2002, she is a researcher and since 2005, an assistant professor at the Politecnico di Torino. Since 2008, she is adjunct faculty at the University of Illinois at Chicago and since 2014 she is a Marie-Skodowska-Curie Intra-European Fellow at the London Centre for Nanotechnology. Her research interests include design of CMOS and beyond CMOS devices, circuits and architectures.She is author and coauthor of more than 120 published works. She is a Member of the IEEE since 2007.