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Flux–Charge Memristor Model for Phase Change Memory

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***Abstract*—Phase-Change Memory (PCM) is one of the most promising non-volatile memory technologies and is finding applications in areas such as storage-class memory and emerging non-von Neumann computing systems. Even though powerful physics-based models have been developed for these devices, there is a lack of simple and accurate circuit models to describe these elements. In this work we exploit *memristor theory* to obtain a simple and reliable circuit model based on electrical variables such as *charge* and *flux*. This model is based on experimental measurements of PCM devices fabricated in the 90 nm technology node.**

***Index Terms*—Phase–Change Memory, Memristor, Flux–Charge Model, non-von Neumann computing**

I. Introduction

PHASE-change memory (PCM) is arguably the most advanced among emerging non-volatile memory technologies [1]. PCM has emerged as a promising candidate to bridge the performance gap between the main memory and storage in computing systems typically referred to as storage-class memory [2], [3]. More recently PCM has also found application in non-von Neumann computational paradigms such as neuromorphic computing and memcomputing [4]–[6].

The phase change memory concept is based on the reversible phase change of materials such as $Ge_2Sb_2Te_5$ (GST) from the ordered crystalline phase to the disordered amorphous phase. The resistance of PCM devices depends on the amorphous-crystalline phase configuration. The PCM device exhibits a rich dynamic behavior and is described by an interconnection of electrical, thermal and structural dynamics. There is significant on-going research on understanding this dynamics and physics-based models are being developed [7]–[9].

In parallel, significant developments were also being made in the theory of memristive devices. *Memristors* are two–terminal nonlinear circuit elements capable of changing and maintaining the resistive state depending on the "whole history" of the voltage applied to and/or the current flowing through the device [10], [11]. The integrals between $-\infty$ and t of the voltage and of the current represent the voltage momentum (a.k.a *flux* φ) and current momentum (a.k.a. *charge* q), respectively [12]. Since a pinched v–i curve is found to be just the response to a specific input (i.e. a mathematical description of memristor v–i curves is not a circuit model), a comprehensive classification of memristor devices in terms of flux–charge electrical variable is provided [12]. One such example of a flux–charge model of TiO_2 memristor devices can be found in [13].

Given the behavioral similarity between PCMs and memristors, it will be of significant interest to develop a φ–q memristor model for PCMs thus connecting the research activities in these two hither-to distinct fields. This will also have significant practical ramifications such as having a simple and reliable analytical circuit model that can be included in standard circuit-level simulation tools. It can also benefit the emerging applications of PCMs in non-von Neumann computing.

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II. Physical description of phase change devices

A schematic illustration of a mushroom-type PCM device used for the experimental study is shown in Figure 1(a). The device was fabricated in the 90 nm technology node with a sub-lithographically defined bottom electrode. The phase change material is doped GST of approx. 100 nm thickness. In an as-fabricated device, the phase-change material is typically in the crystalline phase. To create an amorphous region, a voltage pulse of sufficiently high amplitude is applied to the device. The resulting Joule heating melts a substantial portion of the phase-change material. If the voltage pulse is stopped abruptly, the molten material quenches into the amorphous phase due to glass transition. The effective thickness of the amorphous region is denoted by u_a. The amorphous phase blocks the bottom electrode and the device is in a high resistance state referred to as the RESET state.

A characteristic DC I–V behavior of the PCM cell in the RESET state is shown in Figure 1(b). The electrical transport in amorphous phase change materials has a strong field dependence [14], [15]. However, for the sake of simplicity, we assume that at low and intermediate fields, the transport is fairly Ohmic. Hence the electrical resistance is given by

$$R(u_a(t)) = \frac{\rho}{\pi r_E^2} u_a(t) \tag{1}$$

where $\rho = 0.1\,\Omega$m is the low-field resistivity of melt-quenched amorphous GST and $r_E = 20nm$ is the effective radius of the bottom electrode. However, beyond a certain bias voltage denoted by V_{th}, the amorphous phase change material goes into a low resistance state. This phenomenon is known as threshold switching, the physical origins of which is being actively researched to-date [16], [17]. In our devices, for a $u_a \approx 50$ nm, V_{th} is approximately equal to 1.25 V. Note that this is a purely an electronic phenomenon and the phase

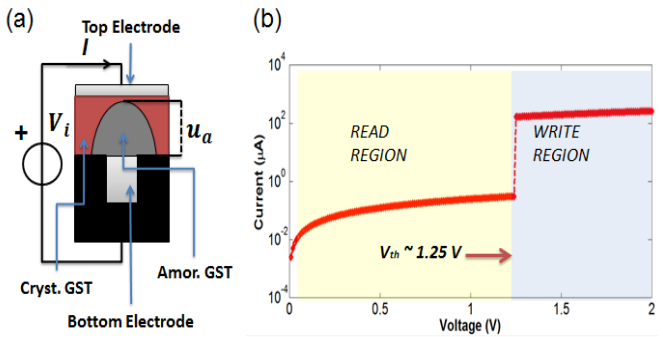


Fig. 1. (a) Schematic representation of a mushroom-type PCM device. In the RESET state, the phase change material in the amorphous phase blocks the bottom electrode and the device is in high resistance state. The effective thickness of the amorphous region is denoted by u_a. V_i denotes the voltage applied to the device and I denotes the resulting current flowing through the device. (b) A characteristic I-V behavior is shown. It can be seen that above the threshold switching voltage (V_{th}), the device exhibits a much lower resistance even in the RESET state. The READ and WRITE regions of the $I-V$ curve are shaded in yellow and blue respectively.

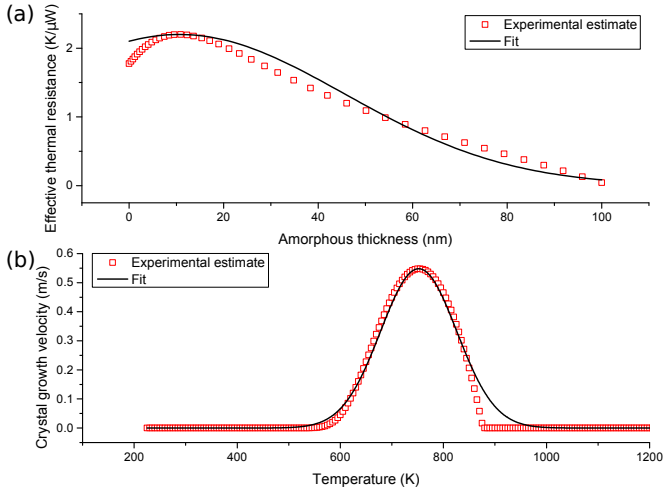


Fig. 2. Experimentally obtained estimate of (a) the effective thermal resistance as a function of the amorphous thickness and (b) the temperature dependence of crystal growth velocity. T_M is the melting temperature of the GST, and from that point on the growth velocity can be considered negligible. Also shown are analytical approximations.

change material is still in the amorphous phase. The resistance of the device drops to an ON-state resistance value of $\approx 7.5\text{k}\,\Omega$ which is mostly independent of the thickness of the amorphous region.

To induce amorphous to crystalline phase transition, voltage pulses have to be applied to the PCM device such that the temperature reached within the cell is in the regime where there is substantial crystal growth at the amorphous-crystalline interface. To pass sufficiently large current through the device and thus induce sufficient Joule heating, it is imperative that the voltage pulses should have an amplitude $V_s \geq V_{th}$. These type of pulses that induce phase transition are referred to as write pulses.

When such write pulses are applied, the evolution of u_a is given by

$$\frac{du_a(t)}{dt} = -\int_{t_0}^{t} v_g(\tau)\, d\tau, \tag{2}$$

where v_g denotes the crystal growth velocity, $[t_0, t]$ corresponds to the time interval in which $v_i(t) = V_w \geq V_{th}$ is applied and $u_a(t_0)$ is the initial amorphous thickness. The value of v_g depends on the temperature at the amorphous-crystalline interface denoted by T given by

$$T(u_a(t)) = T_{amb} + R_{th}(u_a(t))\frac{V_w^2}{R_{on}} \tag{3}$$

$T(t)$ depends on the ambient temperature, T_{amb} as well as the temperature rise due to Joule heating. The latter in turn depends on the electrical power that is dissipated and the effective thermal resistance, R_{th} which is function of the GST thickness $u_a(t)$. $R_{th}(u_a)$ captures the thermal resistance of all possible heat pathways and naturally has a strong dependence on u_a. An estimate of $R_{th}(u_a)$ obtained via experimental means is presented in Figure 2(a) [9]. It shows that the hottest region within the mushroom-type PCM device is close to the bottom electrode while the top electrode is substantially cooler. What is also shown is an approximate analytical description of $R_{th}(u_a)$ given by

$$R_{th}(u_a(t)) \approx A_r \exp\left(-\frac{1}{2}\left(\frac{u_a(t)-\mu_r}{\sigma_r}\right)^2\right) \tag{4}$$

where A_r =2.2 K/μW, μ_r =10.62 nm and σ_r =32 nm.

In Figure 2(b), an experimentally obtained estimate of the temperature dependence of crystal growth velocity is shown [9]. At low temperatures, crystal growth is insignificant while the maximum occurs at a temperature of approximately 750 k. It is also not possible to crystallize beyond the melting temperature of $T_M \approx 900K$. An approximate analytical description of $v_g(T)$ can be obtained given by,

$$v_g(T(u_a(t))) \approx A_g \exp\left(-\frac{1}{2}\left(\frac{T(u_a(t))-\mu}{\sigma}\right)^2\right) \tag{5}$$

where A_g =0.548 nm/ns, μ =752 K, and σ =78 K.

III. Memristor Model for PCM devices

In this section accurate memristor models are developed for PCM devices based on the physical description presented earlier. It was recently shown that memristor devices can be grouped into three classes: ideal memristors, generic memristors and extended memristors [12]. The ideal memristor is defined by a nonlinear relationship $q = f(\varphi)$ corresponds to the original definition given by Prof. L. O. Chua [10]. Theorem 1 in [12] provides the necessary and sufficient condition to describe any memristor devices in term of both (φ, q) and (v, i). In addition, Theorem 2 in [12] specifies the whole class of ideal memristors (also named *memristor siblings*).

Under the assumption that Theorem 1 holds, let us consider a (flux–controlled) extended memristor described by (see [12] for further details):

$$q(t) = f(\varphi(t), u_a(t)) \quad \Rightarrow \quad i(t) = G(\varphi(t), u_a(t))v_i(t) \tag{6}$$

$$v_g(t) = g(v_i(t), u_a(t)) \quad \Rightarrow \quad v_g(t) = g(v_i(t), u_a(t)) \tag{7}$$

$$\dot{\varphi}(t) = v_i(t) \quad \Rightarrow \quad \dot{\varphi}(t) = v_i(t) \tag{8}$$

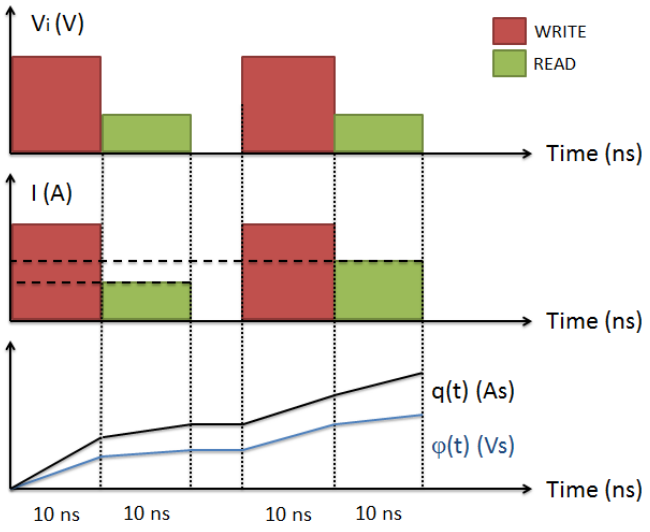


Fig. 3. Figurative example of an input voltage waveform, related to the output current and the respective flux $\varphi(t)$ and charge $q(t)$. The case shown is an example of constant writing voltage (V_w) inputs given to the PCM cell. From the graphs it is possible to note that $\varphi(t)$ and $q(t)$ are calculated as the sum of the areas of the input voltages and output currents respectively. From the last graph it is possible to see that the flux of the reading voltage (V_r) can be considered negligible with respect to the flux of V_w. On the other hand the charge of the current the reading phase increases at every input step.

where the left–hand side represents the flux–charge description and the right hand-side is the description in terms of the voltage and current. The Ohm's law is recognizable where the memconductance $G(\varphi(t), u_a(t))$ depends also on the internal memristor state variable $u_a(t)$ (GST thickness).

To investigate the mapping between the flux, charge and the interfacial temperature, Equations (2) and (3) were used to simulate the behavior of the PCM device when excited by appropriate voltage signals. These signals comprise of two consecutive square pulses. The first is the writing pulse V_w which is set to an amplitude ranging from 1.25 V to 2 V, with a 0.05 V step, and a duration of 10 ns. The second is a reading pulse V_r which has the scope to not modify the amorphous GST thickness, so is set to an amplitude of 0.05 V which is lower than V_t. The duration of V_r is set to $10\,ns$. The duration of the writing and reading impulses respectively were chosen in order to consider the increase of the flux (φ) given by V_r negligible with respect to the voltage momentum increase given by V_w. The ambient temperature is 300 K. The simulations were conducted to study the various scenarios such as

(i) $v_i(t)$ increasing ramp, i.e. constant increase of the V_w in ten steps;
(ii) $v_i(t)$ decreasing ramp, i.e. constant decrease of the V_w in ten steps;
(iii) $v_i(t)$ triangular waveform, i.e. V_w increases in five steps and decreases in five steps;
(iv) with ten inputs of constant amplitude with V_w ranging from 1.25 V to 2 V, with a 0.05 V step.

In Figure 3 is presented a figurative example of an input voltage waveform and the resulting output current respectively related to the momentums generated. $\varphi(t)$ and $q(t)$ can be calculated as the sum of the areas below the curves. From the same figure it is possible to note how the flux of V_r does not significantly increases the overall momentum given by V_w. On the other hand, considering $q(t)$, as expected, the charge calculated from the output current read in the reading phase increases at each input step.

In the simulations previously described were computed the flux ($\varphi(t)$), the charge ($q(t)$), the interface temperature ($T(t)$) resulting from the application of the writing impulse (V_w) and the amorphous thickness ($u_a(t)$). The data obtained was interpolated in order to find the relationships between φ, q and u_a. Figure 4 and Figure 5 show the interpolating surface and the interpolating lines respectively highlighting the relations amongst the three variables. From the data obtained it is possible to derive the following relationship between φ and T taking into account T_M and the *initial temperature* $T_0 = R_{th}(u_a(t_0))V_w^2/R_{on} + T_{amb}$ of the PCM,

$$\frac{T(\varphi) - T_0}{\xi} = \operatorname{erf}\left(\frac{k}{\xi}\varphi\right), \tag{9}$$

where $\xi = (T_M - T_0)$ and the constant $k = 2 \cdot 10^{-9}$ K/Vm. Expression (9) is a direct consequence of the integration of the Gaussian functions used to approximate $R_{th}(u_a(t))$ and $v_g(t)$ (i.e. equations (4) and (5)). Through the same equation it is possible to formulate the relationship between $u_a(t)$ and φ in terms of temperature as

$$\frac{u_a(\varphi) - u_{a0}}{\lambda} = -\operatorname{erf}\left(\frac{T(\varphi)}{T_M} - 1\right), \tag{10}$$

where $\lambda = v_g(T_0)k_1$ and k_1 =1 s/nm. The value $v_g(T_0)$ is the crystal growth velocity, and u_{a0} is the GST thickness at the time point t_0 and the first can be calculated from equation (5). It turns out that (10) corresponds to the solution of equation (7) describing the dynamics of the internal memristor variable and takes into account the GST thickness $u_a(t)$. Furthermore the expression (10) takes also into account from equation (9) the diffusion phenomena between two bodies of different temperature (T_0 and T_M). Moreover from the same equation it is possible to note that the interface temperature T_0 is to be considered as *hidden variable* according to [12].

From what above described, the relationship between φ and q results to be:

$$q(\varphi) = Q_0\varphi \exp\left(\alpha T_M\left(1 - \operatorname{erf}^{-1}\left(\frac{u_a(\varphi) - u_{a0}}{\lambda}\right)\right)\right). \tag{11}$$

where $Q_0 = k\beta\exp(-T_0\alpha)$, β =$1 \cdot 10^{-13}$ KAs/Vm and α =$1 \cdot 10^{-3.5}$ K^{-1}. As a proof that equations (10) and (11) adequately describe the behavior of the PCM cell, a fitting test has been performed between the data obtained from the simulation and the analytical results. The test has returned a reliability factor $R^2 = 0.944$, which denotes an accurate matching between the simulated behavior and the memristor model (10)–(11). Equation (11) is valid for $\varphi \geq 0$ since from equation (3) the interface temperature depends on V_w^2. From this consideration the PCM cell can be considered as an unipolar element. Moreover it is worth noting that the variable

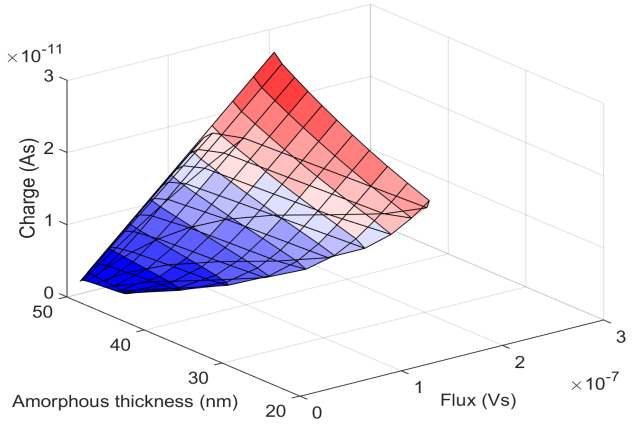


Fig. 4. Surface interpolating the experimental data in the (φ, q, u_a)–domain. The solid black lines highlight the curves that show the actual relationship built through the interpolation of the data obtained from all the simulations.

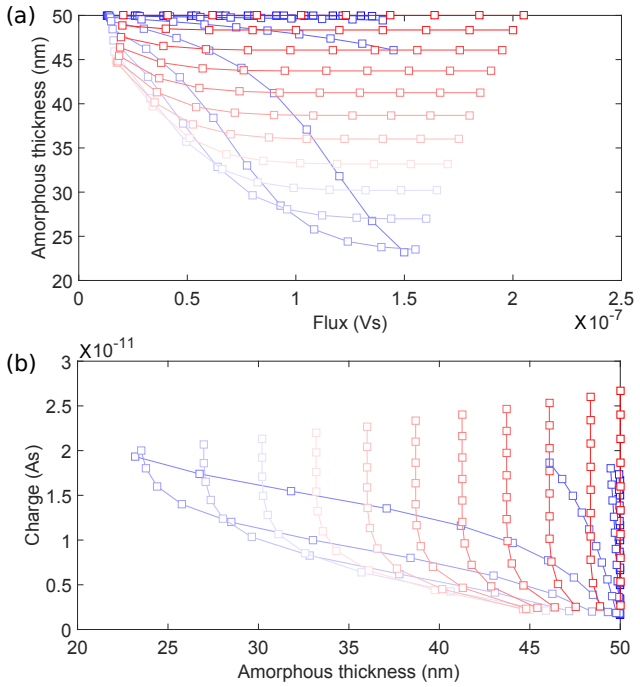


Fig. 5. Interpolating lines derived from the (φ, q, u_a) surface in Figure 4. (a) Interpolating lines that show the family of curves describing $q(u_a(t))$ and (b) $\varphi(u_a(t))$ obtained from the simulations.

$u_a(\varphi)$ in the PCM memristor model given in equation (11) is limited in the range $[0, 100\,\mathrm{nm}]$ due physical characteristics. In addition the same equation (11) expresses the charge as only function of the flux, i.e. the PCM turns out to be an ideal (sibling) memristor as described at the beginning of this Section (III).

IV. Conclusion

PCM technology is a leading non-volatile memory technology that could play a key role in future memory and computing systems. There is a significant understanding of the dynamics of PCM devices which is governed by an interconnection of electrical, thermal and structural dynamics. Even though the PCM devices exhibit significant behavioral similarity with other memristive devices, there have been no attempts at developing a flux-charge based memristor model for PCM devices. In this article, such a φ–q model is derived based on experimentally obtained estimates of the temperature dependence of crystal growth and the thickness dependence of temperature distribution within a mushroom–type PCM device.

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