Fully Synthesizable, Rail-to-Rail Dynamic Voltage Comparator for Operation down to 0.3V

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***Abstract*— A novel rail-to-rail dynamic voltage comparator is presented in this paper. The proposed circuit is fully synthesizable, as it can be designed with automated digital design flows and standard cells, and can operate at very low voltages down to deep sub-threshold. Post-layout simulations show correct operation for rail-to-rail common-mode inputs at a supply voltage V_{DD} down to 0.3 V. At such voltage, the input offset voltage standard deviation is less than 28 mV (8 mV) over the rail-to-rail common-mode input range (around V_{DD}/2). The digital nature of the comparator and its ability to operate down to deep sub-threshold voltages allow its full integration with standard-cell digital circuits in terms of both design and voltage domain. The ease of design, the low area and the voltage scalability make the proposed comparator very well suited for sensor nodes, integrated circuits for the Internet of Things and related applications.**

Keywords*— *Dynamic voltage comparator, fully synthesizable, ultra-low voltage, standard-cell design.

I. INTRODUCTION

Dynamic voltage comparators (DVCs) are key building blocks of analog-to-digital converters (ADCs), sensor interfaces for physical data acquisition and event monitoring, and sensor nodes for the Internet of Things (IoT), among the others [1]. Even if a wide range of solutions have been proposed to implement DVCs (see, e.g., [2-4]), their supply voltage is typically 0.6 V and above, making them unsuitable for ultra-low power systems such as sensor nodes and energy harvested systems. Also, they usually need to be designed in a custom fashion, and their layout needs to be kept separate from the digital standard cell-based modules they drive, thus requiring additional effort for block design and system integration.

The above limitations recently motivated a wider interest in digital implementation of analog functions over the last years [4-6]. In the specific case of DVCs, the only available example of fully synthesizable circuit was proposed in [5] and is depicted in Fig. 1. This circuit is completely based on CMOS digital standard cells, and is attractive for its fully synthesizability and very low area. Unfortunately, its limitations make it suitable for a narrow range of applications, restricting its adoption to stochastic A/D conversion [5-6]. In detail, one of the major drawbacks of the DVC in [4] is its very narrow common-mode input range (CMR), which makes it unusable in many circuits that require a DVC, such as Flash ADCs and successive-approximation-register (SAR) ADCs featuring energy-efficient switching schemes [7], where the common-mode (CM) input voltage is not constant. To address the CMR limitations of the DVC introduced in [5], a novel fully-synthesizable dynamic voltage comparator with rail-to-rail CMR (RRDVC) is proposed

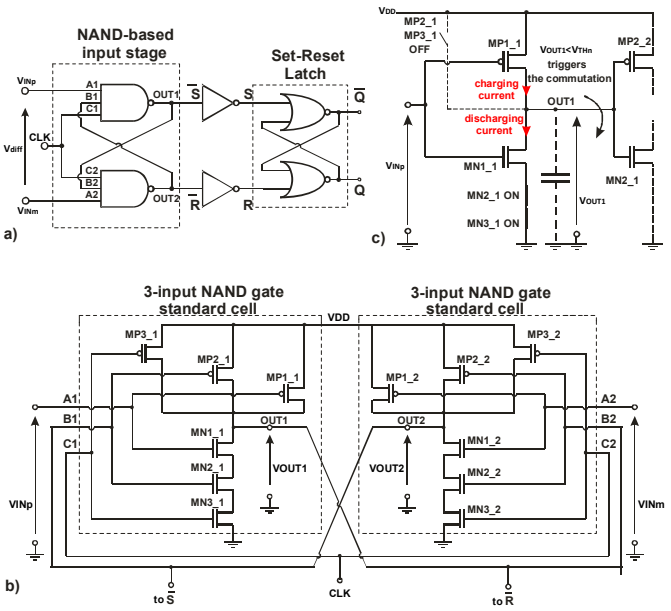

Fig. 1. Fully synthesizable DVC with NAND3-based input stage (NAND3-DVC) in [5] along with a) gate-level structure, b) transistor-level detail of the NAND-based input stage, c) simplified schematic OUT1 commutation.

in this paper. The proposed DVC is shown to be able to operate at deep sub-threshold voltages (e.g., 0.3 V). As opposed to [5], the proposed DVC is compatible with the requirements of medium-low resolution fully digital ADCs.

The paper is structured as follows. The CMR limitation of the DVC in [5] is firstly analyzed in Section II. The proposed DVC topology is then introduced in Section III to overcome this limit. Its performance is analyzed in Section IV via post-layout simulations, and compared with the state of the art. Concluding remarks are finally drawn in Section V.

II. REVIEW OF PRIOR FULLY-SYNTHESIZABLE DYNAMIC VOLTAGE COMPARATOR AND LIMITATIONS

The NAND3-DVC proposed in [5] and depicted in Fig. 1a is made up of an input stage comprising two NAND3 gates (see its schematic in Fig. 1b) and an SR latch. The top inputs A1 and A2 of the NAND3 are tied to the gates of the top nMOS devices (MN1_1 and MN1_2), and are connected to the non-inverting (v_{INp}) and inverting (v_{INm}) analog inputs of the DVC. The middle input B1 (B2) drives the NMOS transistor MN2_1 (MN2_2), and is fed by the output OUT2 (OUT1) in a cross-coupled fashion. The bottom inputs C1 and C2 are connected to the sampling clock, as in Fig. 1b. The outputs OUT1 and OUT2

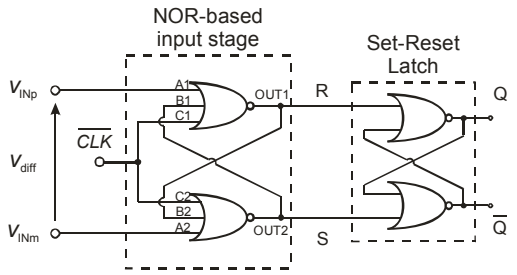

Fig. 2. Fully synthesizable DVC with NOR-based input stage (NOR3-DVC) with a CMR including ground (gate-level structure).

are also connected to the set (S) and reset (R) inputs of the SR latch through inverter gates. The latter ones keep hold the previous comparator output when the sampling clock is at the low level (i.e., when the comparator is inactive). In this case, OUT1 and OUT2 are precharged to V_{DD} by transistors MP3_1 and MP3_2, and transistors MN2_1, MN2_2 are on due to the cross-coupled feedback connection.

The sampling phase occurs at the low-to-high clock transition, when transistors MP3_1 and MP3_2 are turned off, thus disabling the precharge of OUT1 and OUT2, while transistors MN3_1 and MN3_2 are turned on, thus enabling the pull-down networks of the two NAND gates since MN2_1 and MN2_2 are still on immediately after the rising clock edge, as OUT1 and OUT2 are still at V_{DD}. Successively, the output OUT1 is pulled down by transistor MN1_1 faster than OUT2, if the input differential voltage $v_{diff} = v_{INp} - v_{INm}$ is positive (since the gate voltage of transistor MN1_2 is lower than in MN1_1). Accordingly, OUT1 reaches V_{THn} before OUT2 reaches the same voltage, where V_{THn} is the threshold voltage of NMOS transistors. This turns off MN2_2 and triggers a positive feedback mechanism that forces OUT1 to be latched low, and OUT2 to be latched high. Opposite considerations hold if the input v_{diff} is negative. In both cases, the digital output is set by the polarity of the analog input differential voltage around the rising clock edge, as expected from a DVC, and is latched by the SR latch.

As an issue of the above DVC, the pulling down of OUT1 and OUT2 is countered by the drain currents of MP1_1 and MP1_2, which are also driven by the analog inputs. In particular, these currents oppose to the falling transient of OUT1 and OUT2 that would be naturally determined by MN1_1 and MN1_2 (see above). This phenomenon is negligible if the common-mode input voltage is close to V_{DD}, since MP1_1 and MP1_2 are off and their current is therefore very small. However, when the common-mode input voltage is reduced, the source-gate voltage of MP1_1 and MP1_2 increases, thus increasing their currents. The latter subtract from the currents sunk by MN1_1 and MN1_2, which decrease while reducing the common-mode voltage, thus making the pulling down of OUT1 and OUT2 more and more difficult (see detail of currents involved in the switching of the OUT1 node in Fig. 1c).

For excessively low common-mode voltages, the currents of MP1_1 and MP1_2 dominate over the currents MN1_1 and MN1_2, so that OUT1 and OUT2 forcibly remain at V_{DD} regardless of the input (i.e., the comparator stops operating correctly). In other words, the CMR is lower bounded by a voltage V_{N}, which is found to be about $V_{DD}/2$ from simulations.

III. Proposed Rail-to-Rail Fully-Synthesizable Voltage Comparator

The CMR limitations of the DVC in [5] can be overcome by adopting a different topology, while preserving full synthesizability, as discussed below. A rail-to-rail CMR can be achieved by observing that replacing the NAND gates in Fig. 1a by NOR gates (see Fig. 2) would lead to dual circuit operation. Repeating the above analysis after replacing NAND gates with NOR in Fig. 1a, the circuit in Fig. 2 can be found to have dual CMR limitations. Indeed, the comparator operates correctly only if the common-mode input voltage is close enough to ground, whereas it fails when the common-mode input goes beyond a maximum voltage V_P, which is again found to be about $V_{DD}/2$. For common-mode voltages above V_P, OUT1 and OUT2 cannot be properly pulled up and the comparator fails.

The opposite CMR limitations of NAND3- and NOR3-based DVCs suggest that a DVC with rail-to-rail CMR can be obtained by merging a NAND3- and a NOR3-based input stage. Intuitively, NAND3 gates can correctly operate for the portion of the CMR towards V_{DD}, and the NOR3 correctly operate for the portion towards ground. This extends the "complementary differential pair" concept (i.e., NMOS and PMOS) used in rail-to-rail operational amplifiers [9] to digital DVCs. Following the above idea, the input stages of a NAND3-based DVC and of a NOR3-based DVC have been merged as in Fig. 3a.

The outputs of the cross-coupled NAND3 and NOR3 drive a dual-input SR latch, with two "set" inputs S1 and S2 and two "reset" inputs R1 and R2, which are ORed as in the truth table in the Fig. 3c. As such, the correct operation of just one (i.e. the NAND3-based or the NOR3-based) input stage is sufficient to drive the SR latch correctly, if the signals from the other stage are stuck at their precharge level (i.e., when the other input stage is not able to generate a correct output).
When the common-mode input is closer to V_{DD} than ground, NAND3 gates operate correctly and generate the expected outputs S1 and R1. At the same time, NOR3 gates fail, as their outputs are stuck at the precharge value (i.e., ground).

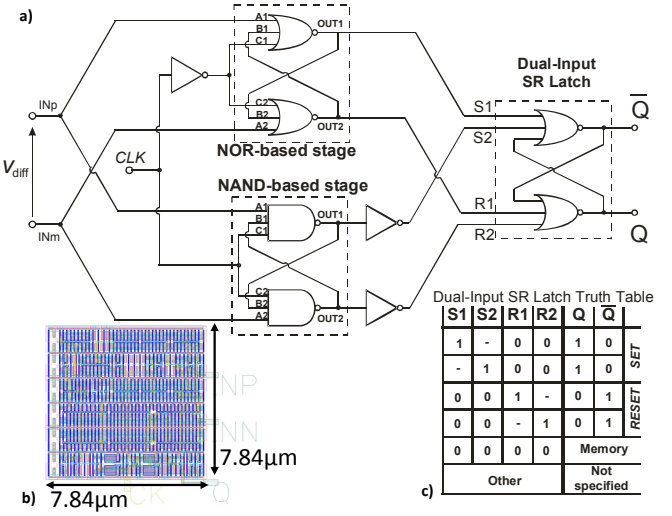

Fig. 3. Proposed fully-synthesizable RRDVC with complementary NAND/NOR input stage and Dual-Input SR latch: a) gate-level structure, b) automatically generated layout, c) truth table of the dual-input SR latch.

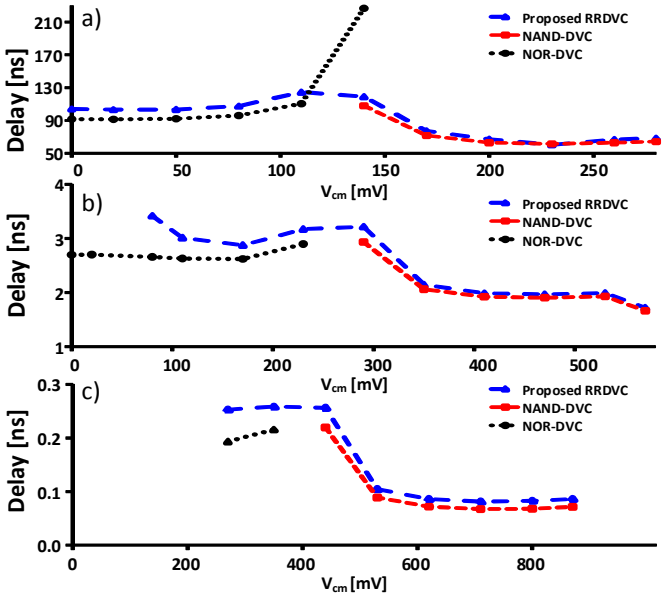

Fig. 4. Propagation delay vs. common-mode input voltage for the NAND3-DVCs, NOR3-DVCs and the proposed RRDVC for v_{diff}=5mV at a) V_{DD}=0.3 V, b) V_{DD}=0.6 V and c) V_{DD}=0.9 V.

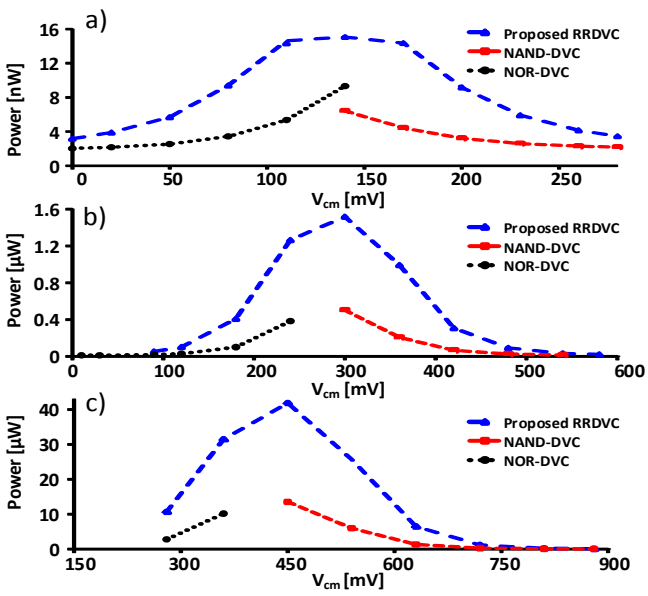

Fig. 5. Power consumption versus common-mode input voltage for a NAND3-DVC, for a NOR3-DVC and for the proposed RRDVC, for v_{diff} =5mV and for a) V_{DD}=0.3 V, b) V_{DD}=0.6 V and c) V_{DD}=0.9 V.

According to the above discussed operation of the dual-input SR latch, the latter stores the value provided by the NAND3 gates, while being unaffected by the output of the NOR3 gates. This assures correct operation under the CMR region towards V_{DD}. Opposite considerations hold when the common-mode input is closer to ground than V_{DD}. In this case, NOR3 gates operate correctly and provide the expected outputs S2 and R2, and the SR latch generates the correct output despite the outputs of the NAND3 gates are stuck at V_{DD}. Based on the above considerations, the proposed RRDVC is still fully synthesizable, and is expected to operate correctly across a much wider common-mode range, compared to the DVC in [5]. Moreover, its digital nature suggests that it can operate at lower voltages than conventional comparators.

IV. Validation and Circuit Simulations

The proposed RRDVC, the NAND3-DVC in [5] and the NOR3-DVC were designed and synthesized in 40nm, starting from a Verilog description. It is worth observing that the input offset voltage of all the considered DVC topologies is determined by the mismatch between the currents provided by the two NAND3 and/or NOR3. The cross-coupled NAND3 and NOR3 gates form a positive feedback loop with a large loop gain, which makes the effect of transistor mismatch in the SR latch insignificant. Accordingly, the input offset voltage was mitigated by employing the standard cell version of NAND3 and NOR3 with a strength of 16, as the maximum available in the available standard cell library. Such strength choice is a reasonable compromise as it makes the offset significantly smaller than minimum-sized cells due to Pelgrom's law [10], while keeping the area, the input capacitance and power low. In particular, the input capacitance was evaluated to be 5.1 fF for V_{DD} =0.6 V. Moreover, the area of the automatically generated layout, shown in Fig.3b, is only $62\mu m^2$. In practical cases, the comparator can be described in Verilog along with the subsequent digital block, and hence placed and routed as part of it.

The three DVC designs were compared by sweeping the common-mode input from rail to rail. Post-layout transistor-level simulations were performed at three different supply voltages covering above-threshold (V_{DD}=0.9V), near-threshold (V_{DD}=0.6V), and deep sub-threshold (V_{DD}=0.3V). The clock-to-output propagation delay of the three DVCs was evaluated for a differential input voltage of 5 mV across the entire rail-to-rail CMR.

The results reported in Fig. 4 show that the CMR of the proposed DVC, powered at V_{DD} =0.3V, covers the full rail-to-rail swing and is much wider compared to the conventional NAND3-DVC (NOR3-DVC), whose CMR is lower bounded by 0.125 V (upper bounded by 0.125V), as expected from the considerations in the previous section. The maximum clock-to-output delay of the proposed RRDVC for v_{diff}=5mV is found to be 250ps, 3 ns and 100 ns for a supply voltage of 0.9V, 0.6V and 0.3V, respectively. The maximum delay was achieved at a common mode input voltage of about $V_{DD}/2$. At other common-mode input voltages, this delay is lower and can differ from the above values by 30%, 20% and 10% at most, showing reasonable consistence across CMR.

The power consumption is reported in Fig. 5, and it is lower than 40µW, 1.5µW and 15nW for V_{DD} equal to 0.9V, 0.6V and 0.3V. The power was found to be dominated by a cross-conduction current during the on phase of the sampling clock. In detail, the power consumption is larger for common-mode input close to $V_{DD}/2$ as this maximizes the current flowing through both the pull-up and pull-down network of the NAND3 and NOR3 gates. This power is nearly independent of the sampling frequency, with a maximum 10% variation from DC frequency to the maximum sampling frequency dictated by the DVC delay.

The impact of the differential input voltage on the clock-to-output delay is analyzed in Fig. 6. This figure shows that the

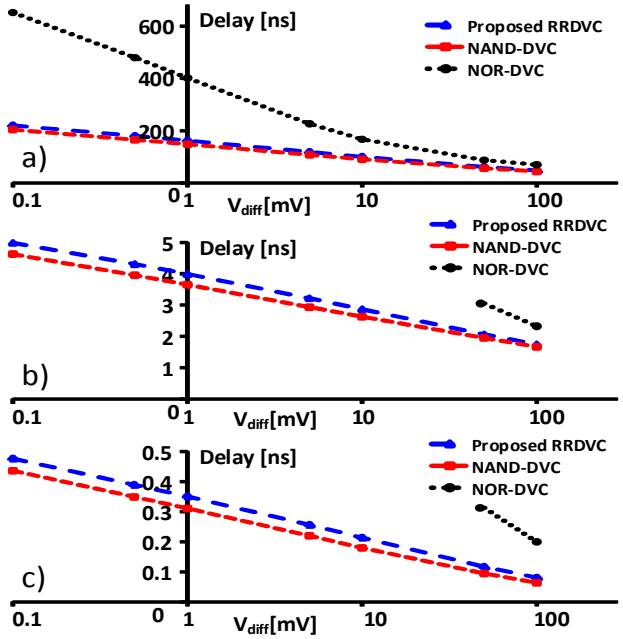

Fig. 6. Delay versus differential input voltage v_{diff} for a NAND3-DVC, for a NOR3-DVC and for the proposed RRDVC, operated at a) V_{DD}=0.3 V, b) V_{DD}=0.6 V and c) V_{DD}=0.9 V.

TABLE I.
PERFORMANCE COMPARISON

Parameters	This work			[3]	[4]	[5]
Design flow	fully digital			analog	analog	fully digital
Technology	CMOS 40nm			CMOS 130nm	CMOS 180nm	CMOS 40nm
Area [µm²]	62			N/A	N/A	35
V_{DD} [V]	0.9	0.6	0.3	1.2	1.8	0.6
CMR (min-max [V])	0.2-0.9	0.1-0.6	0-0.3	0.4 -1.2	0 - 1.8	0.4 - 0.6
delay [ns]	0.25	3	100	2	0.27	2
Max delay variation over CMR (+/-%)	30	20	10	N/A	N/A	30
input offset voltage [mV]	60	40	28	7.8	2.5	40
Power [µW]	40	1.5	0.015	600	230	0.5

delay curve versus input voltage has a slope of 0.1 ns/dec at V_{DD}=0.9V. The sensitivity of the delay to the input voltage clearly increases at lower V_{DD}, due to the larger sensitivity of the current to the gate-source voltage, and reaches 30 ns/dec at V_{DD}=300 mV.

The standard deviation of the input offset voltage for the proposed RRDVC and prior DVCs was simulated by post-layout Monte Carlo analysis with 1,000 runs. The results are in Fig. 7, which shows that the worst-case input offset voltage is 60 mV, 35 mV, 24 mV at V_{DD}=0.9 V, 0.6 V and 0.3 V.

Again, this confirms that the proposed voltage comparator is well suited for operation at deep sub-threshold voltages. From Fig. 7, the offset voltage is reduced to less than 10 mV when the input is biased around $V_{DD}/2$, regardless of the supply voltage.

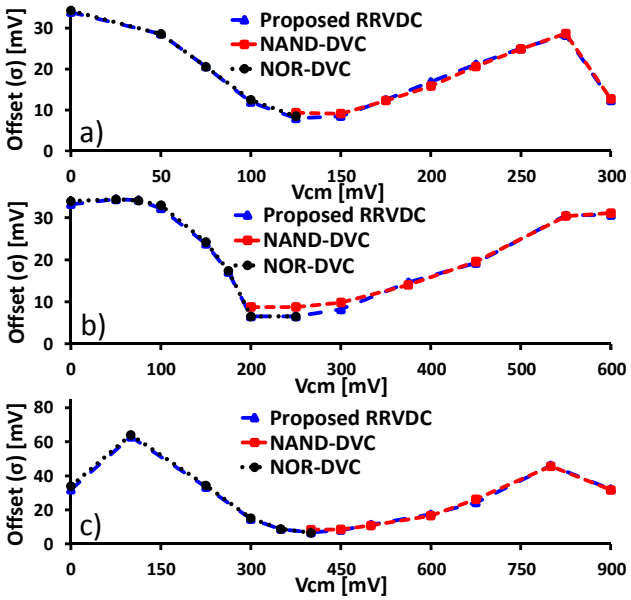

Fig. 7. Input Offset voltage standard deviation versus CM input voltage (Vcm) for a NAND3-DVC, for a NOR3-DVC and for the proposed RRDVC, operated at a) V_{DD}=0.3V, b) V_{DD}=0.6mV and c) V_{DD}=0.9V

Moreover, as expected from Pelgrom's law, the offset voltage is approximately proportional to $1/\sqrt{strength}$ [10], being $strength$ the strength (i.e., size) of the standard cells of the NAND/NOR input stage. This is confirmed by simulations showing 1.45x and 1.95x offset reduction for a 2x and 4x increase of strength under identical conditions. In other words, the offset can be traded off with area and power as normally allowed by conventional analog DVCs designed in a custom fashion. On the other hand, thanks to the full synthesizability of the proposed RRDVC, this tradeoff can be managed in a very agile manner by simply choosing the size of the cells adopted for the input stage. This takes a much lower design effort than conventional analog DVCs, which require a fundamental layout redesign of the input stage.

The resulting performance metrics of the proposed DVC are summarized in Table I, and are compared with prior art. From this table, the proposed RRDVC extends up to 3x the CMR of the previously proposed digital DVC [5]. Also, unlike analog designs, it operates properly down to V_{DD} =0.3V with nano-watt range power consumption, which makes it attractive for energy harvested IoT nodes.

V. CONCLUSIONS

A fully synthesizable, rail-to-rail DVC has been presented in this paper. The operation of the circuit over the rail-to-rail CMR for supply voltages down to 0.3 V has been demonstrated by post-layout simulations in 40nm CMOS. As a major advantage over previously proposed fully synthesizable DVCs, the proposed RRDVC can be adopted as a replacement of its analog counterpart in ultra-low voltage circuits, such as medium-low resolution ADCs for IoT applications.

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