POLITECNICO DI TORINO
Repository ISTITUZIONALE

On-line temperature estimation of SiC power MOSFET modules through on-state resistance mapping

Original
On-line temperature estimation of SiC power MOSFET modules through on-state resistance mapping / Stella, F., Pellegrino, G., Armando, E., Dapra, D.. - ELETTRONICO. - (2017), pp. 5907-5914. (Energy Conversion Congress and Exposition (ECCE), 2017 IEEE Cincinnati, OH, USA 1-5 Oct. 2017) [10.1109/ECCE.2017.8096976].

Availability:
This version is available at: 11583/2697232 since: 2018-01-12T11:25:04Z

Publisher:
Institute of Electrical and Electronics Engineers Inc.

Published
DOI:10.1109/ECCE.2017.8096976

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright
IEEE postprint/Author's Accepted Manuscript

©2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

27 November 2026

On-line Temperature Estimation of SiC Power MOSFET Modules through On-state Resistance Mapping

Fausto Stella, Gianmario Pellegrino, Eric Armando
DENERG, Politecnico di Torino, Turin, Italy
fausto.stella@polito.it

Davide Daprà
Vishay Semiconductor Italiana S.p.A., Turin, Italy

***Abstract*—The paper deals with real-time estimation of the junction temperature of a SiC power MOSFET modules. The junction temperature of one device of the module is real-time estimated by measuring its current and on-state voltage at each time sample, and entering the temperature model of the device. The temperature model is obtained in a dedicated commissioning session, where the v_{ON} is measured at different temperature and current conditions. A sequence of current pulses of short duration is closed-loop imposed to the device at different values of the measured DBC substrate temperature, so that the temperature measurement is consistently representing the junction temperature during the identification. The presented results show that the proposed method permits on-line temperature monitoring and even closed loop regulation of the junction temperature of the tested SiC power MOSFET modules. Different module from two different manufacturers are tested under realistic operating conditions. This concept can be usefully applied to all DC/AC conversion structures, where the monitoring of one device can be of reference value for the entire module.**

Keywords— SiC power MOSFET, Junction temperature monitoring, On-state resistance, TSEP.

I. INTRODUCTION

The failure rate of power semiconductors is closely related to their junction temperature during operation, which in many cases is known very approximatively through a temperature sensor placed into the power module. Despite the efforts of the scientific community and power module manufacturers, the measurement of the junction temperature of power semiconductor devices is still a challenge. Over the years the problem has become more important due to the further increased power density of the new devices such as Silicon Carbide (SiC) power MOSFETs.

According to [1], the methods currently used to evaluate the temperature of power semiconductors devices are divided into **optical methods**, **physical contact methods** and **electrical methods**. Each approach has its own strengths and weaknesses. The methods of the first class are based on the detection of optical proprieties of the semiconductor, which are temperature dependent, or more simply on the acquisition of the thermal image of the semiconductor die through an infrared camera.

This class of techniques can achieve a high level of accuracy and provide a thermal map of the semiconductor die, from which the points of maximum temperature and the gradient of temperature across the die are easily determined. However, all such methods need visual access to the chip, the removal of the dielectric gel and extra computing resources to process the thermal image.

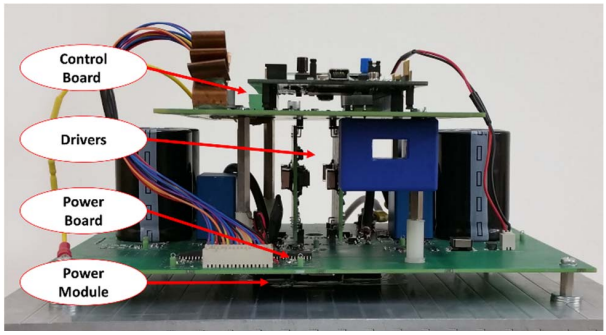

Fig. 1. Picture of the experimental setup.

Physical contact methods put the die in direct contact with a thermo-sensitive material (e.g. thermocouples or thermistors). This approach requires mechanical access to the die inside the module and has a limited accuracy and dynamic response, as also confirmed by the results of this paper.

Above the many techniques based on thermo-sensitive electrical parameters (TSEP) developed over the last years, the most significant are based on the evaluation of switching times or on the threshold voltage of the body diode [1] and [2]. Most of the TSEP techniques require complex calibration procedure that makes their application in a commercial converter impractical.

Nevertheless, the knowledge of the junction temperature during operation is a powerful source of information for many purposes, including protection, diagnostics and full exploitation of the device safe operating area.

This paper presents a technique for the estimation of the junction temperature of a SiC power MOSFET, with high accuracy and dynamics, applicable to all types of PWM commanded DC/AC converters. The proposed experimental setup consists of an H-bridge power converter made with an Emipak 2B module, equipped with additional sensors for the measurement of the on-state current and voltage of one of the four power devices of the module. The junction temperature model is built via the initial commissioning of the on-state

resistance of the monitored power switch, whose output is a look-up-table defining the on resistance as a function of the junction temperature and conducted current. The look-up table is then used in operation for on-line determination of the junction temperature, according to the real-time sampled on-state current and voltage of the device. The points of strength of the proposed method are related to its simplicity and accuracy. In turn:

1) The converter commissioning does not need dedicated equipment like a curve tracer, and can be performed directly on the final application.

2) The additional hardware is off the shelf and low cost, easy to include in the power converter schematics.

3) Temperature detection does not affect the converter operation with either noise injection or additional parasitics, and has a fast dynamic response.

4) No complex computation is involved.

A prototype was built and tested to validate the proposed method, depicted in Fig. 1.

II. PROPOSED SETUP

The power converter prototype depicted in Fig. 1 consists of the power module, one power board, two gate-driver boards and one control board on top. The heatsink, partially visible in the low part of the picture, has two fans for ventilation and four resistors for pre-heating the components and impose the case temperature during the commissioning stage.

Fig. 2 reports the schematics of the power section. The custom Emipak 2B power module (courtesy of Vishay Semiconductor Italiana) of Fig. 3-a is connected in H-bridge configuration, and supplies a purely inductive load. This permits to mimic realistic operating conditions while absorbing a fraction of the converted power from the input DC source. The load current is closed-loop controlled by one leg of the module (LEG2), while the other leg (LEG1) is open loop controlled at a fixed duty-cycle, to mimic a constant voltage source. The power module is monitored electrically and thermally, as detailed in the next paragraphs.

A. Power Module

Fig. 4 shows the layout of the power module. Two capacitors are embedded into the module (green rectangles in Fig. 4), to minimize the stray inductance of the power loop. One embedded thermistor (NTC1) is used for measurement of DBC (direct bond copper) substrate temperature, also called the "case temperature" in the text. Moreover, one additional thermistor (NTC2) was later put in direct contact with the die of the MOSFET under monitoring, as depicted in Fig. 3-b.

B. Power Converter Description

The control board was made for easy plug-in of one STM32F429 Discovery demo board, for real-time control and data collection purposes.

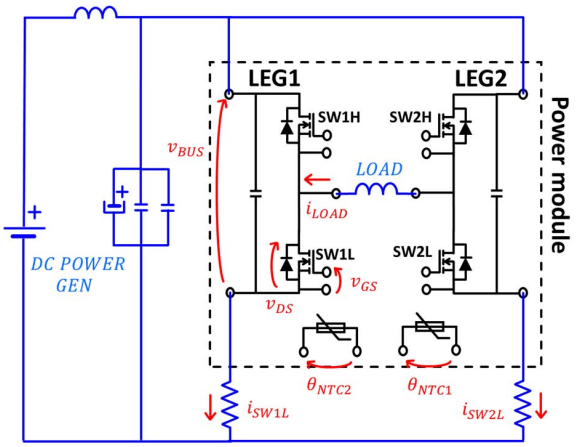

Fig. 2. Schematic diagram of the proposed setup: red quantities are measured online.

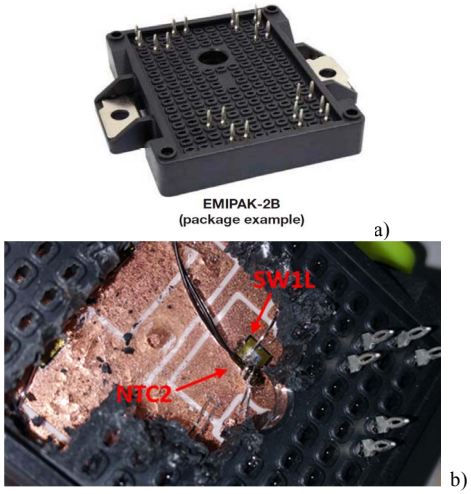

Fig. 3. a) Power module package. b) Placement of NTC2 thermistor.

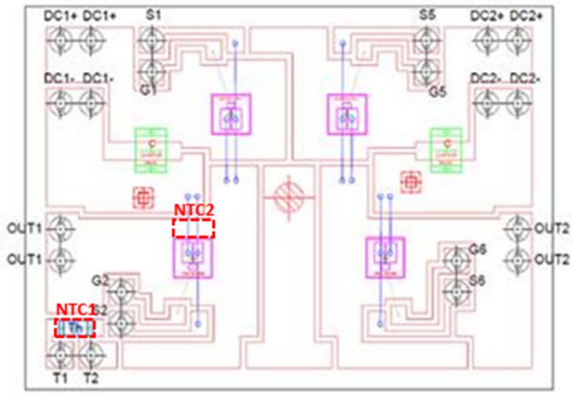

Fig. 4. Layout of power module (courtesy of Vishay Semiconductor Italiana). Internal capacitors are in green. NTC1 and NTC2 are the NTC resistor embedded in the module and one additional temperature sensor, in intimate contact with the die of the MOSFET under monitoring.

Table I - Ratings of the experimental setup

Maximum RMS Load current	40 A
Maximum DC Voltage	1000 V
Maximum Switching frequency	500 kHz
Electrolytic capacitors (total)	1120 µF
Film capacitors	10 µF
Ceramic capacitors (SMD)	300 nF
Inductive load	22 to 176 µH
Microcontroller	STM32F429ZI
12-bit A/D channels of the MCU	3
12-bit A/D converters on the power board	5
On-board SDRAM memory	64Mbit
Adjustable plate temperature	30°-150°C
V_{GS}	-5/+20V
Power Module #1 (from datasheet)	
Rated current (T_{sink}=80°C)	19A
Breakdown voltage	1200 V
Ron @ 25°C, 20A	78 mΩ
$C_{internal}$	2 x 47 nF
Max Junction Temperature	175°C

The Discovery board embeds the ARM Cortex-M4 microcontroller unit STM32F429ZI, and was chosen for its onboard 64 Mbit SDRAM memory, used for data buffering during PC communication. The control board includes one LEM current transducer used for closed loop control of the load current, and a resonant high frequency power generator which provides insulated power distribution to the gate drivers and additional A/D converters placed on the power board.

The driver boards, one per module leg, are sandwich-connected between the upper control board and the lower power board. Such 3-dimensional arrangement permits to minimize the distance between the drivers and the power module and therefore to minimize the parasitic inductance of the gate driver circuit. The drivers boards are based on the intelligent driver STGAP1S, that offers programmable fault check and hardware protection thresholds.

The power board houses the DC link electrolytic capacitors visible in Fig. 1 and five additional A/D converters. These sample the electrical quantities v_{GS}, v_{DC}, v_{DS}, i_{SW1L}, i_{SW2L} indicated in red in Fig. 2. The trigger of A/D synchronization is provided by the MCU. Each A/D converter communicates with the MCU through a dedicated opto-isolated SPI connection.

C. Measurement of the on-state drain-source voltage

Special attention was paid to the measurement of the on-state voltage drop V_{ON} of the monitored switch SW1L. The schematics of the signal conditioning circuit is reported in Fig. 5. The two diodes D8 and D9 protect the signal circuit from the DC-link voltage when the MOSFET SW1L is OFF.

When the SW1L is in ON state, the diodes are forward-biased by injection of a calibrated current and the drain-source voltage V_{ON} turns into the output signal ADC, to be sampled by the dedicated A/D unit. For guaranteeing that the forward voltage drops of the diodes are identical, the bias currents are obtained from a current mirror. Moreover, the diodes are placed close to each other on the board (see Fig. 6), so that temperature variations might affect their voltage drop to the same extent.

The operational amplifier U15 is an OPA 357 with an output voltage slew-rate of 150 V/µs, for fast transition between saturated and linear states at every commutation of the power component.

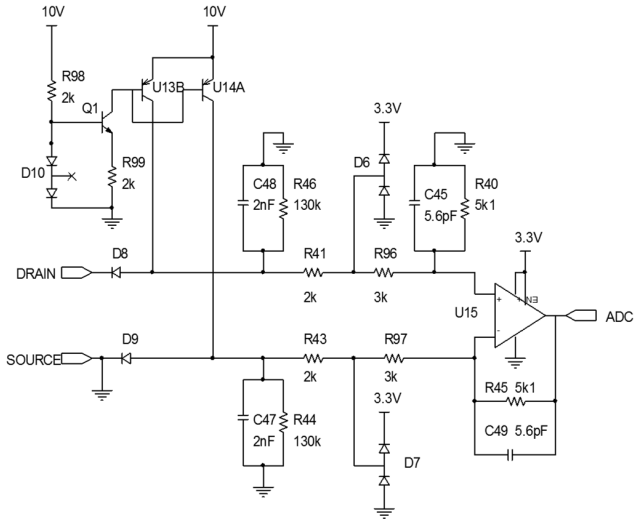

Fig. 5. Schematic of measurement system for the VON

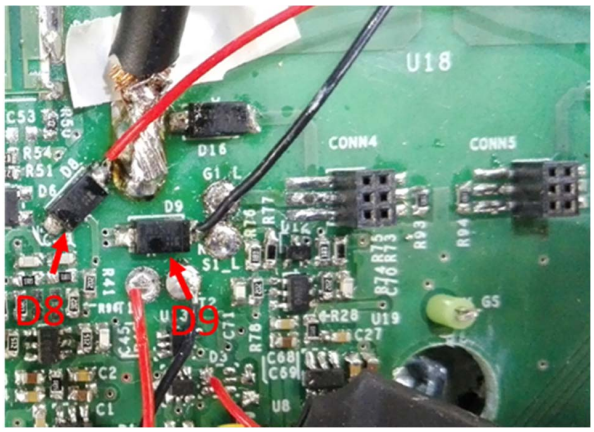

Fig. 6. Detail of the PCB board with the two diodes in close proxymity.

Fig. 7 shows the V_{ON} voltage at the input of the ADC converter, during operation, with a duty cycle around 50% and i_{DS}>0. When the switch SW1L is OFF the ADC voltage is clamped to the upper rail voltage of the OPA, equal to 3.3V, and the OPA input is protected by the two diodes describe

above. The blue arrows indicate when the V_{ON} is sampled by the A/D converter.

In this setup, the voltage conditioning circuit was off-line calibrated for the purpose of producing precise identification curves for the modules under test. However, if the proposed commissioning methodology were applied to a commercial converter, this would not require precise calibration of the drain-source voltage.

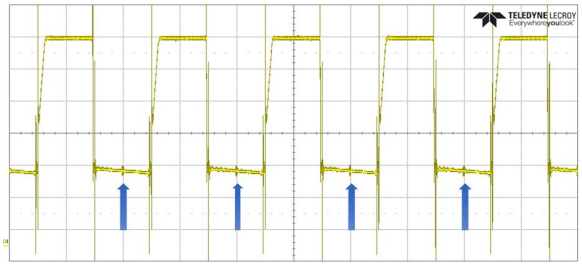

Fig. 7. ADC output of the OPA in Fig. 5 (25µs/div, 500 mV/div). The switch SW1L is commanded at 50% duty-cycle. Arrows indicate the sampling time.

III. Commissioning and On-line Monitoring

A. V_{ON} map Concept

First, the on-state voltage drop of the MOSFET under test SW1L is characterized as a function of junction temperature and on-state current. An example of results of such V_{ON} commissioning is shown in Fig. 8. Then, the obtained $V_{ON}(I_{DS}, \theta_J)$ model is used for real-time estimation of the junction temperature during operation, as explained later.

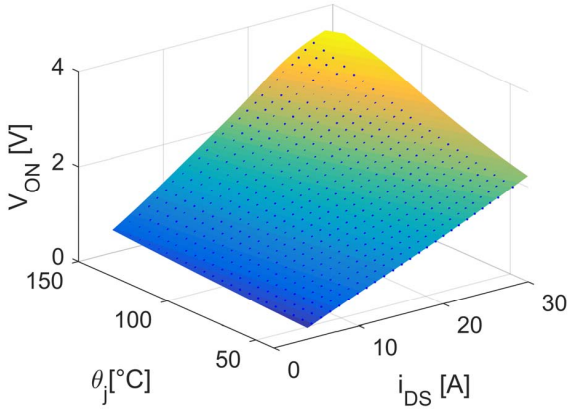

Fig. 8. Measured Von as a function of junction temperature and current.

B. Self-Commissioning of V_{ON} vs Temperature and Current

The characterization of V_{ON} versus the junction temperature θ_J and drain current i_{DS} is done by imposing a series of current pulses of short duration to the module, and repeat the sequence for different values of the case temperature. The device voltage and current in on-state are measured and stored in a look-up table. The case temperature is imposed by heating the heatsink plate of the setup using two external resistors. The DBC temperature is continuously measured with the NTC1 thermistor embedded in the module and used as temperature feedback.

The heatsink is preliminarily heated using two external heating resistors until the NTC1 outputs 145°C. Then, the resistors are turned off, the fans are turned on and the identification sequence begins. Twenty-eight current pulses of short duration (100 µs each) are closed-loop controlled in the H-bridge, from 1 A to 28 A as shown in Fig. 9. The on-state voltage and current of the switch SW1L under test are measured at each current pulse. The series of current pulses is launched at 145°C and then repeated at every 5°C during the cool down of the heatsink, until a temperature of 25°C is reached.

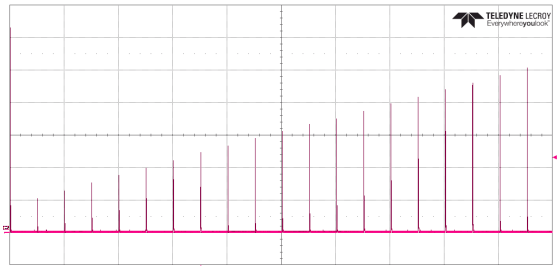

Fig. 9. Impulsive current test for mapping the Ron. iSW1L=5 A/div t=200 ms/div

The 100 µs pulse duration ensures that the junction temperature does not vary with respect to the case temperature, which is measured. The module datasheet in Fig. 10 tells that the transient thermal impedance for a DC pulse of duration 100µs is 0.03 °C/W, to say that the temperature rise during one current pulse is $\Delta\theta_J$ < 3.06°C, evaluated in worst case conditions (V_{ON} = 3.64V, i_{DS}=28A, θ_J=145°C, P_{ON} = 102W). This temperature variation is small enough to assume that the junction temperature remains equal to the case temperature when V_{ON} and i_{DS} are sampled and stored at each pulse. Moreover, the time lag between current pulses is of 100 ms, so that the junction temperature has time to return exactly to the measured DBC temperature value, before the next pulse occurs.

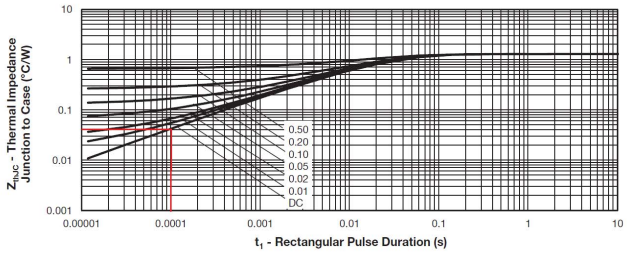

Fig. 10. Maximum thermal impedance Junction-to-Case Characteristic (courtesy of Vishay Semiconductor Italiana).

One current screening from 1 A to 28 A is completed in a total of 3.5s, during which the DBC temperature remains reasonably constant, as confirmed by measurements. After the first current scan is completed, the heatsink fans are turned on until the case temperature reaches the next level of 140°C. The current sequence is repeated for the next 3.5 s, and so on. The test is stopped when the case temperature reaches 25°C.

Fig. 8 reports the results for one power module, whose reference data is reported in Table 1. The V_{ON} surface as a function of current and junction temperature summarizes the results of this test.

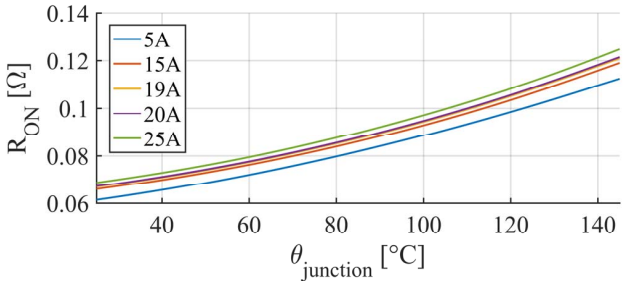

Fig. 11. Measured values of Ron as a function of junction temperature.

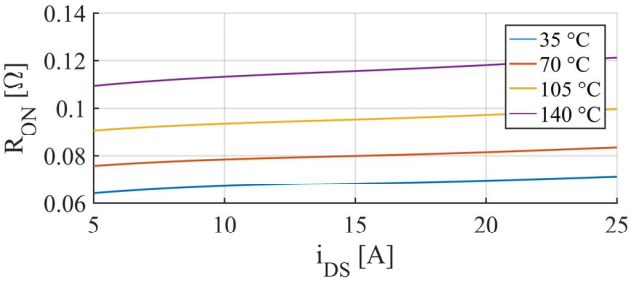

Fig. 12. Measured values of Ron as a function of current.

Fig. 11 and Fig. 12 report the corresponding on-state resistance curves, as a function of temperature and current, respectively. According to Fig. 11, the sensitivity to junction temperature is significant. For example the resistance increases by 84% when passing from 25°C to 145°C. Conversely, the sensitivity to the load current is less pronounced, as shown in Fig. 12. Other modules were characterized, with SiC MOSFET dies from a different manufacturer, proving the consistency of the proposed setup and methodology [8].

C. *Online Monitoring of Junction Temperature*

The $V_{ON}(i_{DS}, \theta_J)$ table of Fig. 8 is used for on-line estimation of the junction temperature, in the form of its inverse model $\theta_J(i_{DS}, R_{ON})$. The on-state current and voltage of the device are measured at each PWM period, the resistance is evaluated and the temperature estimated from the table. A computationally efficient implementation is obtained by direct use of a LUT built in the form $\theta_J(i_{DS}, V_{ON})$, as reported in Fig. 13. V_{ON} and i_{DS} measurements are used for real-time estimation of the junction temperature, being the former the only additional measurement required for the implementation of the proposed technique, respect to a standard power converter. The index (k) in Fig. 13 indicates the current time sample of the digital controller t_k.

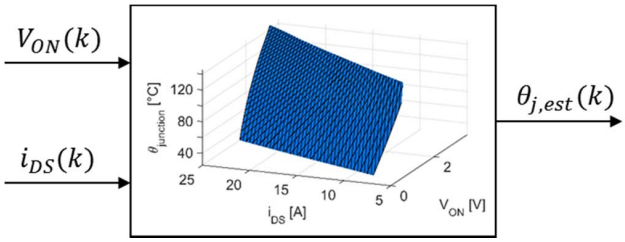

Fig. 13. On-line temperature monitoring, functional block.

The response of the temperature estimate to a square-wave load current is reported in Fig. 14, showing the fast dynamic response of the method. A similar concept of temperature monitoring was proposed in [3] for CoolMOS devices, but without addressing the dependency of R_{ON} (same as V_{ON}) from the drain current, that is not negligible here, and using data from datasheet or external hardware for identification of the R_{ON} characteristic, used in place of V_{ON} in that work.

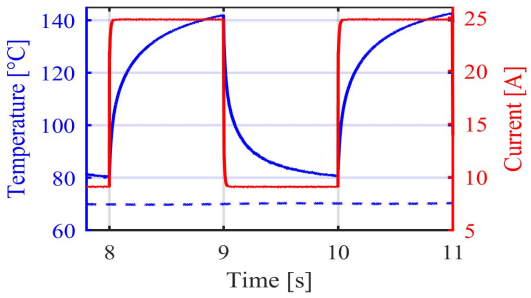

Fig. 14. On-line estimation of SW1L junction temperature (blue), with squarewave load current (red). Dashed blue line: DBC substrate temperature, measured from NTC1.

D. *Singular conditions and implementation issues*

When the conduction time of the switch SW1L decreases to the order of few microseconds, the V_{ON} measurement can become problematic. If the duty cycle is close to 100%, the switch SW1L is in conduction for a limited amount of time. The same is true when the switching frequency is high, e.g. >100 kHz, which might be reasonable with SiC devices. The proposed current measurement system was tested with success up to 80 kHz, with duty cycle = 50%. Work is in progress to push the switching frequency limit up to 200 kHz.

Another singular condition is when i_{DS} is very low. In this case the V_{ON} is low as well and the measurement accuracy deteriorates. However, this situation is normally associated to low conduction loss, i.e. the junction temperature similar to the DBC temperature. In turn, the accuracy of the temperature estimate is not critical in this condition.

E. Real-Time Limitation of the Junction Temperature

As a proof of concept, the on-line estimation of θ_J is used here for closed-loop limitation of the junction temperature during operation at variable load conditions. A PI regulator was used at this purpose, which limits the load current reference when the estimated temperature reaches a predefined maximum value. This is not intended as the final use of the proposed monitoring technique, but it is considered a valid stress test for demonstrating the potential and the high dynamic response of the proposed temperature estimation technique.

In the tests described in Fig. 15 to Fig. 18 the junction temperature limit is set at 140°C, 120°C and 100 °C in sequence, as indicated by the black horizontal dashed lines. The load current in the first 15 seconds of the test is constant and equal to 18A. After 15 s, a sinusoidal current reference is superimposed to the direct current.

Fig. 15 and Fig. 16 refer to a leg1 duty-cycle = 0%, i.e. SW1L in continuous conduction, with the ac current component at 0.5 Hz and 1.0 Hz, respectively. The estimated temperature has a peak value of 150°C in the first case (0.5 Hz) and circa 130°C when 1 Hz is used. The frequency of the AC current component expectedly lowers the amplitude of the temperature swing. In both Fig. 15 and Fig. 16, during the periods where the temperature threshold is 120°C and 100°C the current is real-time limited and the temperature instantaneously clamped to the threshold value.

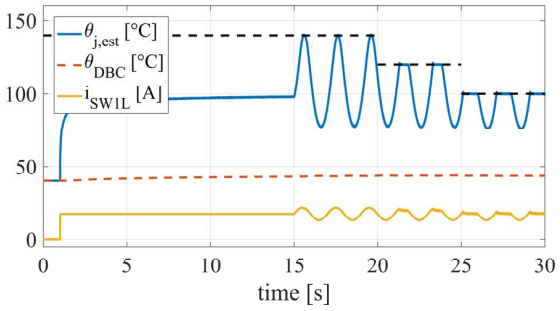

Fig. 15. Online junction temperature estimation, average duty-cycle LEG1 0% (SW1L always close). a) AC current frequency 0.5Hz

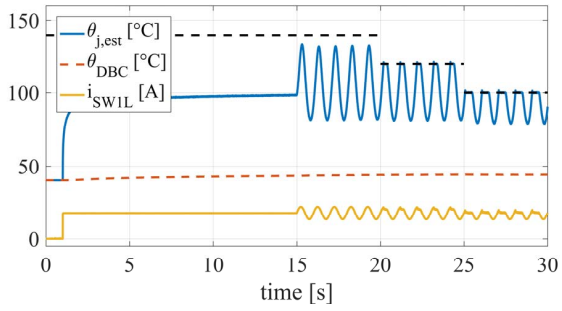

Fig. 16. Online junction temperature estimation, average duty-cycle LEG1 0% (SW1L always close). AC current frequency 1Hz

Fig. 17 and Fig. 18 report similar tests where the load current is the same but the duty-cycle is 50%. In this case the switch SW1L conducts for a shorter time and its temperature never touches the upper threshold. The proposed technique is compatible with more sophisticated temperature control techniques like the ones presented in [5] and [6].

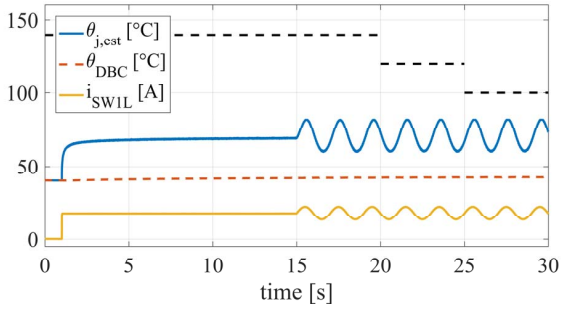

Fig. 17. Online junction temperature estimation, average duty-cycle LEG1 50% (SW1L close for 50% of the period). AC current frequency 0.5Hz

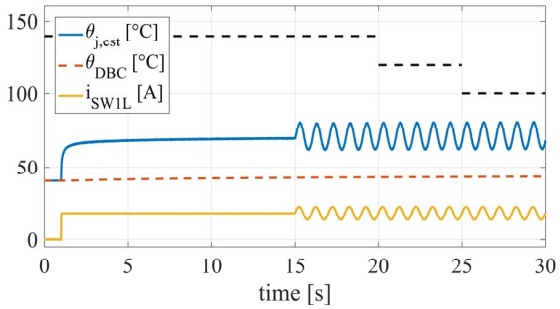

Fig. 18. Online junction temperature estimation, average duty-cycle LEG1 50% (SW1L close for 50% of the period). AC current frequency 1Hz

F. Use of NTC2 in Direct Contact with the Die

Besides the standard DBC thermistor NTC1, an additional sensor named NTC2 was later included for direct measurement of the die temperature of SW1L (Fig. 3-b). NTC2 has been placed as close as possible to the die, right under the bonding wires. The direct die measurement NTC2 was compared to the proposed temperature measurement in different operating conditions.

In Fig. 19 reports the temperature response to a load step, showing that the reading from NTC2 is far from being a good estimate of the junction temperature, both in terms of steady-state accuracy and dynamic response. The steady-state error between the NTC2 measurement and the estimate from the VON table here is around 50°C for a 25 A load. The response of the NTC2 output to the load step is also non representative of the fast response of the junction temperature. Similar conclusions can be drawn after the DC + AC load current test of Fig. 20. A 5 A peak current component at 0.1 Hz is superimposed to the 25 A direct current. Also in this case, the NTC2 output is underestimated both in average and peak values, and delayed respect to the junction temperature estimate. The source of underestimate and delay has to do with the thermal impedance between the thermistor and the junction

of the device. Although the thermistor touches the die, this is not enough for an accurate monitoring of the junction thermal status. This result is consistent with the literature [1].

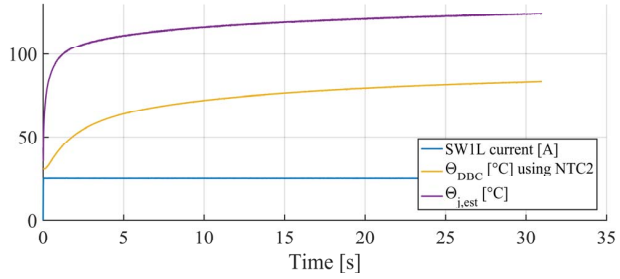

Fig. 19. Current step of 25A. Comparison between junction tmeperature estimate and direct-contact measurement with NTC2.

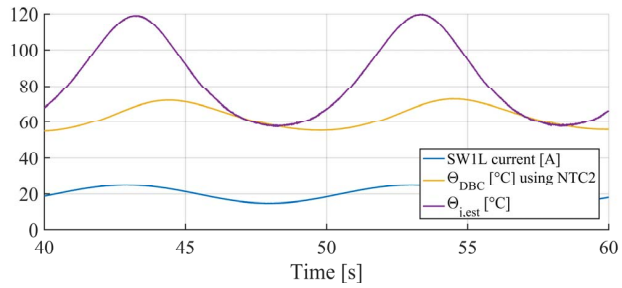

Fig. 20. AC current at 0.1 Hz superimposed to 25 A DC. Comparison between junction tmeperature estimate and direct-contact measurement with NTC2.

G. Self-Commissioining using NTC2

The characterization of the module has been repeated using NTC2 resistor instead of NTC1 to produce a second V_{ON} look-up table. The look-up table is identical to the one obtained using NTC1, shown in Fig. 8. The tests of Fig. 19 and Fig. 20 where repeated running the temperature estimates coming from the two tables in parallel, for the sake of comparison. The results of Fig. 21 and Fig. 22 show that the two table-based estimates are superimposed, the one coming from the former look-up table obtained with NTC1 and the new one using the look-up table obtained with NTC2.

The results show that the characterization of the module is insensitive to the placement of the NTC sensor within the power module. Otherwise said, the proposed commissioning and temperature estimation method does not require modifications of the power module, provided that this includes thermistor placed on the DBC substrate. The positioning of the thermistor within the module, and its distance from the monitored switch are not critical.

IV. Applicability of the Concept

A. Minimum Set of Measured Quantities

Not all the sampled quantities indicated in Fig. 2 are necessary for implementing the proposed online temperature estimation. The minimum set of dedicated measurements required by the proposed technique consists of:

- Switch current in on-state, measured via a shunt resistor in series with the switch. In many conversion structures the same shunt is already used for current control purposes. Current transducers of other type are also viable.
- Case temperature: one thermistor placed in the module, in contact with the DBC substrate.
- Drain-source voltage in on-state: this is the most critical measurement, as discussed in section II.C.
- Monitoring of V_{GS}. This measurement is not strictly necessary if the gate driver commands the V_{GS} properly at constant voltage. As shown in Fig. 23, the R_{ON} of the considered SiC power MOSFET has a significant sensitivity to the gate-source voltage.

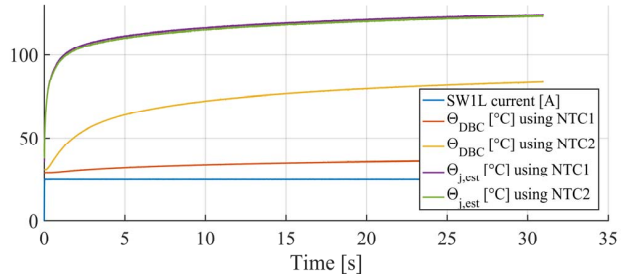

Fig. 21. Junction temperature estimation during a current step of 25A

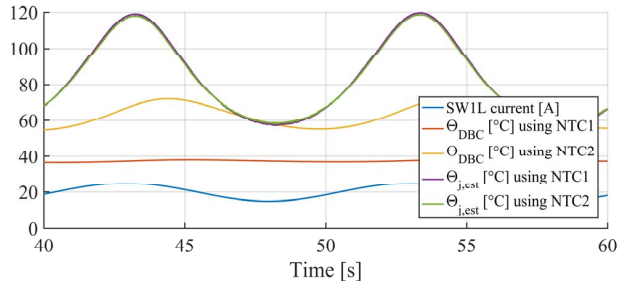

Fig. 22. Junction temperature estimation with sinusoidal current reference

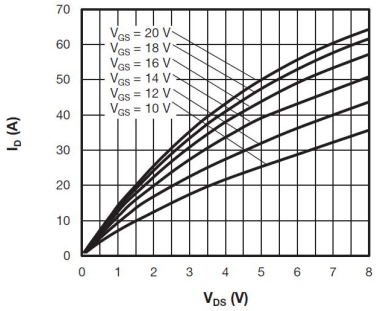

Fig. 23. Typical drain to source output characteristics at Tj=25°C (courtesy of Vishay Semiconductor Italiana).

B. Feasible Conversion Structures

One key assumption behind the proposed methodology is that the monitored switch is representative of the entire module's behavior. This is surely true for H-bridge structures operated in DC/AC configuration, as well as for 3-phase or n-phase 2-level voltage source inverters. All the mentioned DC/AC converter structures have in common the fact that all power devices, high side and low side, any leg, see the same duty-cycle and current over one period of the AC side. This guarantees that their peak temperature will be the same and that monitoring one switch will protect the entire converter.

For other structures, where the switches are loaded unevenly, the monitoring should be repeated for a number of significant switches. For example, if the H-bridge is used as a 4-quadrant DC/DC converter, monitoring the two switches of one leg is representative of the whole converter, because the two legs behave symmetrically. Other structures require to be evaluated case by case.

C. Aging of the Component and Prognostics

The R_{ON} tends to increase with the aging of the component. According to [7] the on state resistance can increase by 10%-17% before the components fails. This would lead the proposed technique to overestimate the device temperature, i.e. to over-limit the device current according to the detected extra-resistance. This to say that, without recalibration of the look-up table, the method tends to accelerate the detection of the component aging, and can be considered also as a tool for prognostics. In case the converter tends to under perform, a new self-commissioning session can put in evidence the increased R_{ON} and the aging effect. Future investigation will be needed to evaluate the increment of the R_{ON} before the failure of the component especially in SiC devices.

D. Limitations and future improvements

Due to limitations of the current prototypal hardware, the temperature of the switch SW1L can be monitored **only for positive values of the drain-source current**, because the V_{ON} conditioning circuit does not cover the negative range. This choice was initially made to mantling a high level of accuracy of this measurement. After a certain number of tests it is clear now that the current 12 bit A/D converters are accurate enough to measure a wider range of voltage, and the input range of the circuit will be extended to cover negative currents soon.

As explained before, the switching frequency for having a valid temperature evaluation is **currently limited to 80 kHz**, but also in this case a new release of the setup will improve the V_{ON} measuring system.

In a real-world converter, the measurement system might be integrated in the drivers, considering that most of the drivers already integrate desaturation protections based on V_{ON} inspection.

About the accuracy level of the temperature estimation, the modelling assumptions say that the estimated temperature should be very close to the real junction temperature, with maximum error lower than 3 °C, as said. However, a direct validation of such level of accuracy is not provided here, and it will hardly be in the future. It is difficult to find a reference test to prove the accuracy of the system, considering the scarcity of alternative methods that can offer a better level of precision and the same time response without impacting on the working conditions of the module. If possible, tests with infra-red thermal images will be performed in the future.

Last, the proposed solution provides the average temperature of the die, though the temperature gradient across the die is not always negligible. Nevertheless, in the authors' opinion this apparent limitation does not harm the applicability of the proposed method, which is considered a strong step ahead towards a seamless integrated temperature estimation.

V. CONCLUSIONS

The paper demonstrates that inserting the V_{ON} measurement on board of a power converter permits a good and high-dynamic estimation of the junction temperature of one of the power devices. The method is promising for application to standard and special converters, with little impact in terms of additional components and cost. The measurement system can be integrated into the gate driver circuit. Through the knowledge of the junction temperature it is possible exploit completely the SOA of the component while maintaining high reliability levels. It is expected that this innovation might reduce the cost of the final application.

REFERENCES

[1] Y. Avenas, L. Dupont and Z. Khatir, "Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters—A Review," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 3081-3092, June 2012.

[2] N. Baker, S. Munk-Nielsen, M. Liserre and F. Iannuzzo, "Online junction temperature measurement via internal gate resistance during turn-on," 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, 2014.

[3] A. Koenig, T. Plum, P. Fidler and R. W. De Doncker, "On-line Junction Temperature Measurement of CoolMOS Devices," 2007 7th International Conference on Power Electronics and Drive Systems, Bangkok, 2007.

[4] B.Callanan,"Application considerations for silicon carbide MOSFETs," Appl. Notes, CREE, Inc., Morrisville, NC, USA, Jan.2011.

[5] D. A. Murdock, J. E. R. Torres, J. J. Connors and R. D. Lorenz, "Active thermal control of power electronic modules," in IEEE Transactions on Industry Applications, vol. 42, no. 2, pp. 552-558, March-April 2006.

[6] M. Andresen, M. Liserre and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, 2014, pp. 1-10.

[7] S. Dusmez and B. Akin, "An accelerated thermal aging platform to monitor fault precursor on-state resistance," 2015 IEEE International Electric Machines & Drives Conference (IEMDC), Coeur d'Alene, ID, 2015.

[8] F. Stella, G. Pellegrino, E. Armando and D. Daprà, "Advanced Testing of SiC Power MOSFET Modules for Electric Motor Drives", 2017 International Electric Machines and Drives Conference (IEMDC), Miami, 2017.