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27 November 2026

Advanced Testing of SiC Power MOSFET Modules for Electric Motor Drives

Fausto Stella[1], Gianmario Pellegrino[1], Eric Armando[1], Davide Daprà[2]
[1]Politecnico di Torino, Turin, Italy, fausto.stella@polito.it
[2]Vishay Semiconductor Italiana S.p.A, Turin, Italy

***Abstract*—SiC power MOSFETs are an advancement in the power electronics technology today available on the market. Respect to Si-based power devices, they offer potential for higher operating temperatures, higher breakdown voltage with low on-state resistance, and lower switching losses permitting much higher switching frequencies. To date, the attempts to apply the SiC power devices to the field of AC drives are relented by the high price of such new devices and by the challenges related to electromagnetic compatibility and reliability. A new test rig is proposed, built for comprehensively testing SiC power MOSFET modules in real operating conditions, using off-the-shelf hardware. The presented results focus on the evaluation of on-resistance as a function of drain current and junction temperature, and on dv/dt evaluation as a function of external gate resistance. Different modules are tested, custom realized using SiC MOSFET dies by two leading manufacturers. Finally, a new methodology for on-line estimation of the devices junction temperature is presented.**

Keywords —SiC power MOSFET, Junction temperature monitoring, dv/dt limit, Regenerative test, On-state resistance.

I. Introduction

SiC power MOSFETs have been one of the hits in power electronics for at least the last five years [1]. The literature reports a number of comparisons between SiC power MOSFETs and IGBTs, applied to hard switching power converters [1]-[2]. Key advantages of SiC power devices are the lower switching and conduction loss, the higher operating temperature and the possibility of operating at higher switching frequencies. Altogether, SiC devices are expected to revolutionize power conversion more and more. Discrete devices and power modules are on the market, and converters designers are investigating feasible ways to exploit the SiC potential for realizing more efficient, more integrated and more rugged power converters. Dealing with the application of SiC devices to the field of electric motor drives, improvements are expected in terms of better physical integration of the power electronics into the electrical machine and increased time resolution coming from the high switching frequency, useful for the control of high-speed machines. The downsides in the application of SiC power devices to DC/AC and DC-DC converters [3]-[4] deal with the cost of the components, the non-compatible gate drivers, the tendency to generate electromagnetic interferences [5] and switching overvoltages.

This paper describes a new setup for testing SiC power MOSFET modules, capable of producing insightful information on the behavior of the power devices in realistic operating conditions. All hardware needed for comprehensive characterization of the power module was realized in house using low cost off-the-shelf components, including an industrial microcontroller for control and data collection purposes. The power modules where custom realized by courtesy of Vishay Semiconductor Italiana, using SiC dies from two leader semiconductor manufacturers.

The results show the characterization of the on-state resistance as a function of junction temperature and drain current, the evaluation of the voltage slew rate (dv/dt) as a function of gate resistance and load current, and a new procedure for online monitoring the junction temperature, particularly useful both for the modules characterization and for monitoring in operation.

II. Proposed Setup

The power section of the proposed setup is reported in Fig. 1. The custom Emipak 2B power module is connected in H-bridge configuration, suppling a purely inductive load. The inductive load permits to mimic realistic operating conditions without absorbing significant active power, in a regenerative fashion. The same structure can be easily readapted to a three phase converter. The regenerative configuration is useful for testing the power devices since it avoids the need for high-power power supply and load, and because it makes it easier to measure the power loss of the converter. The power module is monitored electrically and thermally, as detailed in the next paragraph.

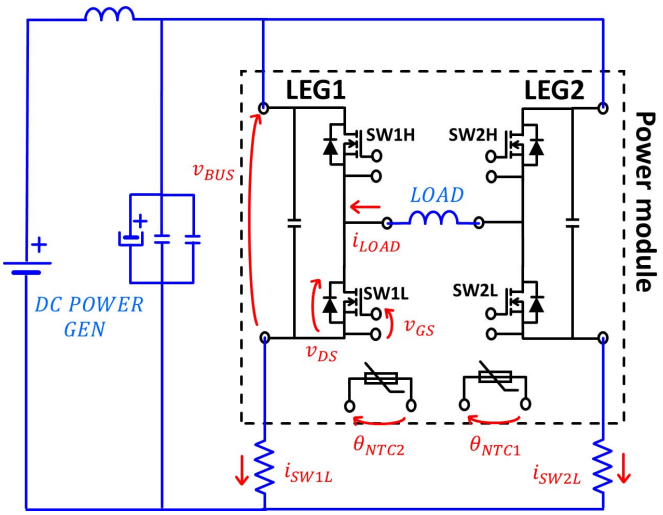

Fig. 1. Schematic diagram of the proposed setup: red quantities are variables measured online by the embedded controller.

With reference to Fig. 1, LEG1 of the module is closed-loop current controlled, to impose the load current, and LEG2 is open-loop controlled at a fixed duty-cycle, to mimic a constant voltage source. The 2-leg custom module (Fig. 2) has two inner capacitors (green rectangles), intimately connected to the power devices to minimize the parasitic inductance of the power loop. Moreover, a first NTC is embedded into the module (red rectangle labeled as NTC1), and used for measurement of the DBC substrate temperature (DBC = Direct Bonded Copper). A second NTC (red rectangle label as NTC2) was later added in intimate contact with the switch SW1L, for a closer measurement of the die temperature.

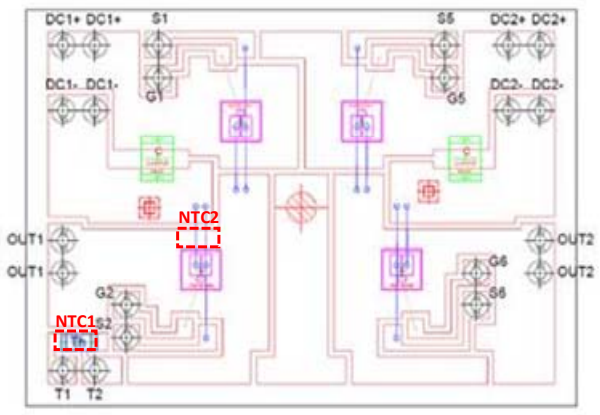

Fig. 2. Layout of power module (courtesy of Vishay Semiconductor Italiana). In green the two internal local capacitors. In blue the internal NTC resistor (label "Th"), for measurement of case temperature.

A. Custom Boards Description

The setup depicted in Fig. 3 and Fig. 4, consists of one control board, one power board and two gate driver boards, all developed in-house.

The upper control board houses the STM32F429 Discovery demo board based on the STM32F429ZI microcontroller unit, which controls the power converter and the data acquisition and collection. The Discovery board has a 64 Mbit SDRAM memory onboard, used for data buffering during the acquisitions at high sample rates, and the ST-LinkV2 embedded interface, for debug and data exchange between the microcontroller and a host PC during the tests.

The control board includes one LEM current transducer used for closed loop control of the load current (in blue in Fig. 4). A Wheatstone bridge is used for measuring the resistance of the NTC1 embedded in power module and a resonant high frequency power generator on board of the control board provides insulated power distribution to the gate drivers and to the data acquisition hardware located on the power board.

The two driver boards, one for per leg of the module, are sandwich-connected between the upper control board and the lower power board. Such three-dimensional arrangement permits to minimize the distance between the drivers and the power module and therefore the parasitics of the gate driver circuit. The driver boards are based on the intelligent driver STGAP1S, that offers programmable fault check and hardware protection thresholds.

The power board houses the DC link capacitors and data measurement systems (additional external DC link capacitor are also provided). Five local A/D converters sample electrical quantities with a synchronization trigger provided by the MCU (Micro Controller Unit). Such quantities are V_{GS}, V_{DC}, V_{DS}, i_{SW1L}, i_{SW2L}, all indicated in red in Fig. 1. Each A/D converter communicates with the MCU through a dedicated opto-isolated SPI link.

Besides on board data logging, the power absorbed from the dc source and the power loss in the inductive load can be measured with external power meters, for further verification of the converter's efficiency.

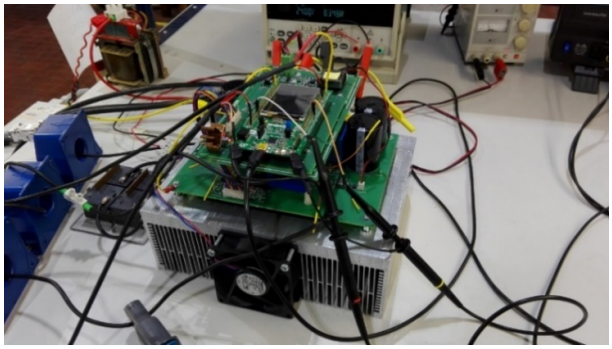

Fig. 3. Overview of the proposed experimental setup.

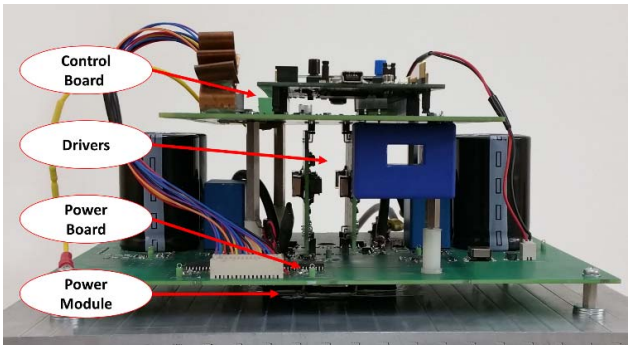

Fig. 4. Detail of the different boards.

Table I - Ratings of the experimental setup

Maximum RMS Load current	40 A
Maximum DC Voltage	1000 V
Maximum Switching frequency	500 kHz
Electrolytic capacitors (total)	1120 µF
Film capacitors	10 µF
Ceramic capacitors (SMD)	300 nF
Inductive load	22 to 176 µH
Microcontroller	STM32F429ZI
12-bit A/D channels of the MCU	3
12-bit A/D converters on the power board	5
On-board SDRAM memory	64 Mbit
Adjustable plate temperature	30°-150 °C

Table I - Ratings of the experimental setup

Power Module #1 (from datasheet)	
Rated current (T_{sink}=80 °C)	26A
Breakdown voltage	1200 V
R_{ON} @ 25 °C, 20 A	71 mΩ
$C_{internal}$	2 x 47 nF
Max Junction Temperature	175°C
Power Module #2 (from datasheet)	
Rated current (T_{sink}=80 °C)	19 A
Breakdown voltage	1200 V
R_{ON} @ 25 °C, 20 A	78 mΩ
$C_{internal}$	2 x 47 nF
Max Junction Temperature	175 °C

B. *V_{ON} sampling method*

One key point of the proposed setup is the accurate measurement of the on voltage (V_{ON}) of SW1L, through sampling of the signal V_{DS} in Fig. 1. The system adopted for sampling V_{ON} is represented in Fig. 5. An operational amplifier in a differential configuration measures the difference between the drain and the source terminals of SW1L. When the switch is OFF, the two diodes D8 and D9 block the OFF voltage to protect the measurement system from over voltage. When SW1L is ON, the two diodes are polarized by identical currents provided by the current mirror (U13B and U14A) so that the amplifier can measure the VON with no effect of the diodes voltage drop. As said, the two diodes (labels D8 and D9 in Fig. 6) are polarized so to have the same voltage drop. A small residual difference was off-line calibrated prior to the tests. About the temperature effect on voltage drop of D8 and D9, the two diodes can be considered at the same temperature; due to their proximity. It is important that the slew rate of the operational amplifier is high enough to switch from saturated to linear output at every turn ON of the power component. An OPA 357 by TI with a 150 V/µs was chosen for this setup.

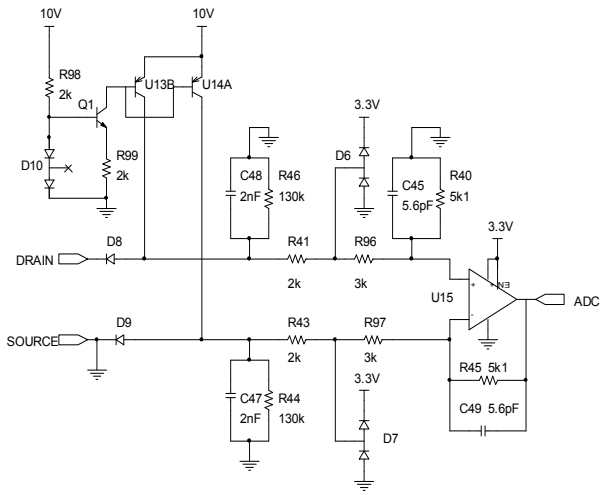

Fig. 5. Schematic of measurement system for the V_{ON}

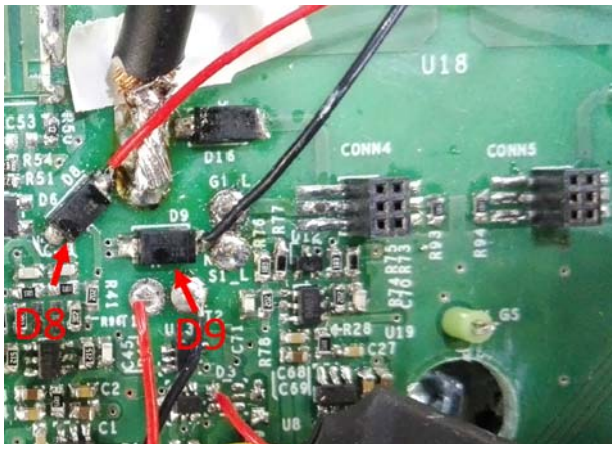

Fig. 6. Detail of the power board. The two diodes D8 and D9 are close to eachother.

III. RESULTS

During the tests, the converter work in regenerative conditions: the current flow from LEG2 to LEG1 with the sign indicated in Fig. 1. In other words, LEG2 behaves as a buck converter, while LEG1 behaves as a boost converter.

A. *Mapping of R_{ON} via a sequence of current pulses*

Characterization of R_{ON} versus junction temperature and ON current is done by repeating a set of current pulses at different values of case temperature, starting from 145 °C and repeating the current sequence at every 5 °C down to 25 °C. The heatsink is preliminarily heated to 145 °C using two external heating resistors, not visible in Fig. 3.

The DBC substrate temperature (or "case temperature") is measured with the NTC1 resistor embedded in the module. When the target case temperature is reached (say 145°C), the heating resistors are shut off and current screening at junction temperature 145°C begins. Thirty-five current pulses of short duration (150 µs each) are closed loop controlled in the H-bridge, from 1 A to 35 A, and the on voltage and current of SW1L are measured at each current pulse to evaluate the R_{ON}. The 150 µs pulse duration ensures that the junction temperature does not vary with respect to the measured case temperature. The time lag between one pulse and the following one is 100 ms, so that the any residual perturbation of the junction temperature is canceled before the next pulse occurs. The 1 A to 35 A current screening is completed in a total of 3.5 s (see Fig. 7), during which the case temperature remains reasonably constant, as confirmed by measurements.

After the first current scan is completed, the heatsink fans are turned on until the case temperature reaches the next level of 140 °C. The current screening is repeated at the new temperature, and so on. The test is stopped at a case temperature of 25 °C. The complete test sequence is shown in Fig. 8 for one of the modules under test. At low current values (range 1.0 to 3.0 A) the measurement of voltages and currents is more imprecise and so is the R_{ON} estimate.

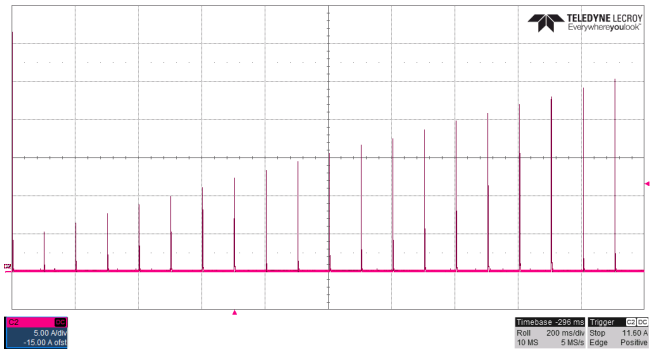

Fig. 7. Impulsive current test for mapping the Ron. iSW1L=5 A/div t=200 ms/div

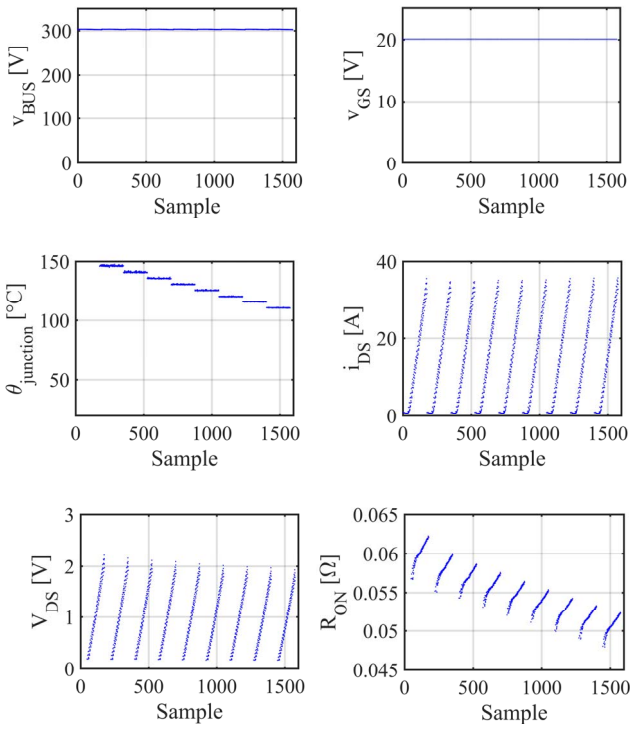

Fig. 8. Impulsive current test for mapping the R_{ON} (module #1).

B. R_{ON} comparison between the two modules

The results of the impulsive module scan described above are reported in the form of an R_{ON} map, function of the junction temperature and the current. Fig. 9 reports the R_{ON} maps obtained for the different types of SiC MOSFETS under test (module #1 and module #2). Besides having a lower on resistance, module #1 is also more insensitive to temperature than module #2. Comparing the two modules in terms of resistance value would be incorrect because they have different current ratings, but some consideration can still be made in percentage terms. According to Fig. 10, the on resistance of module #1 increases by 36 % when the temperature varies from 35 °C to 145 °C at its rated current of 26 A. On the other hand, according to Fig. 11 the on resistance of module #2 increases by 84 % when the temperature varies from 35 °C to 145 °C, at rated current of 19 A. For both modules the R_{ON} is stable respect to the conducted current at constant temperature, as show in Fig. 12 and Fig. 13.

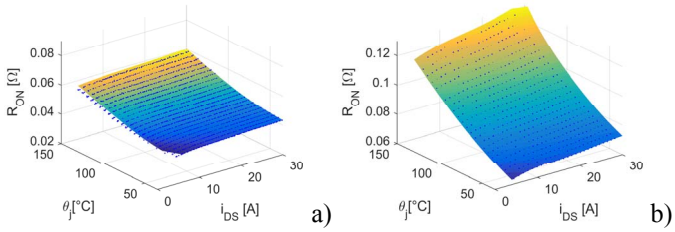

Fig. 9. a) Measured R_{ON} as a function of junction temperature and current for module #1. b) Same for module #2.

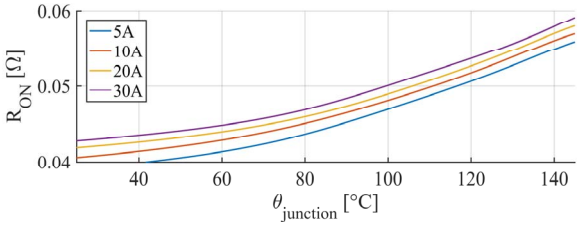

Fig. 10. Measured values of R_{ON} as a function of $\Theta_{Junction}$ for module #1.

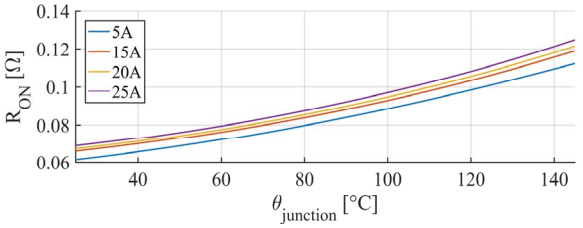

Fig. 11. Measured values of R_{ON} as a function of $\Theta_{Junction}$ for module #2.

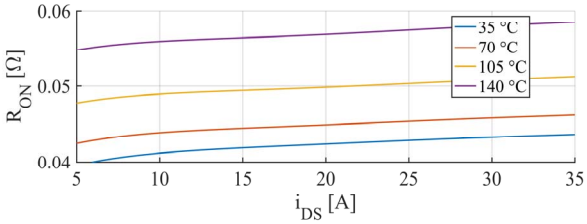

Fig. 12. Measured values of R_{ON} as a function of i_{DS} for module #1.

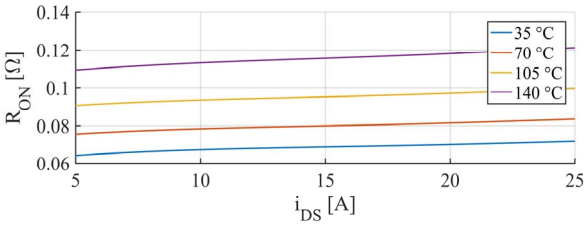

Fig. 13. Measured values of R_{ON} as a function of i_{DS} for module #2.

C. *dv/dt test*

The possibility of high *dv/dt* of SiC power MOSFETs is an opportunity that often turns into a curse, due to related problems of electromagnetic interference, switching overvoltages, line reflections and so on. Dealing with the field of electrical drives, electrical machines tend to suffer the high voltage slew-rate imposed by the converter resulting in premature aging of the insulations and the excitement of parasitic capacitances that can lead to impulsive common mode currents. High voltage slew rate combined with the use of long cables can lead to significant over voltages at the end of the cables [6]-[7]. For this reason, it is important find a compromise between increasing the *dv/dt* to reduce the switching losses and mitigating the problems discussed above.

Different values of gate resistance were tested to evaluate the voltage slew-rate and peak overvoltage at turn-OFF. The results are summarized in Table II for the two types of modules. The maximum voltage slew rate for module #1 is 31 kV/µs and it is obtained during the turn-ON with a rated current of 10 A and a gate resistor of 5 Ω. The maximum voltage slew rate for the module #2 is 50.5 kV/µs and it is obtained during the turn-ON with a rated current of 5 A. Unfortunately the slew-rate rejection of the gate driver is up to 50 kV/µs, and this limited the capability of testing module #2 above such limit. A new driver board with augmented dv/dt transient immunity is under design.

Peak over voltage during the turn-OFF is limited in all tested conditions, despite the high slew-rate voltages. This thanks to the optimized layout of the power loop within the modules, mainly a merit of the dc-link capacitor embedded into the module (green rectangles in Fig. 2). The module #2 can reach higher levels of voltage slew rate: compared to module #1 this means a potential for lower switching losses. However, underdamped oscillations and 40% peak overvoltage are observable at the turn-ON of module #2, with R_G=15 Ω and i_{DS}=25 A (Fig. 17). This shows that further increasing the *dv/dt* of module #2 is hardly doable, despite the good layout of the module.

Table II: Summary results collected dv/dt test

Power Module #1		
Turn-ON	Rg=10 Ω	19.5 kV/µs (10 A) //// 19.5 kV/µs (30 A)
	Rg=5 Ω	31 kV/µs (10 A) //// 24 kV/µs (30 A)
Turn-OFF	Rg=10 Ω	14.5 kV/µs (10 A) //// 17.5 kV/µs (30 A)
	Rg=5 Ω	18 kV/µs (10 A) //// 23 kV/µs (30 A)
Power Module #2		
Turn-ON	Rg=39 Ω	17 kV/µs (5 A) //// 20.5 kV/µs (25 A)
	Rg=15 Ω	50.5 kV/µs (5 A) //// 41.5 kV/µs (25 A)
Turn-OFF	Rg=39 Ω	12.5 kV/µs (5 A) //// 18 kV/µs (25 A)
	Rg=15 Ω	15.5 kV/µs (5 A) //// 37.2 kV/µs (25 A)

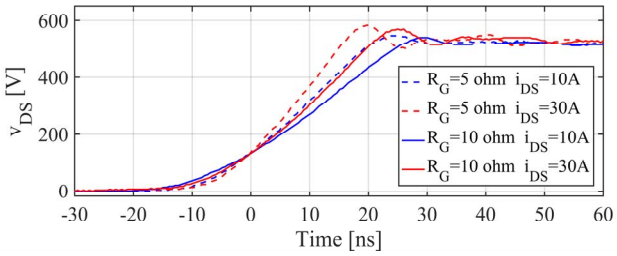

Fig. 14. Module #1 turn-off, behavior of V_{DS} for different values of gate resistor.

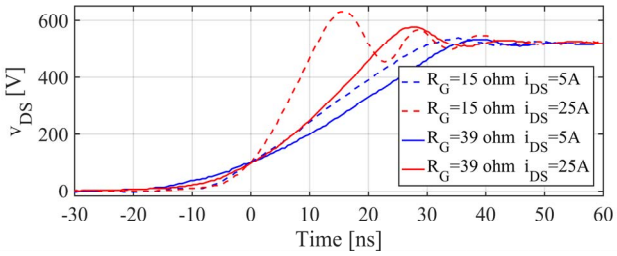

Fig. 15. Module #2 turn-off, behavior of V_{DS} for different values of gate resistor.

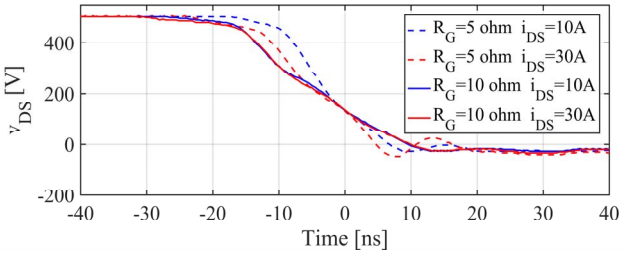

Fig. 16. Module #1 turn-on, behavior of V_{DS} for different values of gate resistor.

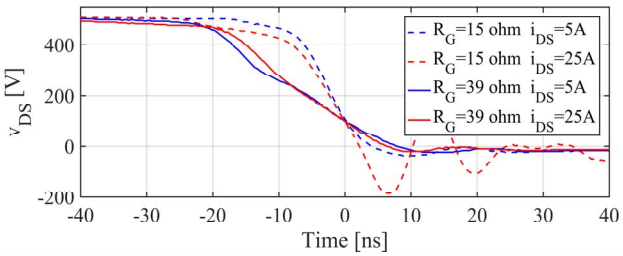

Fig. 17. Module #2 turn-on, behavior of V_{DS} for different values of gate resistor.

D. *Switching Losses Evaluation*

Switching losses can be evaluated by measuring the DC power absorbed by the module, for example using the opposition method suggested in [8]. Respect to the standard double pulse test (DPT) method, the proposed setup has the advantage of testing the device in its final layout, inside the module. The DPT is normally performed inserting the device under test into a testing equipment with its own parasitics, and with current and voltage probes adding other parasitics to the

power loop. The goodness of the layout is demonstrated by the switching waveform in Fig. 14-Fig. 17. Unfortunately, at the time of writing this paper tests are not completed. The main unforeseen problems were the accuracy of input and output power measurement when trying to avoid heavy preliminary filtering of the measured quantities, and the already mentioned limitations of the present gate drives.

E. Online Monitoring of Junction Temperature

Knowing the junction temperature during operation would be a powerful source of information for many purposes, including protection, diagnostics and full exploitation of the device safe operating area. The literature reports methods based on Thermal Sensitive Electrical Parameters (TSEPs) [9], [10], such as switching times or the threshold voltage of the body diode. Most of the TSEP based techniques are impractical to apply during operation of PWM power converters used in industrial applications.

In this work, the R_{ON} table of Fig. 9a is used for real-time estimation of the junction temperature, as reported in Fig. 18. The junction temperature is estimated in real time using voltage and current samples, plus the R_{ON} table. Index k indicates the current time sample of the digital controller t_k. This technique was developed at the purpose of testing the SiC power MOSFET modules safely up to their maximum junction temperature of 175°C.

The response of the junction temperature estimate to different current waveforms is reported in Fig. 19. Results for saw-tooth step and sinusoidal current waveforms are presented. The case temperature is constant for all three tests (dashed blue line) and the junction temperature follows the current waveform with the delay of a first order low pass filter.

The good results reported here for SiC MOSFETs also tell that this online temperature monitoring concept applies to Si-MOSFETs, that have a more pronounced dependency of the R_{ON} from the junction temperature [1]. A computationally efficient implementation of the block diagram of Fig. 18 can be obtained by replacing the LUT Θjunction= f(R_{ON}, i_{DS}) with a similar one where v_{DS} is used in place of R_{ON}: $\Theta_{junction}$ = f(V_{DS}, i_{DS}). This releases the MCU from one division operation per sampling cycle.

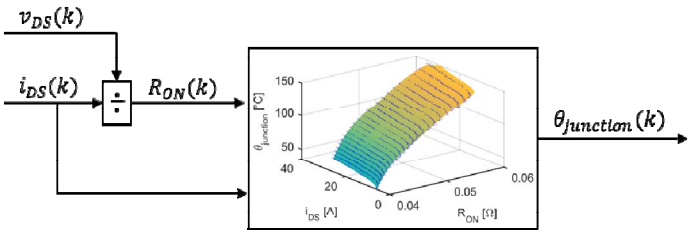

Fig. 18. Block diagram of the on-line temperature monitor.

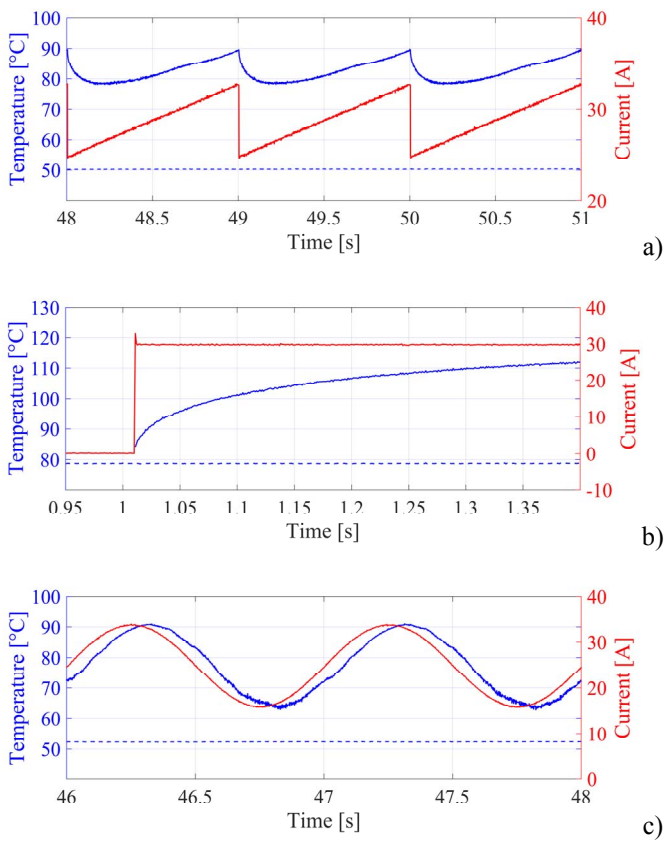

Fig. 19. a),b),c) On-line monitoring of junction temperature for module #1. Continuous blue line represents the estimated junction temperature of SW1L, dashed blue line represents the DBC temperature of the module, and the red line represents the current of the SW1L.

A similar concept of temperature monitoring was proposed in [11] for CoolMOS devices, but without addressing the dependency of R_{ON} from the drain current, that is not negligible here, and using imprecise datasheet data or additional hardware for accurate R_{ON} identification.

F. Repeatability of test

The R_{ON} characterization was repeated three times for module #2 to evaluate the robustness and repeatability of the proposed method. The resulting three look-up tables are used in Fig. 20 for on-line temperature monitoring during the same test, with load current of rectangular type. The junction temperature estimate from the three look-up tables is the same. It is possible to notice how the graphics overlay very well at high current levels, and less perfectly at low current. This is due to the lower precision of V_{ON} and I_{DS} measurements at low currents.

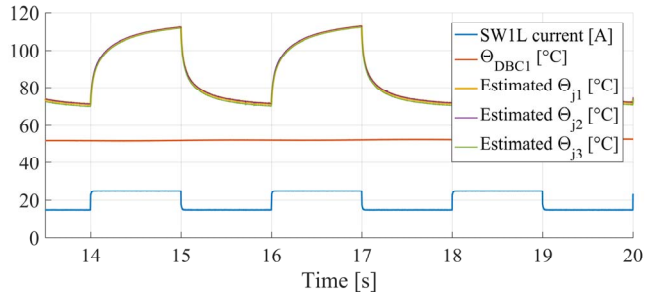

Fig. 20. Temperature estimation using three different look-up-tables, made during three different tests (module #2)

G. *Insensitivity to the DBC temperature sensor position*

Besides the main case temperature sensor NTC1 embedded into the module, an additional sensor named NTC2 was later included for measuring the temperature of the die SW1L in a more intimate way (Fig. 2). The NTC2 has been placed as close as possible to the die (Fig. 21), right under the bonding wires.

The characterization of the module has been repeated using the output of the NTC2 resistor instead of NTC1 as case temperature, and another R_{ON} look-up table has been produced. The comparison of the new look-up table with the old ones tells that the R_{ON} is well estimated in both cases. Subsequently, the on-line temperature monitoring test was repeated to compare the output of the two look-up tables, the one obtained with the NTC1 and the new one obtained with NTC2. Fig. 22 reports the results of the test, made using a current step reference. A similar test is show in Fig. 23, where a sinusoidal current reference was used.

The two tests show that the junction temperature estimates confirm each other correctness, as the respective temperature maps where obtained using different NTC resistors in very different positions for the measurement of the case temperature. The case temperature waveforms, as measured from NTC1 and NTC2, are reported in Fig. 22 and Fig. 23, confirming that NTC2 is way more intimate to the SiC die than NTC1, but far away from correctly estimating the die temperature.

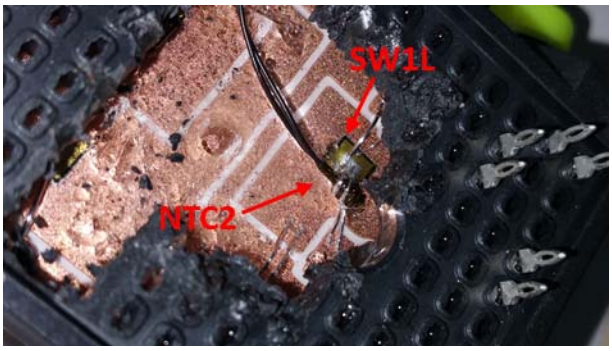

Fig. 21. Local NTC resistor label as "NTC2" in Fig. 2 positioned near the SW1L.

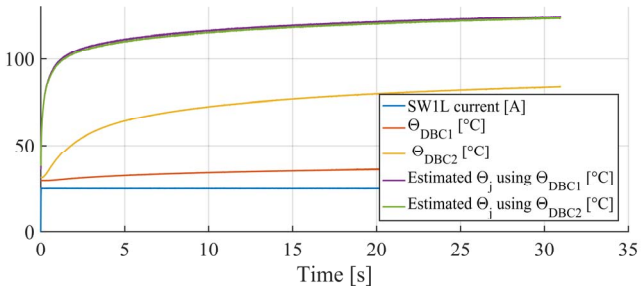

Fig. 22. Junction temperature estimation during a current step of 25 A (module #2)

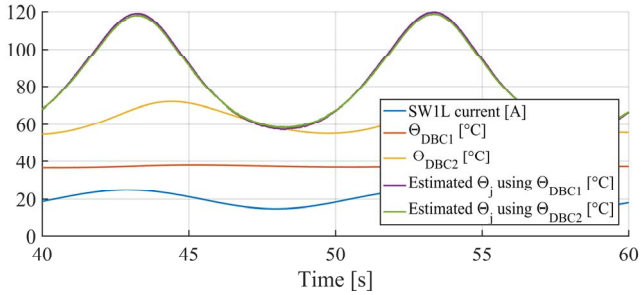

Fig. 23. Junction temperature estimation with sinusoidal current reference (module #2)

The results of Fig. 22 and Fig. 23 also tell that the proposed method for R_{ON} characterization is insensitive to the placement of the NTC sensor within the power module. In particular, the proposed method applies to commercial power modules, taking advantage of standard NTC resistors normally included in the module.

Efforts for using one NTC for direct measurement of the junction temperature fall short: the difference between the junction temperature and the NTC2 temperature is as high as 50 – 70°C or more, depending on operating conditions.

IV. Conclusion

This work presents a setup and a test methodology for the comprehensive characterization of SiC power MOSFET modules. Dealing with *dv/dt* and switching overvoltages, the results of the paper show that the layout of the module and the presence of embedded capacitors can mitigate these problems a lot. The on-state resistance was characterized comprehensively via a new testing sequence, based on current pulses of short duration and measurement of the case temperature with a standard NTC embedded into the module. The inverse of the resistance look-up table was used for on-line estimation of the junction temperature during operation. Future work will focus on the application of the proposed concepts to commercial converters, because no expensive laboratory equipment is involved in the tests, and because, in principle, the characterization procedure can included in the commissioning routines of any converter. The results of this work aim at providing useful insights towards the broader application of SiC MOSFET modules in high-speed AC motor drives.

REFERENCES

[1] B.Callanan,"Application considerations for silicon carbide MOSFETs," Appl. Notes, CREE, Inc., Morrisville, NC, USA, Jan.2011.

[2] G. Wang, F. Wang, G. Magai, Y. Lei, A. Huang and M. Das, "Performance comparison of 1200V 100A SiC MOSFET and 1200V 100A silicon IGBT," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013.

[3] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock and D. J. Costinett, "Evaluation of Switching Performance of SiC Devices in PWM Inverter-Fed Induction Motor Drives," in IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5701-5711, Oct. 2015.

[4] J. Biela, M. Schweizer, S. Waffler and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," in IEEE Transactions on Industrial Electronics, vol. 58, no. 7, pp. 2872-2882, July 2011.

[5] N. Oswald, P. Anthony, N. McNeill and B. H. Stark, "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2393-2407, May 2014.

[6] R. Ruffo and P. Guglielmi, "Simple parameters estimation and precise over-voltage simulation in long cable connected drives," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016.

[7] H. Akagi and I. Matsumura, "Overvoltage Mitigation of Inverter-Driven Motors With Long Cables of Different Lengths," in IEEE Transactions on Industry Applications, vol. 47, no. 4, pp. 1741-1748, July-Aug. 2011.

[8] J. Brandelero, B. Cougo, T. Meynard and N. Videau, "A non-intrusive method for measuring switching losses of GaN power transistors," IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, 2013.

[9] N. Baker, S. Munk-Nielsen, M. Liserre and F. Iannuzzo, "Online junction temperature measurement via internal gate resistance during turn-on," 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, 2014.

[10] Y. Avenas, L. Dupont and Z. Khatir, "Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters—A Review," in IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 3081-3092, June 2012.

[11] A. Koenig, T. Plum, P. Fidler and R. W. De Doncker, "On-line Junction Temperature Measurement of CoolMOS Devices," 2007 7th International Conference on Power Electronics and Drive Systems, Bangkok, 2007.