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Leakage Compensation in Analog Random Modulation Pre-Integration Architectures for Biosignal Acquisition

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Abstract—As Compressed Sensing (CS) emerges as an innovative approach for analog-to-information conversion, more realistic models for studying and coping with the non-idealities of real circuits are required. In this paper we consider the effect of the voltage drop due to leakage currents in the random modulation pre-integration approach, which is the most common CS architecture. In particular we focus on switched capacitor implementations, and we show that leakage currents may significantly alter the acquired information especially when integration time is long as it happens, for example, in biosensing applications. With a simple but realistic circuit model we show that the voltage drop has two contributions. The first is signal independent and causes an offset in the measurement, while the second is signal dependent. To cope with these effects we propose two compensation techniques that ensure signal reconstruction even in the presence of measurement degradation due to leakage.

I. INTRODUCTION

Compressed Sensing (CS) [1] is an innovative approach in the area of analog-to-information (A2I) converters due to the capability of sampling a waveform with a number of measurements that depends on the actual information of the signals rather than on its bandwidth as dictated by the classical Nyquist theorem [2][3][4]. Roughly speaking, CS is capable to achieve signal compression directly during the acquisition of the signal in the analog domain. The fundamental concept behind this approach is *sparsity* [5]. Mathematically, given a proper basis Ψ , each realization x of the input signal class is such that $x = \Psi\alpha$, where the coefficients vector $\alpha \in \mathbb{R}^n$ has only $K \ll n$ non-null entries, where n represents the intrinsic dimensionality of x . In this case, the class of input signals is called K -sparse.

Many circuit architectures for A2I have been proposed so far in the literature [6][7][8]. In this paper we consider the random modulation pre-integration (RMPI) architecture depicted in Fig. 1, first proposed in [9], and in particular we focus on the discrete-time approach, suitable for a switched capacitor (SC) implementation. Given a discrete-time input signal $x_k = x(kT)$, the RMPI collects a set of measurements y_j , $j = 1, 2, \dots, m$, by projecting x on a set of sampling vectors p_j , i.e., $y_j = \langle p_j, x \rangle$. In the discrete-time domain this is achieved by means of the numerical integration

$$y_j = \langle p_j, x \rangle = \sum_{k=1}^N p_{j,k} x_k$$

where $p_{j,k}$ is the k -th element of p_j , and where N is defined as the number of integration steps corresponding to a time window $T_W = NT$. Interestingly enough, SC implementations of RMPI systems can be realized with very simple architectures assuming binary antipodal sampling vectors, i.e. $p_{j,k} \in \{-1, +1\}$. With such an assumption, the multiplication is reduced to a simple sign inversion that can be achieved with a proper switches configuration [7].

It is important to note that when considering low-bandwidth input signals, both T and N are large (the latter is usually large to obtain high compression rates), resulting in a very long integration window T_W . The aim of this paper is to analyze in details the behavior of real RMPI circuits in this case. This setting is actually quite common [3][10], and is typical for the acquisition of biological signals, including Electrocardiograms (ECG) or Electroencephalograms (EEG), that represent one of the most interesting applications for the CS scenario [3][4][11]. Here, T_W can be in the order of few tenths of a

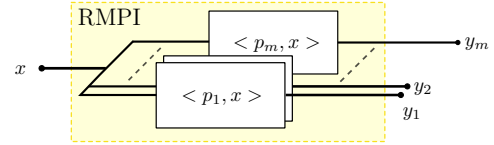


Fig. 1. Block diagram of an RMPI-based CS system.

second, or even a few seconds, so the design is not critical in terms of speed. Conversely, the circuit may greatly suffer from data retention problem. In SC circuits, as in any sample/hold circuit, a long hold time requires either very large sampling capacitors, or the adoption of special techniques to cope with the voltage drop due to leakage currents [12].

In this paper, starting from the differential equations regulating the evolution of the SC integrator both in the sampling and evaluation phases, we develop a simple mathematical model to compute the voltage drop at the analog integrator output nodes. With this model, we are able to compute the expected error on the y_j , and to understand when this error is negligible and when it has to be considered. Furthermore, we develop an *ad-hoc* reconstruction strategy which is capable to keep into account the voltage drop due to leakage.

The paper is organized as follows. In Section II, we introduce the basic circuit that can be used as SC integrator for an RMPI system. We develop a simplified model for the output voltage drop in Section III. Finally, Section IV describes the proposed approach for leakage current compensation. Our result is important since it is the necessary step for the implementation of a digitally assisted RMPI architecture for biosignal processing.

II. MODEL OF THE ANALOG IMPLEMENTATION

The RMPI circuit we consider in this paper is that shown in Fig. 2(a). It is composed by an initial modulator stage (implementing the multiplication between the input signal and the binary antipodal sampling symbols $p_{j,k}$), which is followed by a standard switched-capacitor integrator based on a fully differential architecture, with gain C_s/C_f . Switches are driven by two non-overlapping clock signals ϕ and $\bar{\phi}$. For the sake of simplicity, we assume that the non-overlapping time is negligible. This is not restrictive, since we are assuming to process low-bandwidth signals, where the period T of the ϕ and $\bar{\phi}$ clock signals is sufficiently long.

An additional ϕ_R signal asserts the reset command, which ensures that the charge in the C_f and the differential output voltage are zeroed. The switches necessary for the reset operation are assumed T-shaped (see SW5, SW6, and SW7), thus removing any undesired coupling between the input and output nets.

We will focus our analysis on the critical nodes, i.e. those with high impedance, highlighted with yellow boxes in Fig. 2(a). In particular, we must consider any parasitic element that is connected to these two nodes, as well as any other non-ideality that may alter the accumulated charge. We indicate the voltage at these nodes with $V^+(t)$ and $V^-(t)$, or with their differential and common-mode contributions, defined respectively as $V^D(t) = V^+(t) - V^-(t)$ and

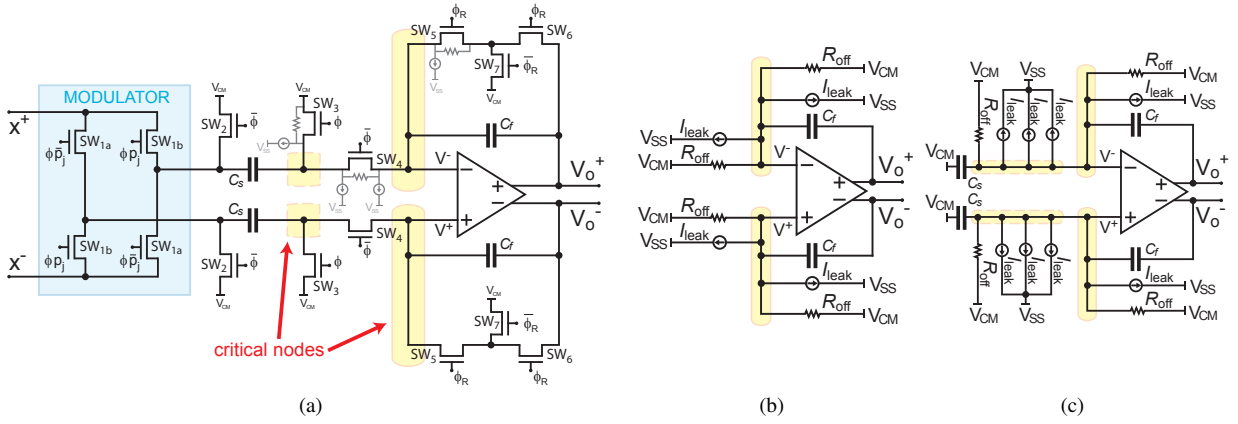


Fig. 2. (a) Basic schematics of a fully differential switched capacitor implementation of a (single channel) RMPI. The highlighted nodes are the high-impedance ones, i.e., that affected by leakage; (b) equivalent circuit during the sampling phase; and (c) equivalent circuit during the evaluation phase,

$V^{CM}(t) = (V^+(t) + V^-(t))/2$. The same notation is used in the following for the differential and common-mode contribution of the voltage pair between any couple of nodes.

The op-amp and all switches are modeled as follows.

Op-amp - It is assumed fully differential, with differential gain A_d , offset V_{off} and controlled common mode output voltage. We can also assume that its bandwidth is large enough to ensure that the transient response time is negligible with respect to T , so that

$$\begin{cases} V_o^D(t) = A_d (V^D(t) - V_{off}) \\ V_o^{CM} = V_{CM} \end{cases} \quad (1)$$

where V_{CM} is the common mode reference voltage.

Switches - They are assumed to be simple NMOS transistors, which is a common choice for leakage minimization purposes. In the OFF state, they are modeled as a resistance R_{off} between source and drain, and two current sources I_{leak} respectively from source and drain to bulk, to model the reverse leakage current of the source/bulk and drain/bulk junctions. The leakage current can be considered constant, since the voltage of the critical nodes is expected to have very small variations due to the virtual short circuit imposed by the op-amp. In the ON state we assume that the channel resistance R_{on} is negligible, and switches are modeled as a current source $2I_{leak}$. With these assumptions, we can analyze the evolution of the circuit in its three different phases, namely *reset*, *sampling* and *evaluation*.

During the reset phase (ϕ_R high) the op-amp outputs and inputs are shorted by SW_5 and SW_6 , i.e., $V_o^-(t) = V^+(t)$ and $V_o^+(t) = V^-(t)$. Neglecting the transient time for discharging C_f , the output voltage is constant and expressed by

$$V_o^D(t) = -\frac{A_d}{1 + A_d} V_{off} \quad (2)$$

which can be reasonably approximated as $V_o^D(t) \approx 0$.

In the sampling phase (ϕ high) the C_s are charged at $X^+ - V_{CM}$ or $X^- - V_{CM}$ depending on p_j through switches SW_1 (either *a* or *b*) and SW_3 , while SW_4 is open thus disconnecting the C_s from the critical nodes V^+ and V^- . The equivalent circuit for the op-amp input nodes is depicted in Fig. 2(b), and the evolution is regulated by equations

$$\begin{aligned} 2I_{leak} + 2\frac{V^-(t) - V_{CM}}{R_{off}} + C_f \frac{d}{dt} (V^-(t) - V_o^+(t)) &= 0 \\ 2I_{leak} + 2\frac{V^+(t) - V_{CM}}{R_{off}} + C_f \frac{d}{dt} (V^+(t) - V_o^-(t)) &= 0 \end{aligned} \quad (3)$$

The solution of the differential problem given by (1) and (3) is given

by

$$V^{CM}(t) = V^{CM0} + (V^{CM0} - V_{CM} + R_{off} I_{leak}) \left(1 - e^{-\frac{2}{R_{off} C_f} t}\right) \quad (4)$$

$$V_o^D(t) = V_o^{D0} - (V_o^{D0} + A_d V_{off}) \left(1 - e^{-\frac{2}{(1+A_d) C_f R_{off}} t}\right) \quad (5)$$

where V^{CM0} and V_o^{D0} are the voltage levels that can be found at the beginning of the sampling phase.

During the evaluation phase ($\bar{\phi}$ high), SW_2 and SW_4 are closed, and the charge accumulated in the C_s in the preceding sampling phase is transferred to the C_f . After a transient assumed negligible with respect to T , the circuit evolution is regulated by the equivalent circuit of Fig. 2(c), i.e. by equations

$$\begin{aligned} 4I_{leak} + 2\frac{V^-(t) - V_{CM}}{R_{off}} + C_f \frac{d}{dt} (V^-(t) - V_o^+(t)) + \\ + C_s \frac{d}{dt} (V^-(t) - V_{CM}) &= 0 \end{aligned} \quad (6)$$

$$\begin{aligned} 4I_{leak} + 2\frac{V^+(t) - V_{CM}}{R_{off}} + C_f \frac{d}{dt} (V^+(t) - V_o^-(t)) + \\ + C_s \frac{d}{dt} (V^+(t) - V_{CM}) &= 0 \end{aligned}$$

and the evolution is given by

$$V^{CM}(t) = V^{CM0} + (V^{CM0} - V_{CM} + 2R_{off} I_{leak}) \left(1 - e^{-\frac{2}{R_{off}(C_s + C_f)} t}\right) \quad (7)$$

$$V_o^D(t) = V_o^{D0} + \frac{C_s}{C_f} p_{j,k} X_k + (V_o^{D0} + A_d V_{off}) \left(1 - e^{-\frac{2}{(C_s + C_f) R_{off} + A_d C_f R_{off}} t}\right) \quad (8)$$

where V^{CM0} , V_o^{D0} are the voltage levels at the beginning of the evaluation phase. Furthermore $X_k = x^+(kT) - x^-(kT)$ and $p_{j,k}$ are, respectively, the value of the differential input signal and of the j -th sampling sequence at the end of the previous sampling phase.

III. MODEL OF THE VOLTAGE DROP

The equations describing the evolution of the integrator developed in the previous section can be combined to study the evolution of the RMPI circuit of Fig. 2(a). Let us consider that the reset phase ends at $t = 0$, and that a sampling and an evaluation phases are executed at each period T . Similarly to what we did for the input signal x ,

we refer to the output voltage at the end of the k th evaluation phase with $V_{o,k}^D = V_o^D(kT)$. We also apply a similar notation to all other circuit voltages.

In an ideal RMPI system (i.e., based on an ideal SC integrator) the output voltage is regulated by the well known equations

$$V^{CM}_k = V_{CM} \quad (9)$$

$$V_{o,k}^D = V_{o,k-1}^D + \frac{C_s}{C_f} p_{j,k} X_k \quad (10)$$

hence, the measurement y_j results

$$y_j = V_{o,N}^D = \frac{C_s}{C_f} \sum_{k=1}^N p_{j,k} X_k \quad (11)$$

In a more realistic system, assuming that switches are properly driven, we can get the actual evolution of the input common mode using (4) and (7), while with (5) and (8) we can obtain evolution of the differential output.

Common mode: independently of the initial conditions, the common mode settles at $V_{CM} - R_{\text{off}} I_{\text{leak}}$ or $V_{CM} - 2R_{\text{off}} I_{\text{leak}}$ depending on the phase, with a time constant which may be comparable with T . Assuming that the voltage level $V_{CM} - 2R_{\text{off}} I_{\text{leak}}$ is in the op-amp common mode range, this does not cause any problem to the integrator.

Differential output: the actual evolution of V_o^D includes two exponential terms with very large time constant due to the presence of A_d . For this reason, it makes sense to linearize these terms, by approximating $1 - e^{-\xi} \simeq \xi$. With this assumptions, and also considering that $A_d \gg 1$, we get that the system evolution is not depending on the duration of the sampling and evaluation phase individually, but only on the period T , more specifically

$$V_{o,k}^D \approx V_{o,k-1}^D + \frac{C_s}{C_f} p_{j,k} X_k - \left(\frac{2V_{o,k-1}^D}{A_d C_f R_{\text{off}}} + \frac{V_{\text{off}}}{C_f R_{\text{off}}} \right) T \quad (12)$$

By comparing (10) with (12), we can find an additional term which represents the voltage drop due to leakage. This term has a signal dependent component, regulated by the coefficient $\alpha = \frac{2}{A_d C_f R_{\text{off}}}$, and a signal independent one, regulated by $\beta = \frac{V_{\text{off}}}{C_f R_{\text{off}}}$. Note that with the assumed fully differential model, the evolution of V_o^D is completely independent of I_{leak} . With this notation, we have

$$\begin{aligned} V_{o,0}^D &= 0 \\ V_{o,1}^D &= \frac{C_s}{C_f} p_{j,1} X_1 - \beta T \\ V_{o,2}^D &= \frac{C_s}{C_f} p_{j,2} X_2 + \frac{C_s}{C_f} p_{j,1} X_1 (1 - \alpha T) - (2 - \alpha T) \beta T \\ &\dots = \dots \end{aligned}$$

and thus

$$\hat{y}_j = V_{o,N}^D = \frac{C_s}{C_f} \sum_{k=1}^N (1 - \alpha T)^{N-k} p_{j,k} X_k - \frac{\beta}{\alpha} \left(1 - (1 - \alpha T)^N \right) \quad (13)$$

that is the expected output for a single RMPI channel.

To verify the correctness of our model, the circuit of Fig. 2(a) has been simulated with SPICE. We considered an ideal op-amp described by (1) with $A_d = 10^5$ and $V_{\text{off}} = 50 \mu\text{V}$, we used $C_s = C_f = 1 \text{ pF}$, while switches are designed as ideal SPICE switches, with given R_{on} and R_{off} , and with an additional current generator I_{leak} to each terminal, modeling leakage currents. The values of R_{on} , R_{off} and I_{leak} are strongly depend on the adopted technology, and a realistic estimation is quite difficult. Here, we have considered $I_{\text{leak}} = 5 \text{ pA}$, $R_{\text{on}} = 1 \Omega$ and $R_{\text{off}} \in \{0.2, 0.5, 1\} \text{ G}\Omega$. The integration step T is taken equal to 10 ms and the considered input signal is a sum of

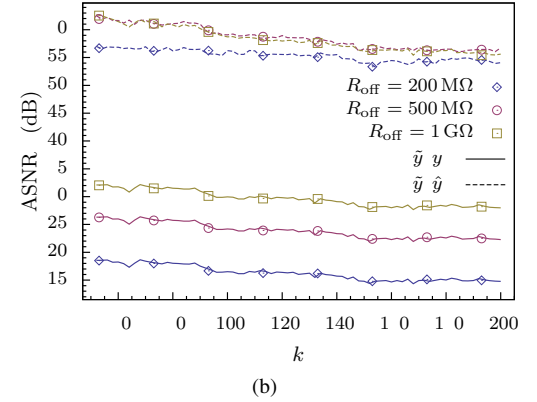
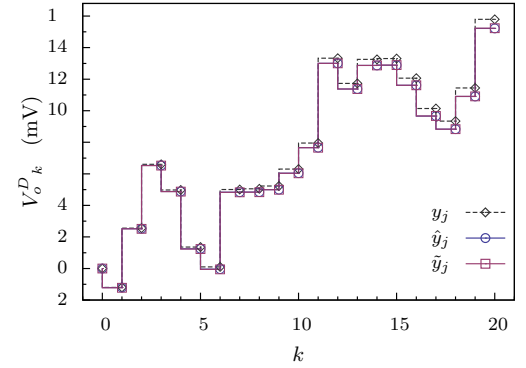


Fig. 3. (a) Short circuital simulation, showing the simulated output integrator voltage \tilde{y}_j compared with the expected one according to the ideal model y_j and the expected one according to our model \hat{y}_j ; and (b) Average SNR for \tilde{y}_j with respect to y_j and \hat{y}_j , for different integration steps k and for $R_{\text{off}} = 200 \text{ M}\Omega$ (corresponding to $\alpha = 0.1$, $\beta = 2.5$), $R_{\text{off}} = 500 \text{ M}\Omega$ ($\alpha = 0.04$, $\beta = 0.1$) and $R_{\text{off}} = 1 \text{ G}\Omega$ ($\alpha = 0.02$, $\beta = 0.05$).

5 sinusoidal or cosinusoidal functions with different amplitudes and frequencies chosen randomly between 1 Hz and 50 Hz. The output of the simulated circuit after N integration steps is indicated with \tilde{y}_j .

Simulation results are shown in Fig. 3(a) and Fig. 3(b). Fig. 3(a) shows an example of the evolution of \tilde{y}_j limited to the first 20 steps with $R_{\text{off}} = 200 \text{ M}\Omega$, compared to y_j and \hat{y}_j estimated by our model. As expected, the deviation between the ideal case and the simulated one is increasing in k , while the our model matches the output of the SPICE simulation. Note that the deviation between ideal and simulated case depends on both α and β values. We here chose to vary only R_{off} implicitly considering different α and β values.

To quantify the adherence between simulation results and the developed model, we introduce the Average Signal to Noise Ratio (ASNR) between a set of simulated measurements a and the expected ones b as follow

$$\text{ASNR}(a, b) = \mathbf{E}_{a,b} \left[\left(\frac{\|a\|_2}{\|a - b\|_2} \right)_{\text{dB}} \right]$$

where $\|\cdot\|_2$ is the standard l_2 norm. In Fig. 3(b) we show the $\text{ASNR}(\tilde{y}_j, y_j)$, solid lines, and $\text{ASNR}(\tilde{y}_j, \hat{y}_j)$, dashed lines, for the three simulated values of R_{off} and over 300 different sampling sequences. $\text{ASNR}(\tilde{y}_j, y_j)$ is between 15 dB and 30 dB for all values of k , while the proposed approach ensures an additional 30 dB with respect to the ideal model.

IV. LEAKAGE EFFECT COMPENSATION

Let us indicate with y a vector composed by m different projections on m different sampling functions such that $y = C_s/C_f P X = C_s/C_f P \Psi \alpha$, where the sampling functions are organized in the rows

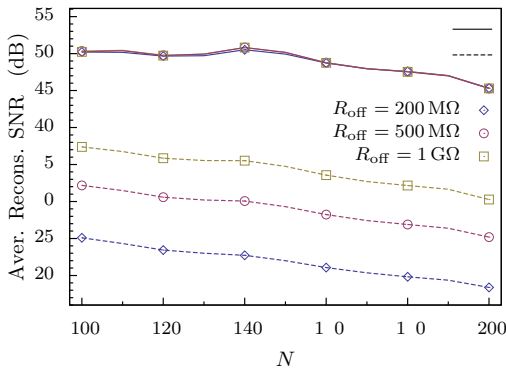


Fig. 4. Average Reconstructed SNR for the simulated CS system using Offset Compensation (OC) only and both OC and Signal-Dependent Compensation (SDC), for different integration windows size and for $R_{\text{off}} = 200 \text{ M}\Omega$ (corresponding to $\alpha = 0.1, \beta = 2.5$), $R_{\text{off}} = 500 \text{ M}\Omega$ ($\alpha = 0.04, \beta = 0.1$) and $R_{\text{off}} = 1 \text{ G}\Omega$ ($\alpha = 0.02, \beta = 0.05$). The average was done over 3000 different trials related to 3000 different random sequences $p_j \in \mathbb{R}^N$ generated as a collection of independent and identically antipodal random sequences.

of the P matrix. Following this notation, the standard CS approach [5][13] guarantees that the input signal can be reconstructed from y by solving an optimization problem that looks for the sparsest vector α satisfying constraint $y = C_s/C_f P \Psi \alpha$ where m must be greater than $4K \log(n/K)$ [13].

Following our model, summarized by (13), the expected measurement vector \hat{y} is instead expressed by:

$$\hat{y} = \frac{C_s}{C_f} \hat{P} X - \hat{y}_{\text{off}} = \frac{C_s}{C_f} \hat{P} \Psi \alpha - \hat{y}_{\text{off}} \quad (14)$$

where the elements of the matrix $\hat{P} \in \mathbb{R}^{m \times N}$ are given by $(1 - \alpha T)^{N-k} p_{j,k}$ and \hat{y}_{off} is a vector with constant entries equal to $\beta/\alpha (1 - (1 - \alpha T)^N)$. This means that, with respect to an ideal system, there are two causes of error. The first is a simple offset \hat{y}_{off} , that linearly increases with N . The second is a signal dependent error that is included in the \hat{P} matrix.

To check the effect of these two errors, and whether they can be effectively compensated, we used the same SPICE setup described in the previous section to simulate of an entire CS acquisition system. The described input signal x can be considered in fact sparse assuming that Ψ is the Fourier basis with $n = 100$ and with sparsity $K = 5$. Simulations are performed using N ranging from 100 to 200, i.e., with a T_W ranging from 1 s to 2 s. We set m as the lowest integer greater than $4K \log(n/K)$.

We propose here two compensation techniques. The first is the Offset Compensation (OC) and simply consists in removing the signal independent error \hat{y}_{off} in (14). Note that the estimation of \hat{y}_{off} is quite simple and this technique can be easily apply to every system even without a knowledge of the underlying voltage drop model. Simulation results, averaging over 3000 different random sampling sequences, are shown in the dashed lines of Fig 4, and show that, depending on the system parameters, it is possible to recover the signal with an Average Reconstructed SNR ranging from 20 dB to 40 dB. Despite simple, this technique represents a noteworthy advantage with respect to the case when no compensation is used, as it still ensures that reconstruction is achieved. It is in fact important to notice that, despite the number of measurement m is larger than what is theoretically needed to ensure reconstruction (i.e. $4K \log(n/K)$) the presence of an uncompensated offset would completely destroy the reconstruction ability of the system.

Better performance can be achieved by additionally considering the Signal Dependent Compensation (SDC), i.e., by considering the actual \hat{P} measurement matrix instead of the ideal on P . With this technique (solid lines in Fig. 4) the achieved reconstruction SNR is

increased up to 50 dB, with a very weak dependence on the system parameters and on N .

V. CONCLUSION

In this paper we have considered how leakage currents can corrupt measurements in a CS system based on a RMPI architecture. Starting from the model of a fully differential, switched capacitor implementation of a RMPI including all possible leakage sources, we are able to show that the voltage drop due to leakage has two main contributions. The first is a simple offset voltage which linearly increases with the integration time and that can be easily compensated, thus allowing signal reconstruction with an Average Reconstructed SNR at most equal to 37 dB even in presence of a voltage drop due to leakage. However, if we want a higher accuracy in signal reconstruction, we need to compensate also the second contribution, which is signal dependent, and may be coped with altering the projection operator that drives the algorithmic reconstruction. When this is done, the Average Reconstructed SNR is always around 50 dB and does not depend on circuit parameter.

This results is very important since it paves the way for the implementation of a digitally assisted RMPI architecture with leakage compensation technique, which has the potential of being extremely effective for the acquisition of low-bandwidth biosignals.

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