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Ripple-based Power-Line Communication in Switching DC-DC Converters exploiting Switching Frequency Modulation

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***Abstract*—Power-Line Communication (PLC) systems represent a very interesting opportunity for introducing low-cost communication capabilities over already existing power-line wires. In this paper we introduce a PLC technique that can be applied to systems with a DC power bus that employ a switching power converter as main power supply unit. The proposed technique is extremely simple to be implemented, and requires only minor modifications on the main switching converter. As a proof of this, we are capable to implement the proposed PLC in a system composed by commercial DC-DC converter boards without any circuital modification to the boards themselves. Measurements on this test system show the capability to communicate up to about 80 kbit/s with a bit error rate so low as 10^{-5}.**

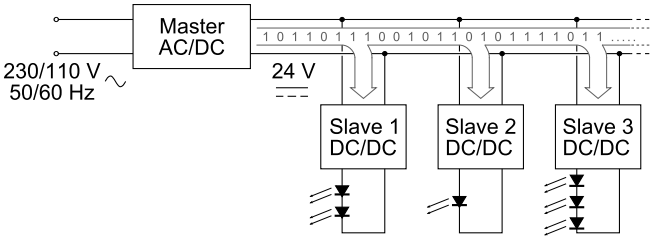

Fig. 1. Possible application scenario for the proposed PLC system.

I. Introduction

Power-line communication (PLC) systems have been introduced with the aim of embedding a data transmission channel in the same wire line used to deliver electrical power. They have been widely investigated in the past [1], since they are extremely appealing in applications where a limited-capacity communication channel is required over long and medium distances, but costs represent a fundamental issue, making thus inconvenient the addition of a supplemental and dedicated wire line.

Despite the fact that PLC are nowadays widely used in very particular systems such as utility digital metering and home automation, two factors are limiting the spreading of these techniques over a wider range of applications. The first one is the impossibility to get a precise and accurate transmission channel model, since it has to be built upon a wire line designed for power transmission, whose length, path and topology are *a priori* unknown, thus limiting the communication speed. The second one is given by the complexity of the standard approach. In fact, the most common solution to add PLC capabilities is based on a dedicated amplifier injecting a high-frequency signal on the power line at the transmission side, and complex signal-processing for extracting and decoding the injected signal at the receiver side [1]. Due to the latter reason, recent researches have been focused in particular on the development of new and simple ways in which injecting and/or decoding the data signal [2], [3].

In this paper, we propose a way to add PLC capabilities to systems based on a single DC power line. The main innovative feature of our approach with respect to other ones specifically designed for the same application [2], [3] is the simplicity. The proposed PLC capability in fact can be implemented at virtually no cost. One possible target application is depicted in Fig. 1 and it is given by a LED-based lightning system, where a master AC/DC switching converter powers a low-voltage DC bus with many LED lightning devices connected. Since LEDs require a constant-current control, additional smaller switching DC-DC converters are usually employed as slave devices to correctly drive the LEDs. In the proposed scenario, communication is established from the master converter to slave converters, for example, to turn LEDs ON and OFF or set their dimming ratio.

In the proposed system the communication is achieved by means of modulation of the master switching frequency. Transmitted data is recovered by looking at the residual ripple on the DC bus. To this purpose, a very simple architecture that includes a band-pass filter followed by a finite-state digital machine is proposed. In order to test the system, a simplified but realistic implementation built upon commercially available DC-DC boards [4], [5] has been designed and tested. Measurements results confirm the communication capabilities of the system, with a transmission rate of about $80\,\mathrm{kbit/s}$ and a measured bit error-rate (BER) so low as 10^{-5}.

The paper is organized as follows. In Section II we describe the basic working principles of the proposed PLC system. Then, in Section III we detail the architecture we used for testing purposes, showing also the achieved performance in terms of transmission speed and BER. Finally, we draw the conclusion.

II. Basic Principle

The proposed PLC system is based on the modulation of the master converter switching frequency. In particular we consider a continuous-phase frequency-shift keying (FSK) [6] modulation. In this approach, the output instantaneous frequency is changed (with phase continuity) every time symbol T_s accordingly to the symbol to be transmitted. In order to

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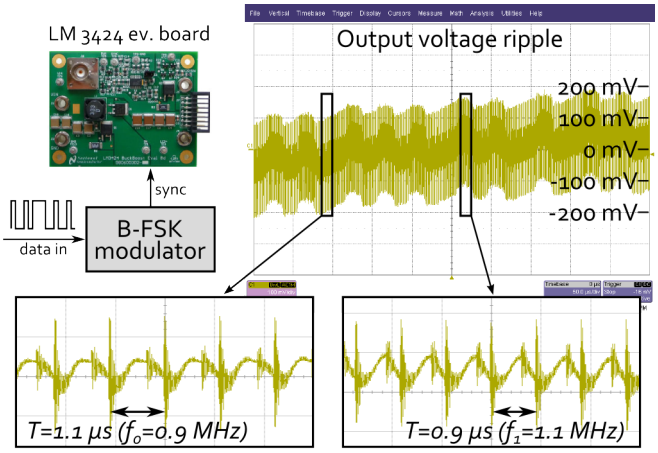

Fig. 2. Example of the output voltage ripple in a system embedding the proposed B-FSK modulation.

limit the complexity and increase the system robustness, we limit ourselves to the binary FSK (B-FSK) case, where all transmitted symbols may be either 0 or 1, and the output instantaneous frequency assumes, respectively, the two values f_0 or f_1. Note that this modulation is equivalent to an *analog* frequency modulation, *i.e.*, in the case of a sinusoidal tone

$$\sin\left(2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau)d\tau\right)$$

where $\xi(\tau) \in \{-1, +1\}$ is the binary driving signal embedding the succession of symbols to be transmitted, f_c is the carrier frequency and Δf the frequency deviation. The output signal instantaneous frequencies are given by $f_0 = f_c - \Delta f$ and $f_1 = f_c - \Delta f$. This approach has two fundamental properties:

- assuming that the employed DC-DC converter is synchronous [7], the implementation is extremely simple. In fact, given an already designed converter, connecting a B-FSK modulator to the external frequency reference pin of the DC-DC controller is enough to add the desired communication capabilities. No other modifications are required to the system, especially regarding the high-power circuitry. This is a great advantage with respect to other solutions where additional power transistors are required [3], in particular for cost reduction purposes;
- it is known [8] that an analog frequency modulation of the switching frequency, under the assumption that $\Delta f \ll f_c$, has no effect on the DC-DC behavior. In particular, the only noticeable effect is a change in the ripple frequency, while all other converter features, including ripple amplitude, are unchanged.

The behavior of a real converter exploiting a B-FSK modulation can be observed in Fig. 2, that shows the measurement of the output voltage ripple of a LM 3424 evaluation board [4] when the DC-DC controller is synchronized with an external B-FSK modulated clock, with $f_0 = 0.9\,\text{MHz}$, $f_1 = 1.1\,\text{MHz}$ and $T_s = 20\,\text{ms}$. As expected, there is not a noticeable difference in the ripple amplitude when the transmitted symbol is 0 or 1, while the ripple frequency is a clear indicator of the transmitted symbol.

In the literature it is known [6] that the FSK coding, despite being not optimal in terms of bandwidth occupation and data

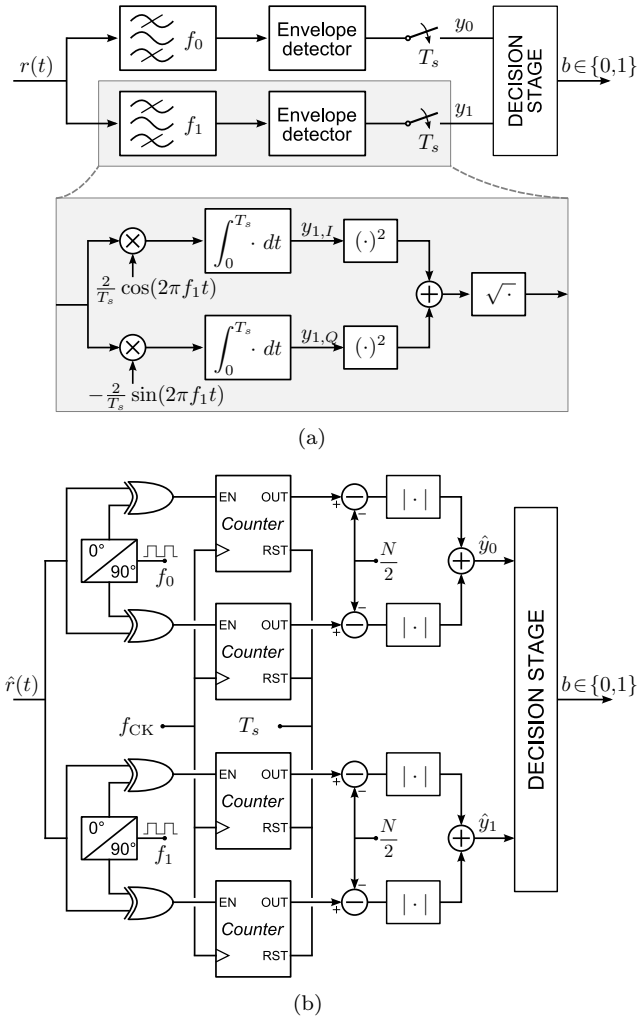

Fig. 3. (a): Correlation receiver architecture for B-FSK modulated signal decoding; and (b): proposed digital approximation.

transmission rate, presents a lot of advantages such as robustness and low hardware complexity, in particular at the receiver side. In fact, one of the most common architecture used for data extraction and decoding is the correlation receiver, that, in the case of a B-FSK, is simply made by two matched filters, centered respectively at frequency f_0 and f_1, followed by two envelope detectors. The two outputs are sampled every T_s, giving y_0 and y_1, that quantify how the input signal $r(t)$ is correlated with two sinusoidal tones at f_0 and f_1. The role of the decision unit is to indicate, accordingly to the higher correlation, if the transmitted symbol b was 0 or 1. This architecture is drawn in Fig. 3(a).

It is also known [6] that in the correlation receiver, under the assumption that f_0 and f_1 are orthogonal (*i.e.*, that $f_0 = k_0/T_s$ and $f_1 = k_1/T_s$, with $k_0, k_1 \in \mathbb{N}$) each of the two blocks measuring either y_0 and y_1 is equivalent to the computational diagram highlighted in Fig. 3(a). In the example of the figure, the input signal $r(t)$ is mixed with two quadrature sinusoidal tones at f_1, and the result is integrated over a time T_s, yielding respectively $y_{1,I}$ and $y_{1,Q}$. The correlation of the input signal with a sinusoidal tone at frequency f_1 is given

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by $y_1 = \sqrt{y_{1,I}^2 + y_{1,Q}^2}$ independently of its phase. In the same way, y_0 can be computed starting from two quadrature sinusoidal tones at f_0, as $y_0 = \sqrt{y_{0,I}^2 + y_{0,Q}^2}$

In our approach we consider the simplified digital approximation of the correlation receiver shown Fig. 3(b). Let us assume to be able to manipulate the ripple signal $r(t)$ and to generate a *digital* representation $\hat{r}(t)$. In this case the analog multiplications with the sinusoidal tones can be replaced with binary multiplications (*i.e.*, an XOR logic processing) with two quadrature square-wave signals. The integrations can also be replaced by counters, clocked at frequency $f_{ck} = N/T_s$, with $N \in \mathbb{N}$. Their purpose is to count for how many clock cycles over a time symbol T_s the XOR output signal is high. After this, counters are reset to zero to start the evaluation of a new symbol. When $\hat{r}(t)$ is uncorrelated with the reference square wave, the output of the counter is approximately $N/2$; when the two signals a strong correlated is detected, the counter output moves either toward 0 or N.

Referring to the notation of Fig. 3(b), $\hat{y}_{0,I} - N/2$ and $\hat{y}_{0,Q} - N/2$ indicate the correlation between $\hat{r}(t)$ and two quadrature square-wave signals at frequency f_0. Similarly, $\hat{y}_{1,I} - N/2$ and $\hat{y}_{1,Q} - N/2$ indicate the correlation between $\hat{r}(t)$ and the two quadrature square-wave signals at frequency f_1. Similarly to the previous case, the decision stage should compare the two values $\sqrt{(\hat{y}_{0,I} - N/2)^2 + (\hat{y}_{0,Q} - N/2)^2}$ and $\sqrt{(\hat{y}_{1,I} - N/2)^2 + (\hat{y}_{1,Q}^2 - N/2)}$; for limiting the hardware complexity of the receiver stage, we propose to evaluate the two functions $\hat{y}_1 = |\hat{y}_{0,I} - N/2| + |\hat{y}_{0,Q} - N/2|$ and $\hat{y}_1 = |\hat{y}_{1,I} - N/2| + |\hat{y}_{1,Q} - N/2|$, that can be easily implemented in any digital finite-state machine, since only addition, subtraction and modulus operations are required.

However, since the proposed receiver is only a simplified approximation of the correlation receiver, performance may be not optimal. In particular, the values of $\hat{y}_0$ and $\hat{y}_1$ are depending on the phase of the input signal. However, as shown in the following section, this is not a limiting factor, and the proposed receiver can be adopted to achieve very good performance with a very simple hardware complexity.

III. Experimental results

Both simulation and measurement results confirm that the approach proposed in Section II can be effectively used to introduce communication capability in the LED lightning system based on a DC bus scenario.

In this section we show measurement results achieved on a simplified but realistic implementation of the system of Fig. 1, where for the sake of simplicity the master converter is replaced with a DC-DC, and only one slave devices has been connected to the DC bus. Furthermore, in order to increase the confidence on our approach, we did not design any *ad hoc* converter, but we limit ourselves to adopt two commercially available DC-DC evaluation boards. More precisely, we used a LM 3424 evaluation board from Texas Instruments [4] as master converter and a LM 5088 evaluation board from Texas Instruments [5] as slave device. The two converters are connected together with two wires of length 2 m and section $1.5\,\mathrm{mm}^2$.

An interesting feature of the employed master converter is the presence of a dedicated sync pin to externally set the switching frequency up to approximately 1 MHz. In our setup, without any circuital modification of the board, we achieved the desired modulation by clocking the converter with a signal generated by an Agilent 33220A arbitrary waveform generator. This instrument has many modulation capabilities, including the desired B-FSK. An example of the output ripple of the LM 3424 board when driven with the B-FSK modulated clock and when transmitting a predefined bit sequence loaded into the waveform generator has already been shown in Fig. 2.

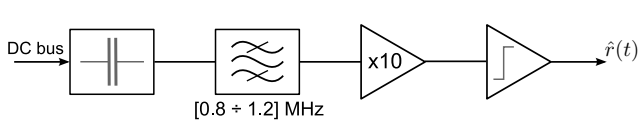

Fig. 4. Analog circuit used to generate the $\hat{r}(t)$ signal to be decoded by the digital correlation filter.

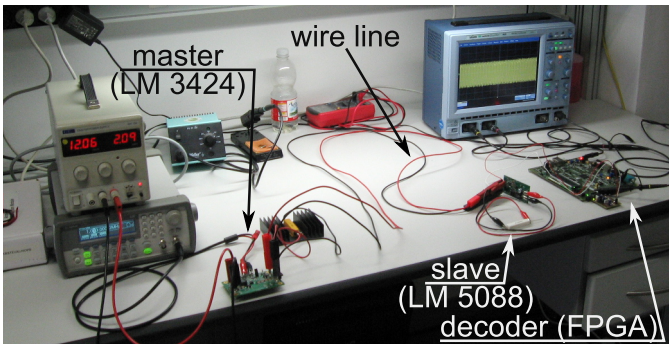

Fig. 5. Overall setup used for measuring performance of the designed PLC system.

The LM 5088 has been used as slave device only to introduce switching noise on the DC bus. Interestingly, this board is running approximately at 250 kHz, that is lower with respect to the master switching frequency. This is intentional, because in this way we are testing the system in the worst case condition, *i.e.*, when the slave switching frequency harmonics are in the same frequency range of the useful ripple signal.

In order to retrieve the transmitted signal with the simplified decoder of Fig. 3(b), we have designed a small full-custom circuit whose block diagram is depicted in Fig. 4 to extract the useful information from the DC bus, and to convert it into a digital signal. To this aim, there is an AC coupling with the DC bus to isolate the ripple signal, that is successively band-pass filtered and amplified, and then processed by a voltage comparator to get a digital signal (ideally, a square waveform either at frequency f_0 or f_1) to be elaborated by the digital correlation receiver. The filter has a $0.8 - 1.2$ MHz bandwidth and a gain equal to 10, and it is designed with a 4^{th} order Butterworth transfer function. Finally, the output of this circuit is fed into a Spartan 3E FPGA that embeds all the digital logic of the receiver of Fig. 3b. The overall setup is shown in Fig. 5.

System parameters have been select as follows. In the implementation of the counters we use the full clock of the FPGA board frequency, that is $f_{ck} = 50\,\mathrm{MHz}$, while we set $f_0 = 50\,\mathrm{MHz}/56 \approx 0.893\,\mathrm{MHz}$ and $f_1 = 50\,\mathrm{MHz}/44 \approx 1.14\,\mathrm{MHz}$ to conveniently generate the two quadrature square waves at f_0 and f_1 by means of simple frequency dividers. Then, we set $T_s \approx 12.3\,\mu\mathrm{s}$, that is the minimum value ensuring

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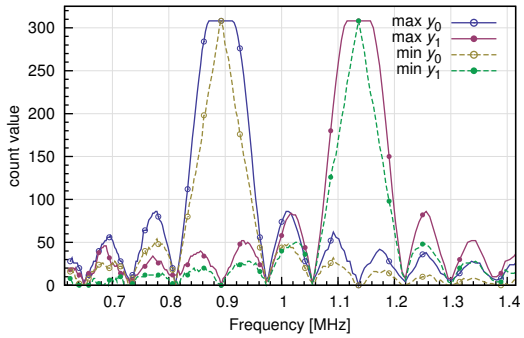

Fig. 6. Theoretically expected performance of the digital correlation receiver of Fig 3(b) in the designed PLC system.

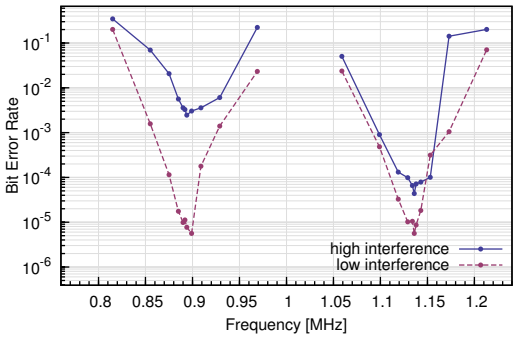

Fig. 7. Measured BER for the designed PLC system.

orthogonality between f_0 and f_1, that leads to $N = 616$. A $10\,\mathrm{bit}$ architecture is therefore enough for computing $\hat{y}_0$ and $\hat{y}_1$.

With these values, we can theoretically compute some of the expected performance of the system. In particular, we are interested in the robustness in terms of deviation of the actual frequencies from the nominal values f_0 and f_1. Since our target is the design of a low-cost low-complexity communication system, we can expect a non-negligible mismatch between the frequencies of the master switching converter and that used in the correlation receiver.

To this aim, we assume that a precise clock reference frequency is used at the receiver side, while only an inaccurate one is available at the transmitter side. In these conditions, it is interesting to look at the theoretical maximum and minimum values assumed by $\hat{y}_0$ and $\hat{y}_1$ in a system without noise perturbations when $\hat{r}(t)$ has a given frequency and an unknown phase shift. Results are plotted in Fig. 6, and reveal a quite high robustness of the system:

- a large deviation in the master switching frequency is tolerated. For example, assuming that the transmitted symbol is 0, the minimum value of $\hat{y}_0$ is sensibly larger than the maximum value of $\hat{y}_1$ (thus ensuring a correct decision even in presence of noise) for a $\pm 2\%$ deviation of the switching frequency with respect to its nominal value f_0. A similar tolerance is observed when the transmitted symbol is 1;
- among the FSK modulations, the B-FSK is the most simple and robust one, since only two symbols are used. Furthermore, the two nominal frequencies f_0 and f_1 are distant enough to avoid any possible not-well defined cases. The frequency range in which $\hat{y}_0$ and $\hat{y}_1$ assume similar values is very far from the nominal values f_0 and f_1, and it is impossible for the master converter to operate in this range solely because of parameter deviation.

Finally, in Fig. 7 we show the achieved BER, measured separately in case of transmission of symbols 0 and 1, for the implemented system under the above used assumption that the clock at the receiver side is generated with high precision, but that the instantaneous switching frequency of the master converter deviates from the nominal values f_0 and f_1.

The measure is achieved in two different conditions. In the first one ("high interference") no particular care has been considered to prevent the slave converter to interfere with the communication system, while in the second one ("low interference") the wiring has been accurately placed, and a small power supply filter has been connected between the LM 5088 slave converter and the DC bus.

In both cases, the feasibility of the communication system is proven. The robustness to frequency mismatch is high as expected from Fig. 6. Furthermore, the measured BER is very low. In particular, in the "low interference" case, we achieved a BER lower than 10^{-5} when the frequency mismatch is negligible. This value is low enough to ensure a reliable communication system, especially if we also consider that no source coding has been applied. Additionally, the achieved transmission rate, given by $1/T_s \approx 82\,\mathrm{kbit/s}$ is very high, especially when compared to similar systems (the prototype proposed in [2] achieves $3.8\,\mathrm{kbit/s}$, while that in [3] $8.3\,\mathrm{kbit/s}$).

IV. Conclusion

In this paper, a novel PLC system for DC buses powered by a synchronous switching converter has been presented. The technique is very simple. At the transmitter side, it is enough to drive the switching converter with a B-FSK capable modulator, while no modifications are required to the power circuitry. Then, a very simple circuit made with a band-pass filter and some digital logic works as signal receiver. Measurements on a system based on commercially available DC-DC converters show very high performance, with a bit error rate of 10^{-5} at a transmission rate of about $80\,\mathrm{kbit/s}$.

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