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A First Implementation of a Semi-Analytically Designed Class-E Resonant DC-DC Converter

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***Abstract*—Resonant power converters represent a step further in the effort of increasing the operating frequency, and consequently the power density, with respect to conventional switching converter architectures. Nevertheless, resonant converters are used only in very specific applications. The main issue is their design that, being not based on a solid mathematical background, results in a non-trivial task. In this paper we present a prototype of a class-E resonant converter with a simplified architecture, allowing both a small size (and so a higher density) and a simple mathematical analysis. Conversely with respect to the state-of-the-art approach, the circuit design is obtained by means of a semi-analytic mathematical approach without any support from circuital simulation. Measurements confirm the performance expected according to the mathematical model, and prove that the design of circuits with the proposed architecture can be effectively achieved with the developed mathematical model.**

I. Introduction

The common trend in recent years power electronics is the increase of circuit power density, defined as the ratio between the maximum deliverable power and the occupied volume. In particular, a key issue in switching dc-dc power converters is the increase of the switching frequency f_s, that allows a design with smaller reactive elements (*i.e.*, inductors and capacitors) and so an overall reduction in circuit size and cost.

However, it is known that the switching losses increase with frequency, and this poses several limitations for conventional architectures, whose operating frequency is actually limited to a few MHz. For this reason, in early 80s [1] resonant converters have been introduced, exploiting common RF design concepts. The ultimate goal was the design of circuits working up to the VHF frequency range ($30 - 300\,\mathrm{MHz}$), with a size small enough to move from the classic single power source scenario to systems with a large number of high-efficiency, low power, small size, distributed power modules.

Nevertheless, the design of a resonant converter is not a trivial task. The state-of-the-art methodology is based on strong simplifying assumptions, allowing a simple design but at the cost of accuracy. To achieve the desired behavior, a refinement of the design by means of additional time-consuming transient simulations and extensive sweeps across circuit parameters is usually necessary.

In this paper we present a $1\,\mathrm{MHz}$ prototype of a resonant converter (more precisely, of a class-E converter), that, conversely with respect to the state-of-the-art approach, has been designed with a semi-analytic approach. Featuring a number of reactive elements smaller compared with other solutions, the developed circuit presents a twofold advantage. On the one hand, its small size allows a further increase in power density. On the other hand, the simplified architecture makes possible the development of a semi-analytic procedure [2] that makes the circuit design a very simple task to achieve, without recurring to any additional refinement based on simulation. Measurements on the prototype are perfectly aligned with expected results, thus proving the effectiveness of the semi-analytic design approach.

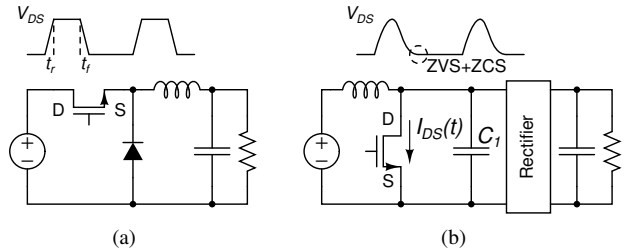

Fig. 1. Typical waveforms for: (a): conventional class-D converter; and (b): resonant class-E converter.

The paper is organized as follows. Section II includes a brief state-of-the-art analysis on class-E converter design. In Section III we present the architecture of the proposed circuit, highlighting the advantages with respect to classical solutions, and proposing the prototype design as case study, whose measurements are shown in Section IV. Finally, we draw the conclusion.

II. State of the Art

The basic principle allowing both high-frequency and high-efficiency operation in resonant converters is transistor waveform shaping, that is roughly sketched in Fig. 1.

A conventional (*hard-switched*) class-D architecture such as the dc-dc buck converter of Fig. 1(a) features rectangular pulses waveforms. In these conditions, one of the limits in pushing the switching frequency up is given by the MOS switch delay time. In particular, let us consider the time required by the MOS switch to turns itself completely ON or OFF, *i.e.*, the time necessary for the drain-to-source voltage V_{DS} to reach a stable value. Actually, two different times can be identified, usually indicated with *rise time* (t_r) and *fall time* (t_f), as shown in Fig. 1(a). Clearly, the longer t_r and t_f, the higher the power loss due to the non-negligible time in which the voltage across the switching device and the current flowing through it are simultaneously high. Another limit is given by the energy stored in the parasitic drain-to-source capacitance C_{DS}, that is almost instantaneously dissipated each turn-on cycle, giving rise to an additional power loss estimable in $\frac{1}{2} f_s C_{DS} V_{DS}^2$. All these effects lower the converter efficiency at high switching frequencies.

In order to cope with the above issues, resonant converters feature the so called *soft-switching* technique, generating sinusoidal-like waveforms by means of additional resonant

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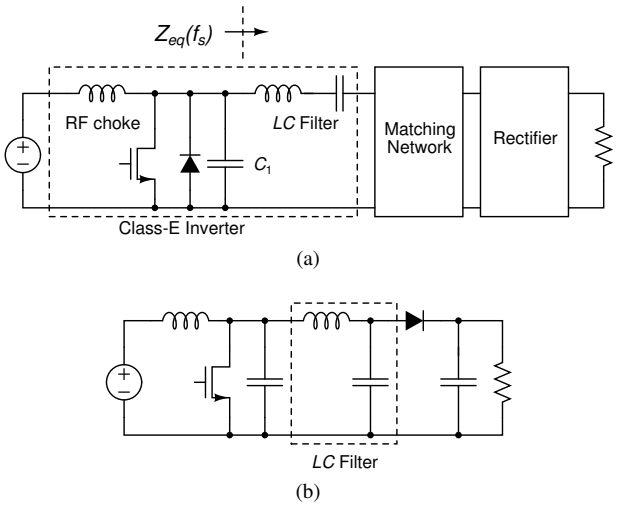

Fig. 2. Standard converter topologies, showing the distinction between inverter and rectifier stages. Schematic (a) comes from [3], while (b) comes from [4].

elements. This is illustrated in Fig. 1(b). In particular, class-E converters aim at synchronizing the zero crossing instant of the drain-source voltage of the MOS switch and of its derivative with the switch turn-on instant. These conditions (*i.e.*, the "optimal class-E operation") are known, respectively, with the name *zero-voltage switching* (ZVS) and *zero-current switching* (ZCS). Roughly speaking, by imposing ZVS we ask that the voltage V_{DS}, that will be forced to zero once the MOS is turned-on, is already zero immediately before the turn-on command. Furthermore, if the current at the inverter side is flowing through a parallel capacitor C_1 during the MOS OFF-state period (following the constitutive relation $I_{C_1} = C_1\, dV_{DS}/dt$) then, if the MOS is turned ON with zero-voltage-derivative, also ZCS occurs. In other words, the current I_{DS}, that is compelled to zero while the MOS is OFF, is still zero immediately after the turn-on command and then gradually increased thus reducing the switching requirements on the MOS itself.

The advantages with respect to the hard-switching approach are clear [1]:

- the effect of t_r and t_f on efficiency is sensibly reduced, since the MOS V_{DS} is now *naturally slowly* changed;
- if we ensure ZVS, *i.e.*, if we turn-on the MOS switch when $V_{DS} = 0$ and no energy is accumulated in the C_{DS}, then no energy can be instantaneously dissipated;
- by ensuring both ZVS and ZCS, neither the V_{DS} nor the I_{DS} suffer from an abrupt change at turn-on instant, thus reducing the device stress.

All the above observations allow the desired increase in the switching frequency and so in the converter power density.

The basic converter topology, of which Fig. 2(a) represents an example taken from [3], is based on two fundamental building blocks: a class-E inverter and a rectifying stage, connected by means of an impedance matching network. The class-E inverter [5], [6] acts like an amplifier, loaded with a properly designed reactive network. An RF choke inductor is usually employed to allow the simplifying assumption that the power supply current is essentially constant. Then, considering a high-Q LC lowpass filter as amplifier reactive load, the output current can be approximated with a sinusoidal tone at the switching frequency f_s. The current flowing either through C_1 (when the MOS switch is OFF) or through the

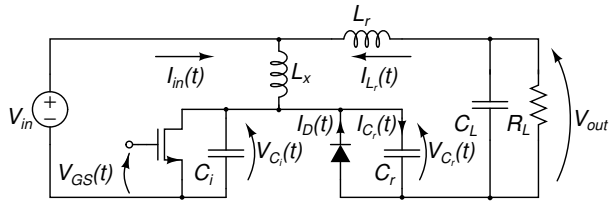

Fig. 3. Schematic of the proposed class-E resonant converter.

MOS itself is simply the superposition of this two currents. Since integrating the current on C_1 allows to know the voltage V_{DS} during the MOS OFF-state, the analysis of the inverter is complete, and it is possible to theoretically design the reactive network to obtain the desired ZVS and ZCS conditions. The ac-dc conversion is accomplished by a resonant rectifier [7], whose design is based on a sinusoidal approximation of its input voltage. The reactive network between the two stages thus performs both an impedance matching from the inverter point of view, and harmonics filtering from the rectifier point of view. Thanks to this sinusoidal approximation one can conveniently split the converter design into two, simplified, procedures: the rectifier design, considering an ideal voltage source as input, and the inverter design, considering the equivalent input impedance of the rectifier at the switching frequency $Z_{eq}(f_s)$ as load.

Nevertheless, the circuit of Fig. 2(a) presents many drawbacks. Mainly, both the RF choke inductor and the high-Q LC filter negatively impact in converter cost and size. However, among the many recent efforts in class-E converter design improvement, only a very few of them were aiming at developing a simpler converter topology. Many of them were targeting the compensation of a variable converter load, by means of either a switching frequency or a duty cycle tuning. A new control strategy, called "burst mode" or simply "on-off control", and new auto-oscillating gate driver topologies have also been introduced [8]. Furthermore, a new ϕ_2 inverter topology was presented in [9], allowing to reduce the V_{DS} peak level and consequently decreasing the transistor stress [10].

One of the few improvements in terms of circuit simplification is found in [4], proposing the circuit of Fig. 2(b). With respect to standard topologies, this circuit features a small number of elements, and, in particular, the RF choke inductor is replaced by a much smaller resonant inductor. However, the accuracy of the suggested design procedure is still affected by sinusoidal approximation, resulting in an appreciable difference between the numerical computed solution and SPICE simulation results, thus requiring additional sweeps across circuit parameters to identify the optimal design point.

The key idea to make a step forward in resonant converters design is to keep a minimal count of reactive components and, at the same time, to increase the accuracy of the design procedure by removing also the sinusoidal approximation. To confirm this, in 2003 the Roadmapping Initiative of the European Center of Power Electronics (ECPE) has stated that mathematical modeling and subsequent multi-objective optimization of a converter system would be the best way to identify the technological barriers and prepare new technologies well in time [11]. In this way, different circuit topologies, control procedures, *etc.* can be analyzed and directly compared with respect to maximum efficiency achievable, power density and costs. The relationship between the technological base and the performance of a system can be formalized through a

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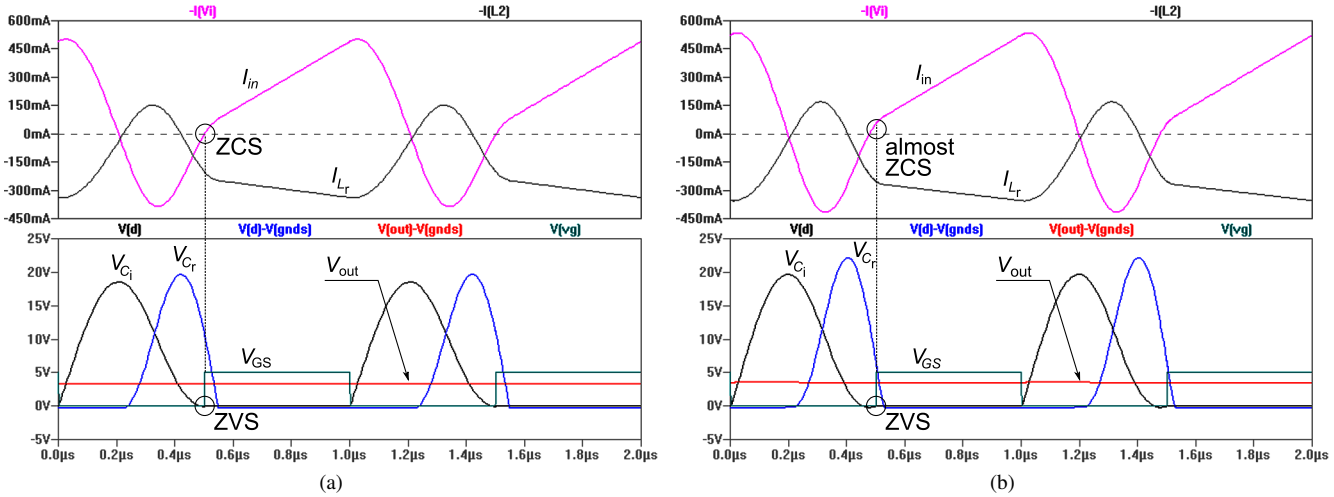

Fig. 4. SPICE simulation of the designed circuit. (a): optimal behavior achieved when active elements are ideal, and passive elements have the exactly computed values; and (b): behavior observed when using a realistic models for active elements, and when passive elements are approximated with available commercial values.

mathematical model that assures the best possible exploration of the Feasible Design Space.

III. Proposed Circuit Design

The schematic of the class-E resonant dc-dc converter considered in this paper is depicted in Fig. 3. With respect to the standard topology of Fig. 2(a), the RF choke inductor is replaced by L_{x} similarly to [4]. Additionally, the LC filter/matching network is removed, and replaced by C_{r} and L_{r}. The advantages of the proposed topology are clear:

- the circuit is composed by the minimum number of reactive elements to achieve the desired behavior. Furthermore, they are not working as RF choke elements, but all of them are oscillating at the switching frequency, and this allows a reduction in their size;
- the circuit features a very low sensitivity to semiconductors (MOS switch and rectifying diode) parasitics, that are absorbed by capacitors C_{i} and C_{r}.

The payload for these circuital advantages is given by the impossibility of applying the state-of-the-art design techniques. However, due to the very simple nature of the converter, a complete and exact semi-analytic procedure for circuit design is possible, and it has been developed in [2] under the assumption of low-loss devices. This opens new possibilities in circuit optimization.

As an example, let us consider the design of a class-E resonant dc-dc converter based on the schematic of Fig. 3 with the following specifications:

$$V_{in} = 5\,\mathrm{V},\ V_{out} = 3.3\,\mathrm{V},\ P_{out} = 600\,\mathrm{mW},\ f_s = 1\,\mathrm{MHz} \tag{1}$$

that leads to $R_L = 18.15\,\Omega$. Despite the fact that class-E converters are usually designed to work at high-frequency, we set a low f_s to ensure low-loss operation even in an off-the-shelves implementation. Then, according to the the semi-analytic design approach in [2], the circuit is readily obtained once we define:

- the design specifications in (1);
- the rectifying diode forward voltage drop ${V_D}^{\mathrm{ON}}$;
- one additional constraint of designer's choice.

The selected rectifying diode is a DB24307 Schottky barrier diode from Panasonic. The forward voltage drop of this diode is very low, measurable in ${V_D}^{\mathrm{ON}} = 0.3\,\mathrm{V}$ in the current range of our interest. Then, we set $L_{\mathrm{x}} = L_{\mathrm{r}}$ as additional constraint. Once all the converter specifications are given, the design procedure leads to the following values:

$$L_{\mathrm{x}} = L_{\mathrm{r}} = 7.04\,\mu\mathrm{H},\ C_{\mathrm{i}} = 3.75\,\mathrm{nF},\quad C_{\mathrm{r}} = 966\,\mathrm{pF} \tag{2}$$

When using the above computed values in a SPICE simulation of the converter circuit embedding only ideal devices (excluding the rectifying diode, for which a non-zero ${V_D}^{\mathrm{ON}}$ is considered) we get the waveforms of Fig. 4(a). In the figure, both ZVS and ZCS operations are clearly identifiable, and the output voltage reaches the desired level $V_{out} = 3.3\,\mathrm{V}$.

For the actual circuit design, low-loss devices have to be considered in order to get adherence of the measurement results with the simulation of Fig. 4(a). First, the selected MOS switch is a IRLML0030TR N-MOS transistor by International Rectifier. This transistor is characterized by a quite high current driving capacity, and a very low turn-on resistance (a ${R_{DS}}^{\mathrm{ON}} < 40\,\mathrm{m}\Omega$ is declared for $V_{GS} = 5\,\mathrm{V}$), thus ensuring low switching losses. Then, the ideal values in (2) for passive devices must be approximated with commercially available values. For L_{x} and L_{r} we use two low-loss $6.8\,\mu\mathrm{H}$ inductors, with high quality factor $Q > 100$ and high self-resonant frequency, so ensuring high performance at $f_s = 1\,\mathrm{MHz}$. To get the desired values for C_{i} and C_{r}, we place many C0G capacitors in parallel. This dielectric grants a very low dissipation factor (DF), defined as the ratio between the accumulated energy and that dissipated into heat. From datasheet, we have $\mathrm{DF} < 0.1\%$ at $1\,\mathrm{MHz}$ testing condition. Furthermore, to cope with the parasitic capacitances of both MOS transistor and rectifyig diode, we use values for C_{i} and C_{r} slightly smaller with respect to the above computed ones. In particular, from the datasheets we know that these (non-linear) parasitic capacitances range from $200\,\mathrm{pF}$ to $80\,\mathrm{pF}$ for the MOS transistor, and from $400\,\mathrm{pF}$ to $50\,\mathrm{pF}$ for the rectifying diode, depending on the applied voltage. The values used in our circuit are $C_{\mathrm{i}} = 3.47\,\mathrm{nF} = 3 \times 1\,\mathrm{nF} + 470\,\mathrm{pF}$ and $C_{\mathrm{r}} = 800\,\mathrm{pF} = 470\,\mathrm{pF} + 330\,\mathrm{pF}$. Finally, we approximate the

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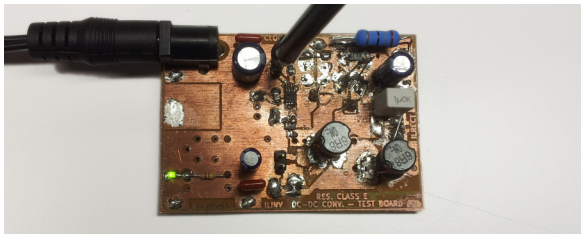

Fig. 5. Photograph of the implemented class-E converter.

load resistance with the nearest commercial value $R_L = 18\,\Omega$. By using the above approximated values for inductances and capacitances, and the actual SPICE models for both MOS transistor and rectifying diode, we get the simulation results depicted in Fig. 4(b). By comparing the obtained results with that of Fig. 4(a) we can observe only small and non-significant differences. The ZVS condition is achieved, while the ZCS condition is not perfectly satisfied, but the current at MOS turn-on instant is still in a perfectly acceptable range to ensure a low device stress. The output voltage level is unchanged. This proves that the proposed architecture is robust enough to tolerate the introduced and unavoidable approximations.

Interestingly, even if the actual computation in the general case is extremely difficult, it is possible to get a formulation for the maximum theoretical efficiency of the proposed architecture under the assumption that all devices but the rectifying diode are ideal and lossless. By defining $I_D(t)$ as the forward current on the diode, and $I_{C_r}(t)$ as the current flowing through the capacitor C_r, we have $I_{L_r}(t) = I_{C_r}(t) - I_D(t)$. Once steady-state operation is achieved, $I_{C_r}(t)$ becomes zero average since C_r is ideal, and in a clock period T we have $\int_0^T I_{C_r}(t) = 0$. Then, if we indicate with E_{out} the energy transferred to the load in a period T, and with E_D the energy dissipated in T on the diode, the converter efficiency is given by $\eta^{MAX} = \frac{E_{out}}{E_{out}+E_D}$, where

$$E_{out} = -\int_0^T V_{out}\, I_{L_r}(t)\, dt = V_{out} \int_0^T I_D(t)\, dt$$

and $E_D = \int_0^T V_D{}^{\mathrm{ON}} I_D(t) dt$. Now it is easy to compute

$$\eta^{MAX} = \frac{V_{out} \int_0^T I_D(t)\, dt}{V_{out} \int_0^T I_D(t) dt + V_D{}^{\mathrm{ON}} \int_0^T I_D(t) dt} = \frac{1}{1 + V_D{}^{\mathrm{ON}}/V_{out}} \quad (3)$$

i.e., the maximum theoretically efficiency depends only on the output voltage and on the rectifying diode forward voltage drop.

For the considered design, $\eta^{MAX} = 91\%$. This value is also confirmed by SPICE simulation results.

IV. Prototype Measurements

Following the design procedure of Section III, we have implemented a prototype of the dc-dc class-E resonant converter using off-the-shelf devices. The photograph of the converter is depicted in Fig. 5.

When the working frequency is set to $f_s = 1\,\mathrm{MHz}$, and with $V_{in} = 5.0\,\mathrm{V}$, we measure an output voltage level $V_{out} = 3.4\,\mathrm{V}$ and an average input current $I_{in} = 0.15\,\mathrm{A}$. Whit this data, the measured efficiency is $\eta = 85\%$, that is similar, but reasonably a bit lower, than that computed in (3), due to losses in actual devices (in particular, in passive devices) that have not been taken into account in the design of Section III.

Finally, the observed waveforms of the voltage signals in the circuit are plotted in Fig. 6. By comparing them with the

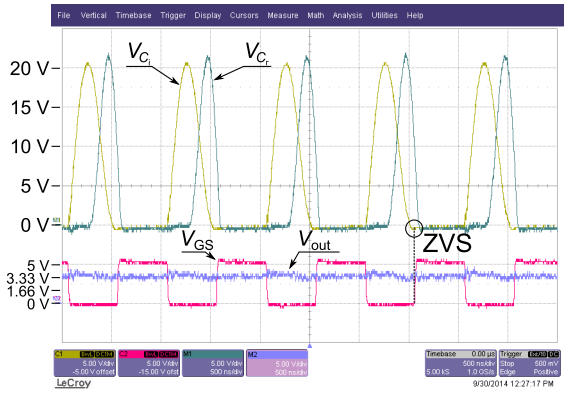

Fig. 6. Measured waveforms for the implemented class-E converter.

vaweforms of Fig. 4(b) we can see a very good matching. In particular, the ZVS behavior is clearly observable, thus confirming again that the design procedure of Section III can be effectively used in the design of resonant class-E dc-dc converter. The waveforms of the current signals are not shown, since we did not include any sensing resistor in order to not reduce the circuit overall efficiency nor add any perturbation to its steady-state operation point.

V. Conclusion

In this paper, a new class-E resonant converter architecture is presented. The proposed circuit features a low elements count, thus allowing either a high power density and a simplified mathematical model. In fact, conversely from the state-of-the-art approach, it is possible to get the converter design by means of a semi-analytic procedure, without recurring to additional and time consuming simulations. Measurements on a designed prototype confirm the effectiveness of the innovative design methodology.

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