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Design of an 87% Fractional Bandwidth Doherty Power Amplifier Supported by a Simplified Bandwidth Estimation Method / Moreno Rubio, Jorge Julian; Camarchia, Vittorio; Pirola, Marco; Quaglia, Roberto. - In: IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. - ISSN 0018-9480. - STAMPA. - 66:3(2018), pp. 1319-1327. [10.1109/TMTT.2017.2767586]

Availability:

This version is available at: 11583/2693890 since: 2018-03-07T10:42:54Z

Publisher:

IEEE Piscataway

Published

DOI:10.1109/TMTT.2017.2767586

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Design of an 87% Fractional Bandwidth Doherty Power Amplifier Supported by a Simplified Bandwidth Estimation Method

Jorge Julian Moreno Rubio, Vittorio Camarchia¹, *Senior Member, IEEE*,
 Marco Pirola, *Member, IEEE*, and Roberto Quaglia², *Member, IEEE*

Abstract—This paper presents a novel technique for the design of broadband Doherty power amplifiers (DPAs), supported by a simplified approach for the initial bandwidth estimation that requires linear simulations only. The equivalent impedance of the Doherty inverter is determined by the value of the output capacitance of the power device, and the Doherty combiner is designed following this initial choice and using a microstrip network. A GaN-based single-input DPA designed adopting this method exhibits, on a state-of-the-art bandwidth of 87% (1.5–3.8 GHz), a measured output power of around 20 W with 6 dB back-off efficiency between 33% and 55%, with a gain higher than 10 dB. System-level measurements prove the linearizability of the designed Doherty amplifier when a modulated signal is applied.

Index Terms—Broadband matching networks, GaN-based FETs, wideband microwave amplifiers.

I. INTRODUCTION

THE Doherty power amplifier (DPA) is widely adopted in mobile base-stations for its ability in amplifying modulated signals with high peak-to-average power ratio (PAPR) while maintaining high efficiency [1], [2]. Several licensed bands are assigned to 4G systems, especially in the 1.6–3.5 GHz range, making the design of DPAs able to operate on different bands of great interest for the provision of a single hardware easily configurable to the specific frequency adopted in the small cell.

Unfortunately, DPAs are affected by several bandwidth limiting factors that extend beyond the typical broadband matching problem in combined PAs and, as a consequence, the scientific and industrial communities have spent a considerable effort in investigating techniques for bandwidth improvement in DPAs. Most of the relevant papers on this

topic focus their attention on the output combiner. The work in [3] analyzed the impact of the output capacitance in an LDMOS DPA, while the work in [4] focused on the impedance inverter in a GaN DPA, proposing an alternative output combiner for improved bandwidth. A comprehensive analysis of the bandwidth limitations given by the output section of DPAs was discussed in [5], where two prototypes were designed according to a broadband matching achieved following a simplified real frequency technique. Moreno *et al.* [6] proposed a GaN-based 3–3.6 GHz Doherty that exploited output compensation networks. In [7], the bandwidth of the classical DPA was expanded using a quasi-lumped quarter-wave transmission line and the Klopfenstein taper. A modified output combiner, based on a nonterminated branch line coupler, was proposed in [8], and then has been improved in [9] to achieve a record bandwidth of 83%. In [10], a broadband GaN DPA, operating on the 1.6–2.4-GHz band, has been designed focusing the attention on the auxiliary amplifier output in order to maximize the power utilization of the adopted devices. A “postmatching” architecture was adopted in [11], obtaining a 42% bandwidth in a 40-W GaN-based DPA. The work in [12] showed a sequential PA using a Doherty-type modulation, achieving a 30% bandwidth adopting GaN devices. A very recent contribution [13] has demonstrated a 50% bandwidth DPA adopting a systematic continuous mode approach [14]. State-of-the-art bandwidth has been achieved through the use of the so-called “Digital Doherty,” where the main and auxiliary inputs are driven with independent modulated signals [15], [16], and proper digital signal conditioning accounts for the output section bandwidth limitations. On the other hand, the utilization of separated baseband processing and up-conversion chains asks for a redefinition of the transmitter: in this case, the pros and cons with respect to standard solutions must be carefully evaluated. This paper presents the design, simulation, and characterization of a GaN-based 20-W single-input DPA, showing a state-of-the-art bandwidth of 2.3 GHz (87% fractional bandwidth), ranging from 1.5 to 3.8 GHz. This paper is organized as follows. Section II describes the proposed new design technique, supported by a novel method for simplified bandwidth estimation in the preliminary assessment of the design. Section III describes the application of the design technique to the specific design, while Section IV describes the translation from ideal components to microstrip

Manuscript received August 3, 2017; revised October 3, 2017; accepted October 5, 2017. Date of publication December 1, 2017; date of current version March 5, 2018. This work was supported by the European Union’s Horizon 2020 Research and Innovation Programme through the Marie Skłodowska-Curie agreement under Grant 654987. (*Corresponding author: Roberto Quaglia.*)

J. J. Moreno Rubio is with the Department of Electronics, Universidad Pedagógica y Tecnológica de Colombia, Sogamoso, Colombia (e-mail: jorgejulian.moreno@uptc.edu.co).

V. Camarchia and M. Pirola are with the Department of Electronics, Politecnico di Torino, 10129 Turin, Italy (e-mail: vittorio.camarchia@polito.it).

R. Quaglia is with the Centre for High Frequency Engineering, Cardiff University, Cardiff CF24 3AA, U.K. (e-mail: quagliar@cardiff.ac.uk).

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Digital Object Identifier 10.1109/TMTT.2017.2767586

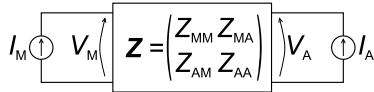


Fig. 1. Basic circuit representation of the DPA output.

and the simulation results. Section V shows the measurements, and finally Section VI draws some conclusions.

II. DESIGN

A. Bandwidth Estimation

The bandwidth of the DPA could be defined as the frequency range F_P on which the saturated output power $P_{OUT,sat}$ is larger than a target $P_{OUT,target}$. However, in this paper, it is also introduced F_L , defined as the frequency range on which the gain compression or expansion in the Doherty region is lower than a target. The DPA bandwidth becomes the intersection $F_P \cap F_L$. The gain compression/expansion can be estimated as the difference between input power back-off (IBO) and output power back-off (OBO), where the back-off is the power range between the Doherty breakpoint and maximum power. This compression figure provides an initial control on the nonlinear distortion focusing on the span of the Doherty region. It has to be recognized that DPA distortion is also affected by other factors, as phase distortion, and in general, it is not limited to the Doherty region only, but it is present at low power due to weak nonlinear effects mainly related to the nature of the active devices [17]–[19]. Despite these limitations in accuracy, defining the range F_L is useful and convenient, because a first assessment of the difference between IBO and OBO can be achieved through the approach proposed in this paper.

In fact, following these guidelines, a simplified bandwidth estimation can be carried out using the scheme in Fig. 1, where the current sources I_M and I_A represent the main and auxiliary devices, respectively, and the two-port \mathbf{Z} matrix represents the output combiner, including the load. This method allows to monitor F_P and F_L through the evaluation of \mathbf{Z} that can be easily obtained by linear simulations running in real time during the tuning or optimization of the circuit elements. This initial bandwidth estimation does not need to rely on nonlinear simulation that can be used instead in a second phase to refine the design.

Potentially, considering fundamental and harmonics would lead to a more accurate approximation of the performance than considering fundamental only. On the other hand, the detection of clipping when considering harmonics is possible but not without a significant added complexity [20]. Moreover, the input harmonic terminations have a strong impact on the effect of output harmonic loads, and in a broadband design, it is very difficult to ensure that input harmonics are shorted or controlled. For these reasons, harmonics are neglected in this simplified analysis. The ac voltage at the device drain terminals can be evaluated as

$$\begin{pmatrix} V_M \\ V_A \end{pmatrix} = \mathbf{Z} \begin{pmatrix} I_M \\ I_A \end{pmatrix} = \begin{pmatrix} Z_{MM} & Z_{MA} \\ Z_{AM} & Z_{AA} \end{pmatrix} \begin{pmatrix} I_M \\ I_A \end{pmatrix}. \quad (1)$$

Assuming devices with maximum current I_{MAX} and ρI_{MAX} for the main and auxiliary devices, respectively, then

$$\begin{aligned} I_M &= i_{1M} I_{MAX} \\ I_A &= i_{1A} \rho I_{MAX} e^{j\phi}. \end{aligned} \quad (2)$$

The current ratio factor ρ is used when a different auxiliary device size is chosen; otherwise, it can be set as one. The parameter ϕ is a frequency-dependent phase delay determined by input splitting and matching, while i_{1M}, i_{1A} are the dimensionless fundamental Fourier components of the current waveform at maximum drive for the main and auxiliary, respectively. For example, in a class B–class B Doherty, both i_{1M}, i_{1A} are equal to 0.5 at each drive level, while in a more typical AB-C configurations, i_{1M}, i_{1A} are drive dependent and in general not identical. The saturated power can be estimated by imposing the device currents at their maximum value. Ideally, with devices without voltage limitations, this would lead to

$$\begin{aligned} V_{M,max} &= I_{MAX}(i_{1M} Z_{MM} + i_{1A} \rho Z_{MA} e^{j\phi}) \\ V_{A,max} &= I_{MAX}(i_{1M} Z_{AM} + i_{1A} \rho Z_{AA} e^{j\phi}). \end{aligned} \quad (3)$$

However, in a more realistic device approximation, in order to avoid top current clipping, it is necessary to maintain the voltage magnitude below $V_{MAX} = V_{DD} - V_K$, where V_{DD} and V_K are the drain bias and knee voltage, respectively [21]. Since the values of the \mathbf{Z} -matrix are fixed, the only way to reduce voltage is by reducing the current that is controlled by the input drive. The effect of drive reduction can be accounted by introducing a current reduction factor σ_x , where x represents the main or auxiliary stage

$$\begin{cases} \sigma_x = \frac{V_{MAX}}{|V_{x,max}|}, & |V_{x,max}| > V_{MAX} \\ \sigma_x = 1, & |V_{x,max}| \leq V_{MAX}. \end{cases} \quad (4)$$

Since we consider the main and auxiliary drive as not independent, the effective current reduction factor at each frequency must be chosen as $\sigma = \min\{\sigma_M, \sigma_A\}$. The effective current at saturation is

$$\begin{aligned} I_{M,sat} &= i_{1M} \sigma I_{MAX} \\ I_{A,sat} &= i_{1A} \rho \sigma I_{MAX} e^{j\phi} \end{aligned} \quad (5)$$

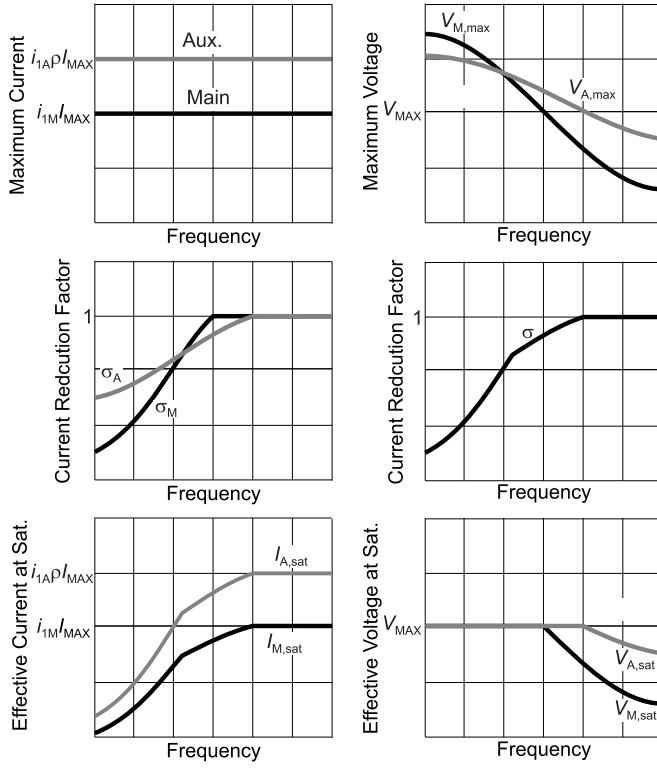
while the effective voltage at saturation is

$$\begin{aligned} V_{M,sat} &= I_{M,sat} Z_{MM} + I_{A,sat} Z_{MA} \\ V_{A,sat} &= I_{M,sat} Z_{AM} + I_{A,sat} Z_{AA}. \end{aligned} \quad (6)$$

Fig. 2 shows an example to clarify the role of σ .

At the Doherty breaking point, the auxiliary is turned OFF ($I_A = 0$) and the main fundamental current is reduced by a factor γ that is related to the power back-off with a square law, according to the simplification in [22]. For example, for a 6-dB Doherty design, $\gamma = 2$. The voltage at the main device is determined as

$$V_{M,back} = \frac{I_{M,sat}}{\gamma} Z_{MM}. \quad (7)$$


 Fig. 2. Graphical interpretation of the current reduction factor σ .

If $V_{M,back} > V_{MAX}$, another current reduction term β must be adopted to avoid current clipping, being

$$\begin{cases} \beta = \frac{V_{MAX}}{|V_{M,back}(f)|}, & |V_{M,back}| > V_{MAX} \\ \beta = 1, & |V_{M,back}| \leq V_{MAX}. \end{cases} \quad (8)$$

The effective back-off current and voltage result as

$$\begin{aligned} I_{M,OBO} &= i_{1M} \frac{\beta \sigma}{\gamma} I_{MAX} \\ V_{M,OBO} &= i_{1M} \frac{\beta \sigma}{\gamma} I_{MAX} Z_{MM}(f). \end{aligned} \quad (9)$$

The output power at saturation and back-off can be calculated, assuming lossless matching networks, as

$$\begin{cases} P_{OUT,sat} = \frac{1}{2} \Re\{V_{M,sat} I_{M,sat}^* + V_{A,sat} I_{A,sat}^*\} \\ P_{OUT,OBO} = \frac{1}{2} \Re\{V_{M,OBO} I_{M,OBO}^*\}. \end{cases} \quad (10)$$

The OBO in decibels is defined as $10 \log_{10}(P_{OUT,sat}/P_{OUT,OBO})$, while the IBO can be evaluated as $20 \log_{10}(V_{in,max}/V_{in,obo})$, where $V_{in,max}$ and $V_{in,obo}$ are the drive voltage needed to generate the maximum and the back-off current, respectively. In a B-B Doherty simplification, $IBO = 20 \log_{10}(\gamma/\beta)$. From these results, the frequency ranges F_P and F_L can be derived according to the matching strategy, i.e., to the calculated \mathbf{Z} matrix.

Moreover, a very rough estimation of the saturated and back-off efficiency can also be carried out, by evaluating the

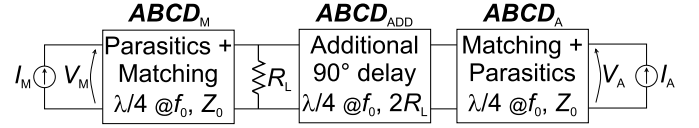


Fig. 3. Block diagram of the designed DPA output.

dc power consumption as

$$\begin{cases} P_{DC,sat} = (i_{0M,max} + i_{0A,max}) V_{DD} I_{MAX} \\ P_{DC,OBO} = i_{0M,obo} V_{DD} I_{MAX}. \end{cases} \quad (11)$$

The Fourier dc current components $i_{0M,max}$, $i_{0A,max}$, and $i_{0M,obo}$ can be calculated according to the conduction angle of the current waveform at effective maximum and back-off conditions. For a B-B simplification, their value is

$$\begin{aligned} i_{0M,max} &= i_{0A,max} = \sigma \frac{1}{\pi} \\ i_{0M,obo} &= \frac{\sigma \beta}{\gamma \pi}. \end{aligned} \quad (12)$$

A first estimation of the bandwidth can be applied to guide the design of the Doherty PA by following these steps.

- 1) Choose a Doherty combiner topology.
- 2) Setup a linear simulation for the \mathbf{Z} -parameters of the combiner, including the output equivalent circuit of the devices.
- 3) Use the equations of this section to evaluate the figures of merit (output power, IBO, and OBO) that determine F_P and F_L .
- 4) Evaluate F_P and F_L and use them as goals for optimization while tuning the combiner's parameters.

After this procedure, the topology can be applied in a full nonlinear simulation for the refining of the Doherty design.

B. Design Strategy

In this section, we present the specific strategy adopted for the design of the Doherty presented in this paper, with the relative bandwidth estimation. The estimation is carried out considering as DPA approximation a class B–class B case, which permits a further simplification with a degradation of accuracy that we consider negligible for our purposes. The \mathbf{Z} can simulated or mathematically transformed from an \mathbf{ABCD} matrix, obtained as the cascade of the \mathbf{ABCD} matrixes of the building blocks composing the proposed Doherty output combiner (see Fig. 3). Identical devices for main and auxiliary are considered, with optimum intrinsic load R_{opt} , while the load impedance at the DPA common node is R_L . The cascade of device parasitics and matching network forms an equivalent impedance inverter, with impedance $Z_0 = (2R_L R_{opt})^{1/2}$, on both main (\mathbf{ABCD}_M) and auxiliary (\mathbf{ABCD}_A) branches. On the auxiliary side, an additional 90° delay is needed (\mathbf{ABCD}_{ADD}), with impedance $2R_L$, to null the impedance inverting effect due to auxiliary device parasitics and matching network. The choice of using a 180° cascade network for the auxiliary output is driven by the difficulty, in the presence of series parasitics, of realizing a 0° output that would probably further benefit the bandwidth.

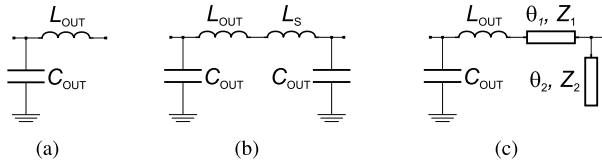


Fig. 4. Design strategy. (a) Simplified device output. (b) Lumped elements' impedance inverter. (c) Semilumped impedance inverter.

As shown in [6], the device output equivalent network can be approximately considered as a current generator shunted with an output capacitance C_{OUT} , and in series with an output inductance L_{OUT} [see Fig. 4(a)]. In our approach, the impedance Z_0 is selected as

$$Z_0 = \frac{1}{Y_0} = \frac{1}{2\pi f_0 C_{OUT}} \quad (13)$$

where f_0 is a reference frequency that corresponds to the center frequency in a narrowband design, while it can be optimized for bandwidth maximization in a broadband design. The values of C_{OUT} and f_0 determine univocally Z_0 and, as a consequence, $R_L = Z_0^2/(2R_{opt})$. Being R_L a real load, it can be matched to the external 50Ω impedance on a very broad bandwidth by means of multisection matching. The Z_0 impedance inverter can be implemented as a Π low-pass filter [see Fig. 4(b)], completing it with a series inductance L_S with impedance value

$$|Z_S| = 2\pi f_0 L_S = Z_0 - 2\pi f_0 L_{OUT} \quad (14)$$

and another shunt capacitor with value C_{OUT} .

In our case, a distributed solution has been preferred for implementation in a microstrip circuit [see Fig. 4(c)] using a short piece of line with arbitrary impedance Z_1 and electrical length $\theta_1 = \sin^{-1}(|Z_S|/Z_1)$ to implement the series inductance, and an open stub with arbitrary impedance Z_2 and electrical length $\theta_2 = \tan^{-1}(Y_0 Z_2)$ to implement the shunt capacitance. \mathbf{ABCD}_M can be built by cascading the elementary \mathbf{ABCD} matrixes of C_{OUT} , L_{OUT} , the series line, and the shunt stub, while the reverse order must be followed to evaluate \mathbf{ABCD}_A .

The additional 90° delay line on the auxiliary side is implemented by means of a transmission line with impedance $2R_L$ and quarter-wave length at f_0 . This delay line works as an auxiliary offset line, showing a high impedance when the auxiliary is turned OFF, but not affecting the impedance matching at saturation [23]. At the input, after a splitter with no delay difference between the output ports, a $50\text{-}\Omega$ transmission line on the main side imposes a $\phi = (\pi/2)(f/f_0)$ to provide a perfect phase balance of output currents at f_0 .

In the proposed combiner topology, the available free parameters that can be tuned or optimized to maximize the bandwidth are f_0 , Z_1 , and Z_2 , while the other parameters are derived using the equations of this section.

III. SPECIFIC CASE DESIGN

The proposed power amplifier is based on the CGH40010F GaN HEMT from Wolfspeed. The bias voltage is $V_{DD} = 28 \text{ V}$,

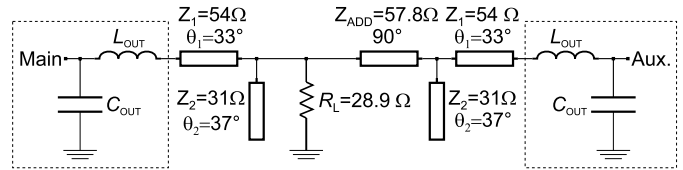
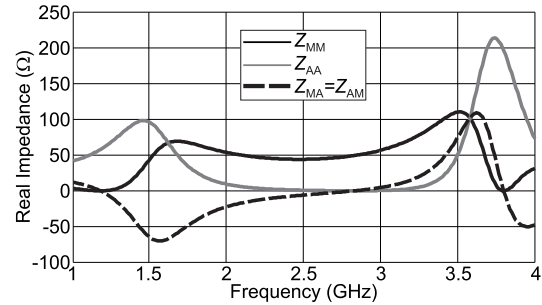
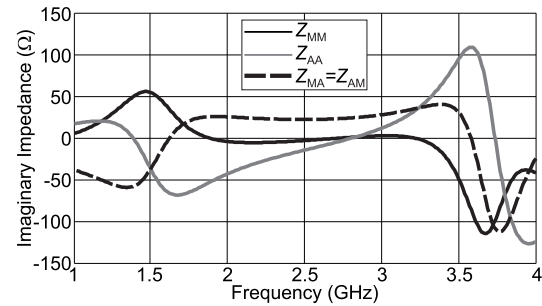


Fig. 5. Circuit schematic of the designed DPA output.



(a)



(b)

Fig. 6. \mathbf{Z} parameters versus frequency in the specific design case. (a) Real part. (b) Imaginary part.

and the estimated knee voltage is $V_K = 3 \text{ V}$. For this design, an optimum intrinsic load $R_{opt} = 30 \Omega$ is selected as target for the design, since it gives a good compromise between output power and efficiency. However, the device is able to deliver a maximum current $I_{MAX} = 2 \text{ A}$, which is the parameter used in the bandwidth estimation and design formula. The values of equivalent output reactive components, already successfully adopted in previous designs [6], are $C_{OUT} = 1.275 \text{ pF}$ and $L_{OUT} = 0.653 \text{ nH}$.

The values of f_0 , Z_1 , and Z_2 have been tuned to maximize the bandwidth with the goal to cover most of the LTE bands, i.e., from 1.6 to 3.5 GHz. The value of f_0 eventually results in 3 GHz, that leads to $Z_0 = 41.6 \Omega$ and $R_L = 28.9 \Omega$. The impedance of the series transmission line Z_1 tends to high values for maximum bandwidth, but it is limited in practice by the device drain pin width, and is set at $Z_1 = 54 \Omega$. The impedance of the open stub Z_2 results in 31Ω . The remaining parameters, which are obtained following the formulas in Section II-B, are reported in Fig. 5, where a full diagram of the designed DPA combiner is sketched.

After the total \mathbf{Z} matrix is derived from the global \mathbf{ABCD} matrix (see Fig. 6), the values of σ and $V_{sat,M} = V_{sat,A}$ can be calculated according to (4) and (6), respectively, and are reported versus frequency in Fig. 7.

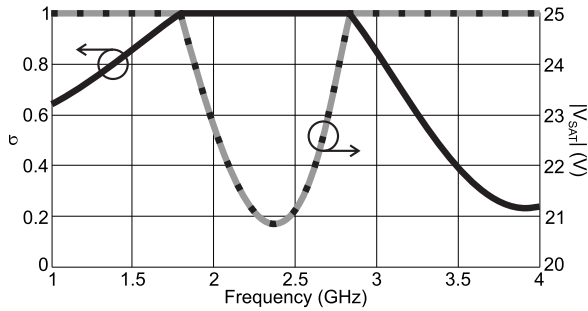


Fig. 7. σ (black solid curve), $V_{sat,M}$ (gray solid curve), and $V_{sat,A}$ (black dotted curve) versus frequency.

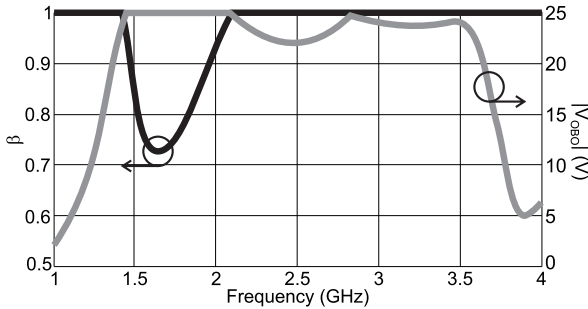


Fig. 8. β (black curve) and V_{OBO} (gray curve) versus frequency.

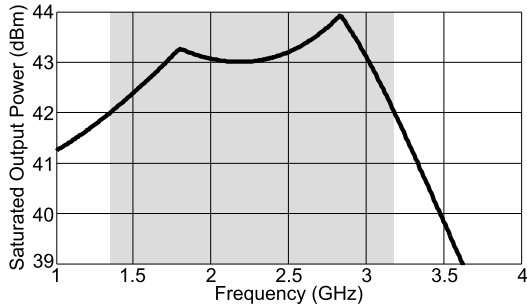


Fig. 9. $P_{OUT,sat}$ versus frequency. The range F_P is shaded.

As a successive step, β and $V_{OBO,M}$ are calculated according to (8) and (9), and are reported in Fig. 8.

The maximum output power defines F_P , and is reported in Fig. 9. Considering an output power target of 1 dB lower than the nominal power delivered by two devices, i.e., $P_{OUT,target} = 42$ dBm, then $F_P = [1.35 \text{ GHz}, 3.18 \text{ GHz}]$ that corresponds to a relative bandwidth of 81%. The range F_L is derived looking at Fig. 10, where the difference between OBO and IBO is reported. Assuming to be able to accept a maximum difference of 2 dB, then $F_L = [1.45 \text{ GHz}, 3.6 \text{ GHz}]$. The alternative bandwidth estimation is $F_P \cap F_L = [1.45 \text{ GHz}, 3.18 \text{ GHz}]$ that corresponds to a 75% relative bandwidth.

The efficiency can be only roughly estimated, especially in terms of absolute values, at each frequency point, as the ratio between RF output and dc absorbed power. A reduction of around 0.5 dB can be considered for output network losses, while at the back-off condition, another 0.5 dB can be added to account for the early turning ON of the auxiliary

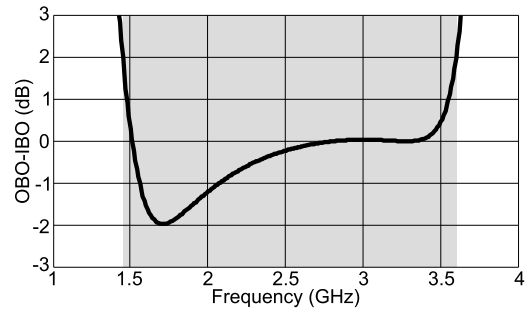


Fig. 10. OBO-IBO versus frequency. The range F_L is shaded.

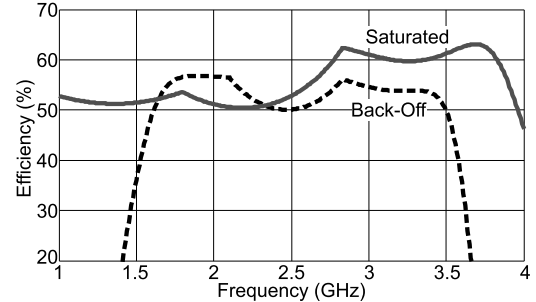


Fig. 11. Estimated efficiency versus frequency at saturation (gray solid line) and back-off (black dashed line).

device, necessary to ensure reasonably flat gain response. The estimated efficiency, at saturation and back-off, is reported in Fig. 11. It is important to note that this estimation is based on very strong assumptions, so nonlinear simulations are necessary to effectively predict the efficiency performance.

IV. MICROSTRIP DESIGN AND SIMULATIONS

The distributed elements composing the DPA output combiner have been substituted by microstrip elements, with a 760- μm Taconic substrate ($\epsilon_r = 3.5$). The overall schematic of the DPA is shown in Fig. 12. The output matching from the common impedance of 28.9–50 Ω is based on a two-section quarter-wave matching, modified to include the drain bias feed network.

The nonlinear model of the device, provided by the foundry, has been used in the design of the input matching and splitter, and in the tuning of the DPA before fabrication. In particular, the fine tuning permits to maintain the bandwidth performance in the passage from the much simplified model of the theory to the nonlinear model. Fig. 13 compares the load at the main device intrinsic plane, when the auxiliary is turned OFF, for different implementations of the output combiner. In particular, it can be noted that the translation from ideal lines to microstrip has negligible impact on the load. Moreover, the load trajectory of the theory-based circuit is only slightly modified by the fine tuning of the output combiner based on large signal simulations, meaning that it represented a good starting point for the design.

The input matching networks of the main and auxiliary stages are based on the same topology [24], but small differences in the components' values were adopted for an

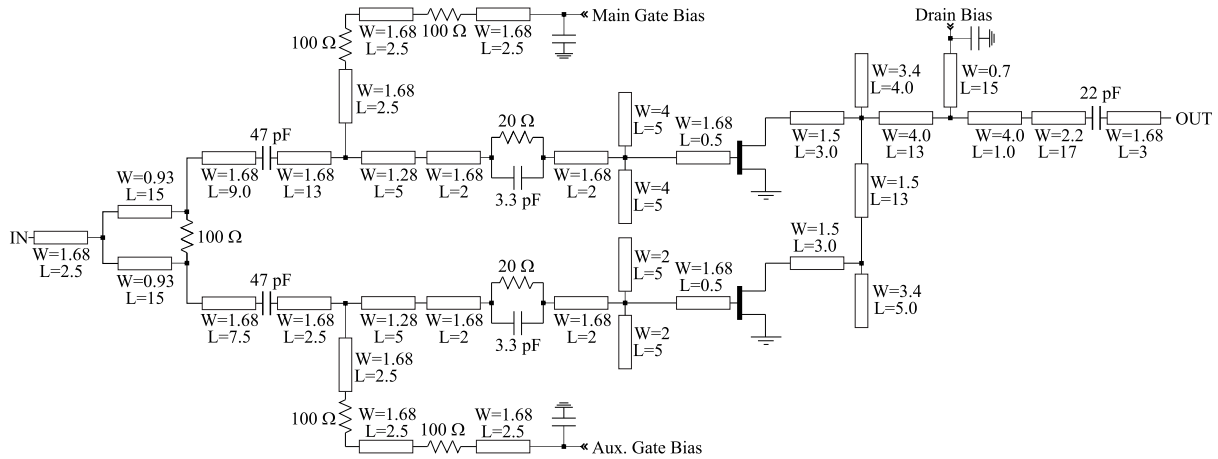


Fig. 12. Electrical scheme of the designed DPA. Lengths and widths are in millimeters.

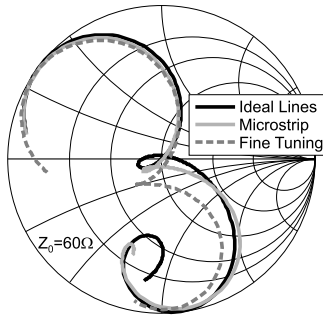


Fig. 13. Simulated load at the main device intrinsic plane, when the auxiliary device is turned OFF, in the 1–4.5-GHz band. Doherty output combiner with ideal lines (black solid curve), microstrip (light gray solid curve), and microstrip after fine tuning with nonlinear model (dark gray dashed curve).

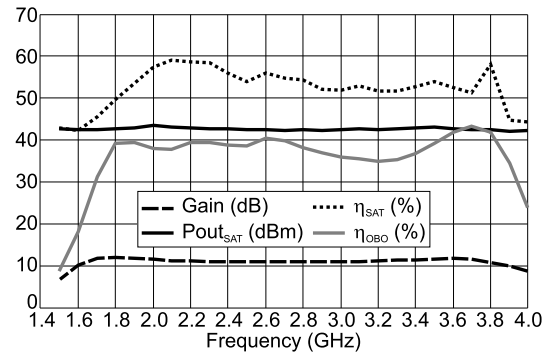


Fig. 14. CW simulated results versus frequency.

optimized operation. The choice of the input splitter is critical for its influence on bandwidth, efficiency, and linearity. Since the main goal of this design is bandwidth optimization, an even Wilkinson divider is preferred for its ability to maintain equal and controlled splitting on a broad band. To alleviate the gain compression issue that arises in AB/C Doherty PAs with the same devices and even splitting [25], the auxiliary gate bias is adjusted in nonlinear simulations and brought closer to class B than what expected from theory, thus trading off back-off efficiency for linearity and bandwidth. A 50-Ω delay line is inserted at the main device input to equalize the phase delay at the common node.

The DPA simulated performance versus CW frequency is resumed in Fig. 14, at a constant input power of 35 dBm. The maximum output power is higher than 42 dBm from 1.5 to 4 GHz, while the back-off efficiency is higher than 30% from 1.7 to 3.9 GHz.

V. CHARACTERIZATION RESULTS

The scattering parameters of the fabricated DPA (Fig. 15) have been measured on the range 1–4.5 GHz for an initial assessment of the device performance. The applied bias is $V_{DD} = 28$ V, with a main device quiescent current of $I_{DD} = 100$ mA, and auxiliary device gate at -5 V.

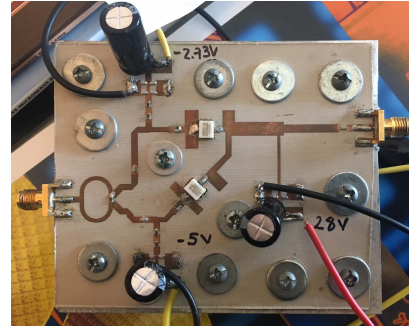


Fig. 15. Photograph of the fabricated DPA.

Fig. 16 shows the measured and simulated S_{21} , S_{11} of the DPA; the measured gain is higher than 10 dB from 1.45 to 3.8 GHz. The agreement between simulations and measurements is rather good, with a slight frequency shift to lower frequency of the measured S_{21} .

The DPA has been characterized with CW single-tone input in the 1.5–3.9 GHz range, with a 100 MHz step. Fig. 17 summarizes the measured CW performance at saturation and back-off versus CW frequency. On the 1.5–3.8-GHz band, the saturated output power exceeds 42.3 dBm, with the associated efficiency in the range 42%–63%. The saturated power is considered in the range of 2–4-dB gain compression, in order

TABLE I
COMPARISON WITH OTHER SINGLE-INPUT BROADBAND DPAS

Measurement	Unit	This	[4]	[9]	[10]	[11]	[12]	[13]
Frequency Range	GHz	1.5–3.8	1.7–2.7	1.05–2.55	1.6–2.4	1.7–2.6	2–2.7	1.65–2.75
Center Frequency	GHz	2.65	2.2	1.8	2	2.15	2.35	2.2
Bandwidth	GHz	2.3	1	1.5	0.8	0.9	0.7	1.1
Fractional Bandwidth	%	87	45	83	40	42	30	50
P_{sat} Max/Min	dBm	43.4/42.3	45.3/42.1	41/40	43.3/42.7	46.3/44.6	42/40.5	46.3/44.5
$DE_{\text{OBO},6\text{dB}}$ Max/Min	%	55/33	55/30	58/35	63/55	57/47	65/36	66/52
DE_{sat} Max/Min	%	63/42	n.a.	83/45	77/72	66/57	70/58	77/60
Gain Max/Min	dB	13.8/10	n.a.	12.5/10	13/11.5	14/11.8	14/8	11.7/9.3

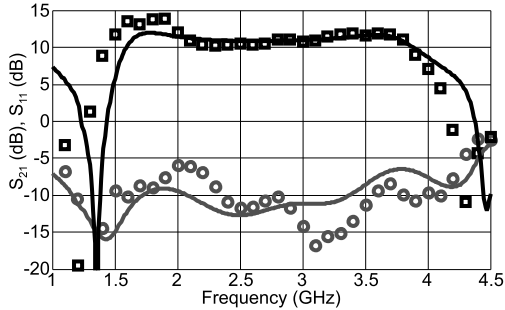


Fig. 16. Scattering versus frequency of the fabricated DPA. Symbols: measured. Solid lines: simulated. Black squares: S_{21} . Gray circles: S_{11} .

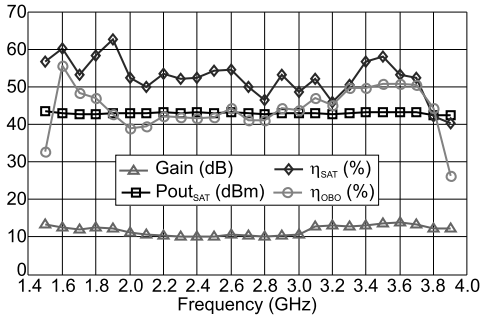


Fig. 17. CW measured results versus frequency.

to account for the 2-dB maximum compression defined for F_L , plus the compression due to the intrinsic nonlinear behavior of the active devices. At 6-dB back-off, the efficiency remains between 33% and 55%, while the small-signal gain is higher than 10 dB, with a ripple of 1.9 dB. The measured results are in good agreement with the simulation in Fig. 14, and the achieved bandwidth is well predicted by the proposed estimation method. Fig. 18 shows the CW power sweeps at 1.6, 2.1, 2.6, and 3.5 GHz.

The measured CW results are resumed in Table I and compared with other broadband DPAs presented in the literature. The proposed DPA has larger bandwidth, both in absolute and fractional terms, and similar output power and back-off efficiency compared with the other DPAs.

The DPA has been characterized with a modulated signal to assess its linearity and linearizability. The measurement setup is shown in Fig. 19. The RF modulated signal is generated by an arbitrary waveform generator (Keysight

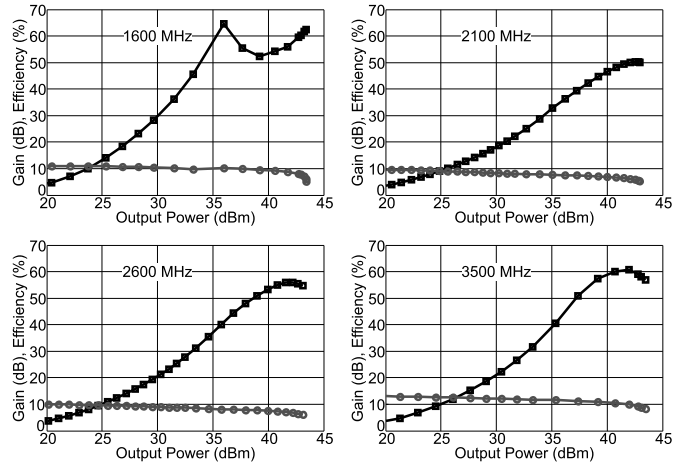


Fig. 18. CW measurements versus output power. Black squares: efficiency. Gray circles: gain.

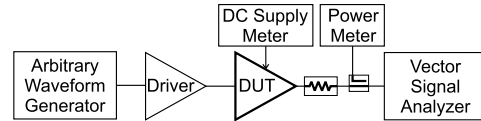


Fig. 19. Block diagram of the system-level characterization setup.

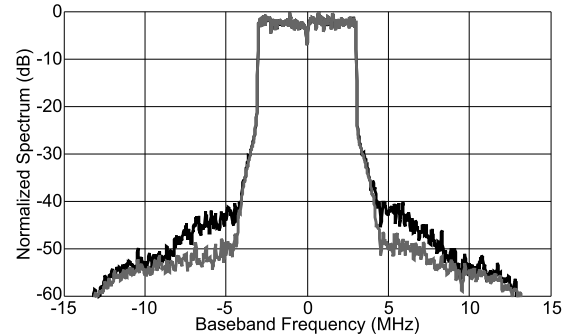


Fig. 20. Measured DPA output spectrum with 7-MHz channel WiMAX signal and 9 dB PAPR. Center frequency: 2.6 GHz. Average output power: 34 dBm. Average efficiency: 33%. Black curve: before digital predistortion. Gray curve: after digital predistortion.

ESG4433B), amplified by a driver amplifier, fed to the DPA, and then detected by a vector signal analyzer (Keysight MXA N9020A). A digital predistorter, based on a memory polynomial model [26], is implemented in MATLAB and is applied

to improve linearity and average efficiency. The predistorter has an odd polynomial order P and finite impulse response filter order M .

The measured spectra, before and after applying the predistorter, are shown in Fig. 20. At 2.6 GHz center frequency, a 7-MHz channel WiMAX signal with a PAPR of 9 dB has been applied, resulting in an ACPR of 42 and 48 dB, before and after predistortion ($P = 5$ and $M = 2$), respectively, at an average output power of 34 dBm and average efficiency of 33%.

VI. CONCLUSION

A state-of-the-art broadband DPA has been designed using a new approach, supported by a simplified analysis for the initial bandwidth estimation. The power amplifier has been fabricated using packaged GaN HEMT devices. On the band 1.5–3.9 GHz, corresponding to a fractional bandwidth of 87 %, the amplifier showed a maximum output power higher than 42.3 dBm, with a saturated efficiency between 42% and 63%, and 6 dB back-off efficiency between 33% and 55%, hence representing, to the best of our knowledge, the state of the art in broadband DPAs.

ACKNOWLEDGMENT

The authors would like to thank E. Angarita for the help in the fabrication of the hardware.

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Jorge Julian Moreno Rubio was born in Villavicencio, Colombia, in 1978. He received the B.Sc. degree in electronic engineering from the Universidad Pedagógica y Tecnológica de Colombia, Sogamoso, Colombia, in 2001, the M.Sc. degree in electronic engineering from Pontificia Universidad Javeriana, Bogotá, Colombia, in 2006, and the Ph.D. degree in electronic devices from the Politécnico di Torino, Turin, Italy, in 2012.

He is currently a Researcher with the Electronics Department, Universidad Pedagógica y Tecnológica de Colombia. His current research interests include the design and modeling of high-efficiency power amplifiers, and both hybrid and monolithic microwave integrated circuits.

Dr. Moreno Rubio was a recipient of the International Doctoral Studies Grant in 2008 given by the Departamento Administrativo de Ciencia, Tecnología e Innovación de Colombia—COLCIENCIAS, Bogotá.



Vittorio Camarchia (S'01–M'04–SM'14) was born in Turin, Italy, in 1972. He received the Laurea and Ph.D. degrees in electronic engineering from the Politecnico di Torino, Turin, in 2000 and 2003, respectively.

From 2001 to 2003, he was a Visiting Researcher with the Electrical and Computer Engineering Department, Boston University, Boston, MA, USA. In 2004, he joined the Department of Electronics and Telecommunications, Politecnico di Torino, first as a Post-Doctoral Researcher, then as an Assistant Professor, and as an Associate Professor in 2015. He has authored more than 140 international publications and some book chapters. In 2016, he edited *Electronics for Microwave Backhaul* (Artech House). His current research interests include the design and characterization of RF and microwave modules.

Prof. Camarchia is a member of the IEEE MTT Chapter-20 Subcommittee on Wireless Communications. In the last three years, he has organized several WS and Focused Sessions at EuMW and IMS on nonlinear measurements, microwave backhaul, 5G and millimeter (mm)-wave applications, and mm-wave power amplifier design. He was a recipient of the 2002 Young Graduated Research Fellowship of the Gallium Arsenide Application Symposium Association.



Marco Pirola (M'98) was born in Velezzo Lomellina, Italy, in 1963. He received the Laurea and Ph.D. degrees in electronic engineering from the Politecnico di Torino, Turin, Italy, in 1987 and 1992, respectively.

From 1992 to 1994, he was a Visiting Researcher with the Microwave Technology Division, Hewlett Packard, Santa Rosa, CA, USA. Since 1992, he has been with the Department of Electronics and Communications, Politecnico di Torino, first as a Researcher and then as an Associate Professor since 2000. His research interests include the simulation, modeling, design, and characterizations of microwave devices and systems.



Roberto Quaglia (M'13) was born in Casale Monferrato, Italy, in 1984. He received the Laurea degree (*cum laude*) in electronic engineering and Ph.D. degree in electronic devices from the Politecnico di Torino, Turin, Italy, in 2008 and 2012, respectively.

He is currently a Lecturer with the School of Engineering, Cardiff University, Wales, U.K. His current research interests include the design, modeling, and predistortion of high-efficiency MMIC power amplifiers.

Dr. Quaglia was a recipient of the European Union Marie Skłodowska Curie Fellow in 2015 and of the 2009 Young Graduated Research Fellowship presented by the Gallium Arsenide Application Symposium Association.