Racetrack logic

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This document introduces a building block for computing in memory systems. Based on the previously introduced Racetrack Memory proposed by IBM, we use a Racetrack Memory not only to store data but also to perform bitwise majority-based computations by coupling the Memory with inputs provided by controllable magnets. We define this solution Racetrack Logic. Micromagnetic simulations are used to confirm that the proposed solution is technically viable.

Introduction: It is well known that the current pervasive diffusion of computing systems has been enabled by the continuous reduction of the dimensions of computing devices, which also enabled lower power consumption and higher performances. This reduction is coming to an end. Several emerging technologies are being explored both for memory and logic implementations non based on conventional CMOS technology.

Among the emerging technologies IBM researchers proposed magnetic racetrack memory, a new class of potential non-volatile storage-class memories [1]. It is based on the controlled motion of a series of domain walls along magnetic nanowires using spin-polarized current pulses. The objective of this paper is to propose a novel device, based on racetrack memories, able also to perform logic functions and thus moving towards a 'computing in memory' paradigm. Differently from previous literature, for example [2], the storage elements are directly performing the logic functions. The rest of the paper is organized as follows: first a background section will introduce the racetrack memory functional paradigm, then we will show the proposed architecture for 'Racetrack Logic' and provide the simulation results. Finally we will summarize the architecture's features with an equivalent circuit and draw some conclusions.

Background: Racetrack memory was initially proposed in [1] as an high density non-volatile memory. A racetrack memory uses a ferromagnetic nanowire to embed information encoded as digital values. Every nanowire can memorize several bits. The first prototype of a racetrack memory integrated with a CMOS circuit was presented in [3], using a 90nm technological process. Racetrack memories can be fabricated using both in-plane magnetization materials [1] and out-of-plane magnetization materials [4]. The use of out-of-plane magnetization allows to build high density low power consumption memories [4]. The cost is an increment of the complexity in the fabrication process of the ferromagnetic materials employed. Recently racetrack memories were also used as building block for non-volatile CMOS hybrid logic circuits [5].

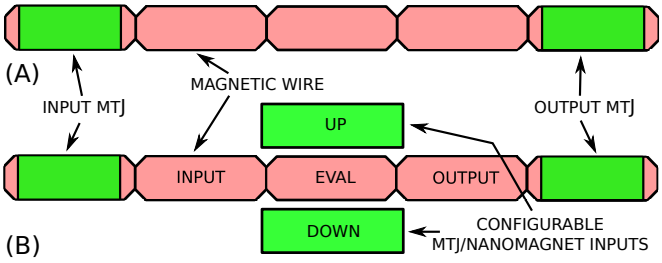

Fig. 1 *(A) Racetrack memory basic structure. A ferromagnetic wire is used to store the information. Notches are used to separates logic bits. Input and output interfaces are based on MTJs. (B) Racetrack logic basic structure. Two magnets are placed around the magnetic wire, their magnetic field is used to locally change the logic values stored inside the memory.*

Proposed architecture: The basic structure of a racetrack memory is depicted in Figure 1.A. A long ferromagnetic wire is used to store a large amount of logic values. Notches are created along the magnetic stripe to physically separate one bit from the other. Each section of the memory can be only in one of two stable states, used therefore to represent digital values. To write inside the memory two techniques can be employed. A magnetic field, locally applied to one section of the memory, can be used to write a new bit inside the memory. Another possibility is to build a Magneto-Tunnel Junction (MTJ) on top of the magnetic wire. When a current flows trough the MTJ the magnetization of the stripe is altered locally, writing a new bit inside the memory. Similarly MTJs can be used as output sensors, given that their resistance change accordingly to their magnetic state. If a current flows through the magnetic wire the information stored can be shifted forward or backward, depending on the direction of the current. A racetrack memory, with the structure depicted in Figure 1.A, can be therefore assimilated to a First-In-First-Out (FIFO) serial memory.

The physical structure of the Racetrack Logic element that we propose is instead highlighted in Figure 1.B. Two magnets are placed around the central section of the magnetic strip. These magnets can be either fixed value magnets or MTJs, for a full programmable logic. Aside from these additional magnets the structure remains the same as a normal racetrack memory.

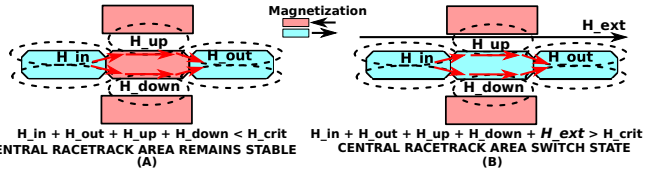

Fig. 2 *Racetrack Logic working principle. (A) The central element of the racetrack wire is influenced by the magnetic field generated by both the additional magnets and the neighbor parts of the magnetic stripe. The sum of these magnetic field is not enough to cause a switch in the magnetization of the strip. (B) If an external magnetic field is applied to the whole circuit, then the sum of all the magnetic fields is enough to generate a local switch of the magnetization.*

The working principle of the Racetrack Logic here proposed is explained in Figure 2. The basic idea is to exploit the same mechanism that can be used to write the memory. A local magnetic field is able to switch one bit of the memory to one stable state to the other. Instead of generating that magnetic field using for example a current flowing through a wire, we use additional magnets placed around one section of the magnetic strip. As depicted in Figure 2.A the section of the memory surrounded by the two magnets is subjected to four magnetic fields. These magnetic fields are the magnetic fields generated by the two additional magnets and the magnetic fields generated by the two neighbor sections of the memory. Normally the sum of these magnetic fields is not enough to cause a local switch of the magnetization. If an external magnetic field is added (Figure 2.B), the sum of this magnetic field and the magnetic fields generated by the magnets is enough to overcome the critical magnetic field, causing a local flip of the magnetization. The magnetization is therefore switched from one stable state to the other directly, without the need to force the magnetic line in an intermediate unstable state. Furthermore the switch depends on the state of neighbor elements, so it is a logic combination of their values. It is a true logic-in-memory operation. The magnetic field is a bidirectional global magnetic field applied to the whole chip. If it is not applied the circuit behaves exactly as a memory. When the magnetic field is applied, the values stored inside the memory can be altered according to a logic combination of all inputs. Further details on the logic behavior of the circuit will be given in the section describing the equivalent circuit.

Simulation Results: To validate this idea we performed a detailed characterization of the proposed structure using micromagnetic simulations. The simulator that we used is Mumax3 [6], a GPU-accelerated physical simulator. The use of Mumax3 allowed us to use a very fine mesh ($2x2x2nm^3$) and to include the effect of thermal noise, obtaining therefore a very accurate simulation of the structure. The magnetic memory strip is made by several sections. Each section has a length of 120nm and an height of 40nm. The two additional magnets are 120nm long and have an height of 40nm. They are separated by a distance of 10nm from the memory. The thickness of all the magnetic structures is 6nm. The material used is Permalloy, which has an in-plane magnetization. Most of the research on racetrack memories is focused on out-of-plane magnetization materials, because they offer better performance and more reliability. In this case we wanted to demonstrate the validity of our idea, not to optimize the structure for the best performance. We choose therefore to use Permalloy as material because it is a widely know material and easy to model. This choice therefore strengthen the validity of the results that we obtain.

Figure 3 depicts an example of physical simulation obtained. In the initial state (Figure 3.A) the magnetization of all magnetic elements,

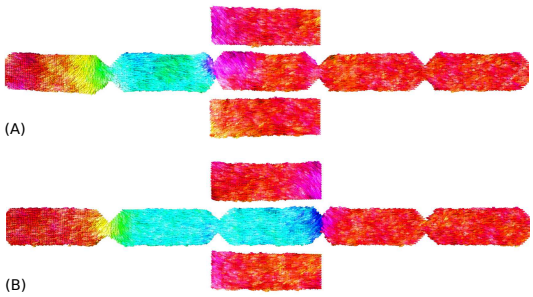

Fig. 3 *Physical simulation of a Racetrack Logic element. (A) Initial state, the magnetization of all elements is parallel to the longer magnets side, pointing leftward. Only the element of the racetrack memory on the left of the central area is forced in the opposite direction, with magnetization pointing rightward. (B) When a global magnetic field pointing rightward is applied to the structure the magnetization of the central element of the memory switches to the opposite state.*

except one, is aligned along the longer side of the magnets pointing leftward. The element of the magnetic memory on the left of the central area is instead forced in the opposite state, with magnetization pointing rightward. Then a global magnetic field of 16kA/m is applied to the structure. The magnetic field is also applied along the x axis, therefore parallel to the longer magnets side. The applied magnetic field points rightward, so it is parallel to the magnetic field generated by the two additional magnets and the magnetic field generated by the left element of the memory. As highlighted in Figure 3.B, the central element correctly switch from one state to its opposite. Of course to validate the structure one simulation is not sufficient. We tested the structure in all 64 possible combinations of state and we verified that effectively the structure behaves as intended. For example, if we invert the state of the two additional magnets there is no switch. We cannot present additional simulations in different conditions or report the complete table of truth of the logic element due to the limited space available. In the next section we report the logic function of the Racetrack Logic and a detailed description of its behavior. The switching time is smaller than 1ns. Considering that the value of applied magnetic field is also very small, we can conclude that the circuit has also excellent performance.

Equivalent Circuit: Figure 4 depicts the complete equivalent circuit of the Racetrack Logic. Considering the memory part alone, its equivalent circuit can be represented as a bidirectional shift register. Every part of the magnetic wire is modeled by a latch, where the clock is the current flowing through the wire itself. The direction of the applied current controls the input multiplexer, deciding therefore the direction of the shift. The behavior of the logic part of the circuit can be summarized

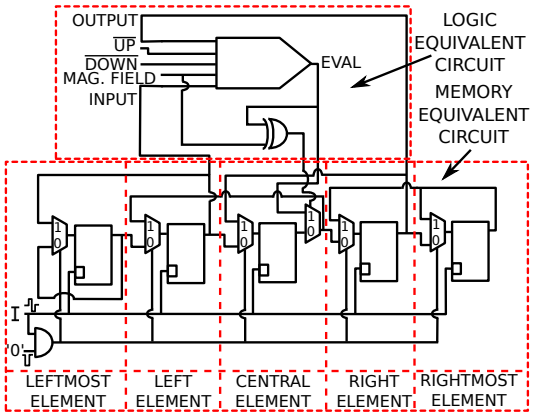

Fig. 4 *Racetrack Logic equivalent circuit. The memory part is equivalent to a shift register, where every register represents one element of the magnetic wire. The current is the clock of the registers, while its direction decides the shift verse. The logic part is equivalent to a 5 input majority voter, where the inputs are the inverted values of the two additional magnets, the value of neighbor memory elements and the external magnetic field. The value of the central memory element can change only if the applied magnetic field is in the opposite direction (exor gate).*

by the equation

$$EVAL = MV(MAG.FIELD, INPUT, OUTPUT, \overline{UP}, \overline{DOWN}).$$

It is a 5-inputs majority voter, where the output (EVAL) is the value of the central part of the memory wire. The inputs are the external magnetic field, the inverted values of the up (UP) and down (DOWN) magnets and the values of the neighbor areas of the memory wire, INPUT and OUTPUT (see Figure 1.B). In addition to this behavior, the value of EVAL can switch only if the applied magnetic field is in the opposite state to it. This peculiarity is modeled by the exor gate in Figure 4.

If we suppose to control independently all the inputs of the logic gate, by setting for example MTJs on both the additional magnets and the left and right part of the central memory element, we obtain exactly a combinational gate. It is a powerful logic gate with a relative small circuit area. Considering instead the circuit as it will be used, where the input and the output interface of the memory are generally placed on the extremities of the wire, then the behavior became more complex. The logic behaves still as a 5-inputs majority voter, but, by shifting the information using the current, the values of INPUT and OUTPUT depends on the previous state of the circuit. The behavior is no more combinational but sequential, and the whole circuits behaves like a very compact finite state machine. This peculiar behavior can open up interesting new ways of designing logic circuits.

Conclusion: We have proposed an innovative approach to use a racetrack memory not only as a memory, but also to perform in-memory logic computations. The Racetrack Logic concept is based on the simple addition of two magnets and a global magnetic field, performing a bitwise majority logic on the information stored in the memory. The obtained circuit is a 5-inputs majority voter, a powerful and compact logic gate. Furthermore, considering that a racetrack memory is equivalent to a shift register, the proposed circuits behaves like a compact finite state machine.

Now that we have demonstrated the feasibility of this idea, we are focusing on solving the critical issues identified by our first analysis. First we will improve the magnetic coupling with the additional magnets, by placing them on top and on bottom of the memory wire, reducing at the same time the distances. Second we will investigate how to improve the reliability and the performance of the circuit by using perpendicular magnetic anisotropy materials.

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