Results from CHIPIX-FE0, a Small Scale Prototype of a New Generation Pixel Readout ASIC in 65nm CMOS for HL-LHC
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on behalf of INFN/CHIPIX65 project

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Goals:

- development of an innovative CHIP for a PIXel detector at extreme rates and radiation HL-LHC conditions using a CMOS 65 nm technology for the first time in HEP community

- an efficient propagation across INFN of CMOS 65 nm technology (Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa and Torino groups)

- close synergy with the CERN RD53 international collaboration

Designed to be compliant with the expected requirements of HL-LHC pixel detectors:

- 40 MHz bunch crossing frequency
- 50 μm × 50 μm pixel size, large chips ~ 2 cm × 2 cm
- up to 200 event pile-up, 3 GHz/cm² hit rate, 75 kHz/pixel particle rate
- 1 MHz trigger rate, 12.5 μs trigger latency
- low power consumption < 0.55 W/cm², 10 μW/pixel
- hit efficiency > 99% at 3 GHz/cm²
The purpose of the **CHIPIX65 demonstrator** has been to satisfy these requirements as a first, intermediate step, towards the **RD53-A prototype** [see **E. Conti** presentation]

- **64×64** pixel matrix, embedding **two different Analog Front End (AFE) designs** working in parallel
  - **synchronous** architecture
  - **asynchronous** architecture

- **design and implementation of a novel 4×4 region-based** **Centralized Buffering Architecture (CBA)** for latency buffering and trigger matching

- **FIFO-based readout architecture** running at 40 MHz, **SPI-based chip configuration** at 13.33 MHz
  - support for **triggerless, triggered** and **scan-chain** operations
  - nominal 320 Mb/s serial-output

- **integration of available silicon-proven IP-blocks designed for RD53**
  - **bandgap voltage reference**
  - **SLVS transmitters/receivers** and **high-speed SER** [see **G. Magazzù** poster]
  - **10-bit biasing DAC**
  - **12-bit monitoring ADC**

- usage of the modified CERN rad-hard I/O library

- independent development from **FE65-P2 demonstrator** [see **T. Heim** presentation]
1. 32×64 pixels with synchronous FE architecture

2. 32×64 pixels with asynchronous FE architecture

3. replicated bias cells with current mirrors

4. 10-bit biasing DACs

5. bandgap voltage reference

6. 12-bit monitoring ADC

7. readout/configuration digital block and high-speed serializer at the chip periphery

8. SLVS transmitters/receivers and I/O cells

3.5 mm × 5.1 mm MPW
Synchronous front-end architecture

Torino INFN design group [JINST 11(2016), C03013]

- telescopic-cascode CSA with Krummenacher feedback for linear Time-over-Threshold (ToT) charge encoding
- synchronous hit discriminator with track-and-latch voltage comparator
- threshold trimming by means of autozeroing using capacitors
- 40 MHz 4-bit ToT or 5-bit fast ToT counting with latch turned into a local oscillator (100-900 MHz)
- efficient self-calibrations can be performed according to online machine operations
- successfully tested (also after irradiation) using dedicated mini@sic small-prototypes
Asynchronous front-end architecture

Bergamo/Pavia INFN design group [JINST 11(2016), C02049]

- folded-cascode CSA with Krummenacher feedback
- fast current comparator
- threshold trimming by means of 4-bit local DAC
- effective 80 MHz 5-bit dual-edge ToT counting at 40 MHz
- successfully tested (also after irradiation) using dedicated mini@sic small-prototypes
Test results
- chips received back from the foundry at the end of September, 2016
- tests performed in Bari, Bergamo and Torino INFN labs
- fully-digital ASIC/FPGA interface based on FMC
- prototype wire-bonded on a **custom test board**
- a few test points to monitor global bias voltages/currents
- custom **Ethernet/UDP firmware** supporting both Kintex-7 and Artix-7 Xilinx FPGA boards
- **NI/LabView** data acquisition interface supporting all chip operations
Irradiation tests

- several irradiation campaigns performed with X-rays at Padova INFN and CERN PH/ESE facilities
- electronics always biased at nominal operating conditions
- continuous monitoring of proper chip configuration and operations, charge scans performed at different steps
- non-uniform irradiation at room temperature up to 230 Mrad TID
- uniform and cold irradiation up to 600 Mrad TID
- uniform irradiation at room temperature up to 630 Mrad TID
- chips fully-functional up to 630 Mrad TID and one-week annealing
- all presented results confirm negligible degradation of analog front-ends performance after irradiation, digital readout and configuration OK

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Charge-injection calibration and monitoring results
— per-pixel generation of the analog test pulse starting from two well defined DC levels
— charge-injection triggered in selected pixels by a digital switching signal distributed to all pixels
— precise 8 fF per-pixel injection capacitance using MOM cap
— one global 10-bit calibration DAC common to both synchronous and asynchronous pixels
— good agreement between measured linearity and CAD simulated data
- calibration voltage fed to monitoring ADC, converted data \textbf{read back through SPI}
- embedded \textbf{self-calibration algorithm} to minimize gain and offset errors
- \textbf{digital trimming} using dedicated configuration registers is also supported
- \textbf{linear ADC characteristic}, good agreement between measurements and CAD simulated data
- DNL/INL performance metrics extracted with automated code-density tests
- measured \(-0.1\) LSB < DNL < 0.1 LSB as from CAD simulations (self-calibration operating mode)
- \(-5\) LSB < INL < 4 LSB, slight larger than simulated values (self-calibration operating mode)
- additional measurements with digital trimming ongoing in Bari
Synchronous FE results
all pixels tested and fully working

autozeroing performed each 200 $\mu$s

effective noise and threshold values determined by means of S-curves

measurements performed with charge scans and fixed threshold

hit efficiency recorded for 100 charge-injection pulses

measured points fitted using an error function (sigmoid)

noise and threshold values extracted from means and variances distributions
Threshold measurements with autozeroing

- effective threshold measured for different values of fixed global threshold
- autozeroing works, residual offset value of about 100 e\(^{-}\) RMS in good agreement with CAD simulations (\(\approx 70 \text{ e}\(^{-}\) RMS latch dynamic offset)
- linear increase as expected
- threshold-to-charge characteristic from fit
- \(\approx 250 \text{ e}\(^{-}\) minimum threshold
Noise measurements

ENC measured for different values of fixed global threshold

- constant behavior with threshold values as expected
- ENC $\approx 90$ e$^-$ in good agreement with CAD simulations
- low-noise performance assured despite continuous latch and region-logic digital switching activity
Fast Time-over-Threshold (ToT) counting

- very good linearity for the 5-bit fast ToT
- 320 MHz frequency reached for a 5 ke⁻
- slope dispersion of about 10% due to mismatches in the analog part, as from CAD simulations
Test-pulse phase scan

- average threshold value measured as a function of the relative delay between the charge-injection pulse and the clock strobing the latch (nominal BX clock from FPGA reduced from 40 MHz to 20 MHz)

- simplified analytical model assumed for CSA output waveform:

  \[
  V_{out}(t) = \frac{Q_{in}}{C_F} \left[ 1 - e^{-(t-t_0)/\tau} \right] - \frac{I_F}{C_F} (t - t_0) = p_0 \left[ 1 - e^{-(t-p_1)/p_2} \right] - \frac{p_3}{C_F} (t - p_1)
  \]

- preamplifier analog output partially reconstructed from fit, good agreement between fit parameters and electrical settings

\[\begin{align*}
p_0 &= 0.13 \pm 0.0011 \\
p_1 &= -7.3 \pm 0.045 \\
p_2 &= 5.1 \pm 0.053 \\
p_3 &= 9.9 \pm 0.14 \\
p_0 &= 0.0011 \pm 0.13 \\
p_1 &= 0.045 \pm 7.3 \\
p_2 &= 0.14 \pm 9.9 \\
p_3 &= 0.053 \pm 5.1
\end{align*}\]
Post-irradiation results

- 3 $\mu$s calibration cycles required for efficient autozeroing after 230 Mrad, still compliant with online LHC machine operations
- threshold linearity verified, no significant threshold variations observed after irradiation
Post-irradiation results

- **ENC constant behavior** still present after 230 Mrad TID (room temperature irradiation)
- no significant degradation of **low-noise performance** observed, $\text{ENC} \approx 100 \text{ e}^-$
− ≈ 15% degradation of **latch oscillation-frequency** (recoverable through current starving in the delay-line)

− negligible degradation of **threshold performance** after 600 Mrad TID (cold irradiation)
Asynchronous FE results
Untrimmed threshold dispersion and noise

- Test setup delivered to Bergamo/Pavia INFN group, requiring some firmware modifications to target Xilinx Artix-7 evaluation board
- All pixels tested and fully working
- \( \approx 400 \, e^- \) RMS untrimmed threshold dispersion and ENC \( \approx 85 \, e^- \) noise before irradiation
- Good agreement with CAD simulations
Threshold linearity

- effective threshold measured for different values of **fixed global threshold**
- linear increase as expected
- threshold-to-charge characteristic from fit
- \( \approx 500 \text{ e}^- \) **minimum threshold**
— **per-pixel DAC codes** extracted from untrimmed S-curves using a set of ROOT macros and then loaded into the chip
— electrical functionality OK, **threshold compensation** works for all pixels
— ≈ 45 e⁻ RMS **residual threshold dispersion** before irradiation, in good agreement with CAD simulations
— ≈ 150 e⁻ after **1-week annealing** (630 Mrad TID) and ≈ 125 e⁻ after **4-weeks annealing**, global threshold-current DAC dynamic range kept as before irradiation
— reduced to ≈ 85 e⁻ by **re-optimizing global DACs settings**
Preliminary results with 3D sensors
— bump-bonding performed at SLAC with **FBK 3D pixel sensors** (2016 wafers)
— sample prototypes coupled to both $50 \, \mu m \times 50 \, \mu m$ and $25 \, \mu m \times 100 \, \mu m$-1E
— chips received back from SLAC three weeks ago, **preliminary tests** just started in Torino
— first $50$- and $25$- $\mu m$ 3D sensors coupled to a complete readout chip in 65 nm CMOS, **never before**!
Noise measurements

- **bump-bonding** and proper sensor electrical connectivity with the chip verified
- **average noise** value extracted from all-pixels S-curves as a function of the sensor reverse bias
- lower noise measured for 25 $\mu$m $\times$ 100 $\mu$m-1E sensors as expected (slight lower capacitance in -1E geometry)
- very promising and comparable results for both front-end architectures!
First tests with laser and sources

- additional preliminary tests performed using **laser** (1060 nm) and **sources** ($^{137}$Cs, $^{241}$Am and $^{90}$Sr)
- **proper readout/masking** of all exposed pixels verified
- major efforts now in developing missing offline-software components for data analysis
Conclusions

- **CHIPIX65 demonstrator** submitted in July 2016, chips received back from the foundry at the end of September
  - 64×64 pixel matrix, 50 µm × 50 µm pixel size
  - first 50- and 25-µm **3D sensors** bump-bonded to a complete readout chip in 65 nm CMOS!

- **full-system integration** with digital-on-top design methodology
  - two different **analog front-end designs** working in parallel
  - novel **region-based centralized buffering architecture**
  - **silicon proven IP-blocks** developed for RD53 (DAC, ADC, BGR, SER, SLVS TX/RX)

- **highly encouraging results** from all pre- and post-irradiation tests
  - fully working electronics **during/after irradiation**, good agreement with all CAD simulations
  - **low-noise** and **low-threshold** performance achieved for both designs despite digital activity
  - **fully-working chip** after 630 Mrad TID with negligible degradation of analog key parameters

- **selected CHIPIX demonstrator components** have been **included into RD53-A prototype**
  - global-bias components (DAC, BGR)
  - improved versions of synchronous and asynchronous front-ends
  - improved version of region digital architecture coupled to synchronous front-end

- **prototype just re-submitted** as part of the shared **RD53/MPA/SSA engineering run** with **further improvements** in analog front-ends

- **next steps**
  - completion of DAQ software, **extensive measurements with 3D sensors, test beam**
  - bump-bonding with **planar sensors** (Hamamatsu)
  - characterization of CHIPIX65 components **now embedded into the RD53-A prototype**
Thank you for your attention

N. Demaria et al., *CHIPIX65: Developments on a new generation pixel readout ASIC in CMOS 65 nm for HEP experiments*. Proceeding of the 2015 IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)


L. Pacher et al., *A Low-Power Low-Noise Synchronous Pixel Front-End Chain in 65 nm CMOS Technology with Local Fast ToT Encoding and Autozeroing for Extreme Rate and Radiation at HL-LHC*. Proceeding of the 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (IEEE NSS/MIC)


L. Ratti et al., *An asynchronous front-end channel for pixel detectors at the HL-LHC experiment upgrades*. Proceeding of the 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (IEEE NSS/MIC)


E. Monteil et al., *A synchronous analog very front-end in 65 nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC*. Proceeding of the 2016 Topical Workshop on Electronics for Particle Physics (TWEPP).Submitted to Journal of Instrumentation (JINST)
