

A custom readout electronics for the BESIII CGEM detector

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## A custom readout electronics for the BESIII CGEM detector

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**ABSTRACT:** For the upgrade of the inner tracker of the BESIII spectrometer, planned for 2018, a lightweight tracker based on an innovative Cylindrical Gas Electron Multiplier (CGEM) detector is now under development. The analogue readout of the CGEM enables the use of a charge centroid algorithm to improve the spatial resolution to better than  $130\ \mu\text{m}$  while loosening the pitch strip to  $650\ \mu\text{m}$ , which allows to reduce the total number of channels to about 10 000. The channels are readout by 160 dedicated integrated 64-channel front-end ASICs, providing a time and charge measurement and featuring a fully-digital output.

The energy measurement is extracted either from the time-over-threshold (ToT) or the 10-bit digitisation of the peak amplitude of the signal. The time of the event is generated by quad-buffered low-power TDCs, allowing for rates in excess of 60 kHz per channel. The TDCs are based on analogue interpolation techniques and produce a time stamp (or two, if working in ToT mode) of the event with a time resolution better than 50 ps. The front-end noise, based on a CSA and a two-stage complex conjugated pole shapers, dominate the channel intrinsic time jitter, which is less than 5 ns r.m.s.. The time information of the hit can be used to reconstruct the track path, operating the detector as a small TPC and hence improving the position resolution when the distribution of the cloud, due to large incident angle or magnetic field, is very broad.

Event data is collected by an off-detector motherboard, where each GEM-ROC readout card handles 4 ASIC carrier FEBs (512 channels). Configuration upload and data readout between the off-detector electronics and the VME-based data collector cards are managed by bi-directional fibre optical links.

This paper covers the design of a custom front-end electronics for the readout of the new inner tracker of the BESIII experiment, addressing the relevant design aspects of the detector electronics and the front-end ASIC for the CGEM readout, and reviewing the first silicon results of the chip prototype.

**KEYWORDS:** Micropattern gaseous detectors, Front-end electronics for detector readout, CMOS readout of gaseous detectors, VLSI circuits, Analogue and Digital electronic circuits

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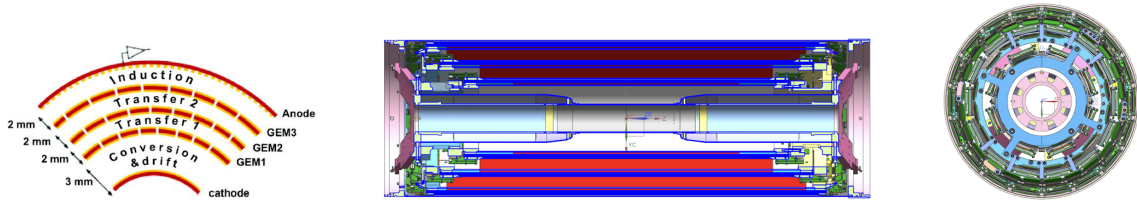
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## 1 Introduction

The Beijing Spectrometer III (BESIII) operates at the  $\tau$ -charm energy region and runs since 2009 at the  $e^+ e^-$  collider (BEPCII), hosted by the Institute of High Energy Physics (IHEP) in Beijing [1]. The high luminosity of this multi-bunch collider, which has reached  $1.0 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$  in 2016, increased the radiation dose on the inner Main Drift Chamber (MDC) tracker. An upgrade program has been set up to counter this ageing effect and allow the operation of the BESIII experiment beyond 2022. This upgrade proposal includes the development of a lightweight Cylindrical Gas Electron Multiplier Inner Tracker (CGEM-IT), and its installation is planned for mid 2018.

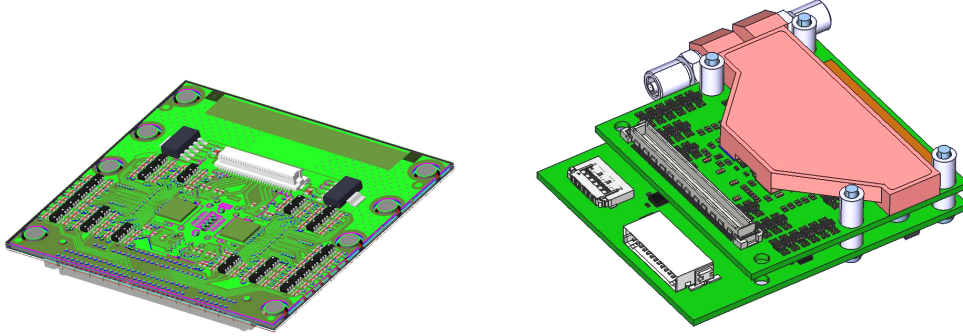


**Figure 1.** Schematic of a Triple-GEM (*left*) and 2D section views (*centre, right*) of the CGEM detector mechanical drawings.

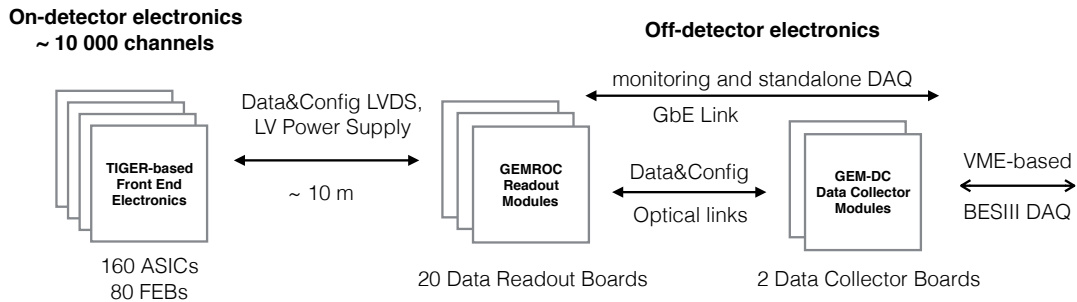
A Triple-CGEM (Figure 1) builds up three concentric independent tracking layers, each of one assembling a cathode, three GEM foils and the readout anode. This design allows for higher gain with lower discharge rates in respect to the single GEM, and covers 93% of the solid angle. The readout anode of each CGEM is segmented with XV patterned strips with a  $650 \mu\text{m}$  pitch. Complementary charge centroid and  $\mu$ -TPC algorithms are then used to provide an  $x - y$  position resolution of  $130 \mu\text{m}$  [2] on the track reconstruction. The analogue readout of the detector, which allows reducing the total number of channels to around 10 000, requires dedicated front-end electronics. This work describes and discusses the design, characterisation and production plans for the on-detector integrated and front-end circuitry, off-detector data collection and power electronics.

## 2 Overview of the CGEM Readout Electronics

The analogue readout of the Triple-GEMs employs a dedicated multi-channel front-end Application-Specific Integrated Circuit (ASIC), developed specifically to target the design requirements of the BESIII-CGEM detector. Two 64-channel chips are mounted on each one of the 80 Front-End Boards (FEBs). The FEB (Figure 2) consists on a stack of an analogue-most layer (FE1), hosting 2 ASICs, regulators and ESD protection networks, interface towards the anode and the digital-domain FE2, which handles the on-detector electronics signal, data and power interface.



**Figure 2.** Front-End Board Design for Layer 1: top-side routing on FE1 (*left*) and FE1/FE2 assembly with liquid cooling heat exchanger plate (*right*).



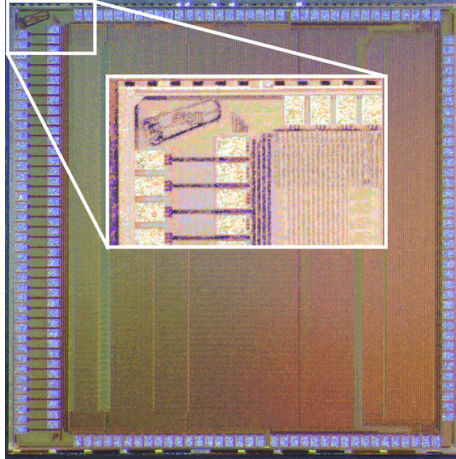
**Figure 3.** Conceptual block diagram overview of the CGEM Detector Electronics

Off-detector GEM Readout Cards (GEMROC) modules handle quad-FEBs through 10-metre LVDS links for data, configuration and monitoring. The GEMROC uses an ALTERA ArriaVGX FPGA development board coupled, through a High-Speed Mezzanine Card (HSMC) high performance connector, to the Interface Card (GEMROC\_IFC), which manages the electrical and physical interfaces to the FEBs, to the GEM-DC data concentrator (bi-directional fibre optic links) and the BES-III Fast Control system. An ethernet port is also available for monitoring and debugging. Each GEM-DC data collector is based on the Advanced Trigger Logic Board (ATLB) [3] and handles up to 16 optical links running at 2 Gbit/s (max 6.5 Gb/s). It features a VME base board for the interface with the BESIII Data Acquisition (DAQ) system. Both the GEMROCs and the on-detector electronics are powered by a dedicated Low-Voltage (LV) distribution system, allowing for single

board current/voltage monitoring, fuses and on/off capability, and remote controlled via ethernet. Figure 3 illustrates the block diagram of the detector electronics.

### 3 The TIGER ASIC

The Torino Integrated GEM Electronics for Readout (TIGER) chip is a 64-channel mixed-mode circuit for the readout of GEM detectors. The  $5 \times 5 \text{ mm}^2$  ASIC is designed on an UMC CMOS 110nm technology node (Figure 4).

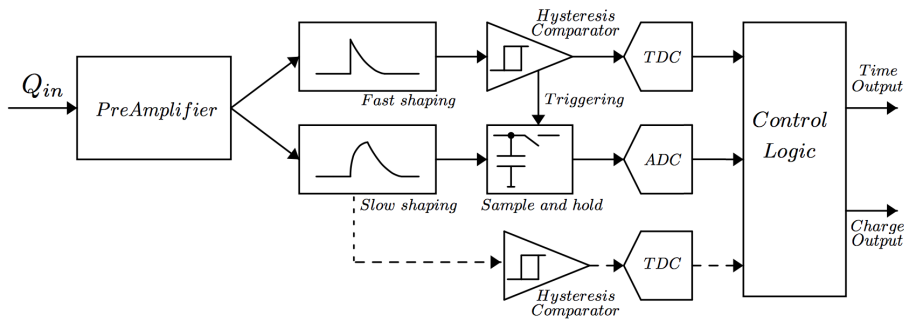


**Figure 4.** Microphotograph of the TIGER chip.

#### 3.1 Design of a mixed-mode 64-channel ASIC for Micropattern gaseous detectors

The ASIC features a linear array of 64 channels, which provide amplification, shaping and signal conditioning, time and charge measurement, at a maximum data rate of 100 kHz. The time stamp and digitisation data are collected by a back-end controller, upgraded from IP used in a family of chips designed for medical imaging [4, 5]. This upgrade adds single-event-upset protection (SEU) for finite-state machines (with TMR) and configuration payload (Hamming encoding). The 8B/10B encoded fully digital data output uses up to 4 LVDS Tx drivers operating in single or double-data-rate at maximum rate of 640 Mb/s per link. An SPI protocol is used for the configuration upload/download, where a set of periphery DACs is used for the biasing of the channel analogue circuitry. On-chip calibration circuits generate programmable test charge pulses to each channel, used for calibration (before and after installation) and debug purposes.

Figure 5 illustrates the block diagram organisation of the TIGER channel. A time-based readout operation mode, using single or double threshold, produces a time stamp on the rising and falling edges of the signals produced by the fast and slow shaping, respectively. The timing measurement is obtained with a sub-50 ps binning (with a system clock of 160 MHz) quad-buffered time-to-digital converters (TDCs) based on time interpolators [4]. When working in a time-based readout, the charge information can be retrieved from the Time-over-Threshold (ToT). The inherent non-linear measurement requires a ToT vs.  $Q_{in}$  calibration, which compression curve is typical when the time-over-threshold is measured with CR-RC<sup>2</sup> shapers.



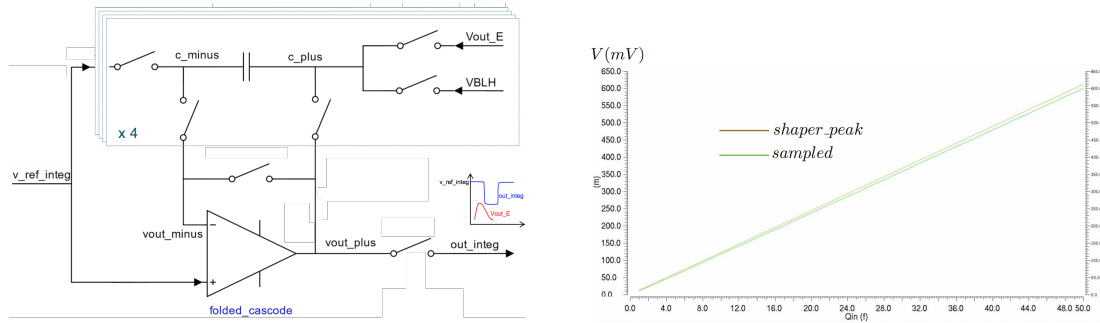
**Figure 5.** Block diagram of the TIGER channel.

In standard operation with GEMs, a Sample-and-Hold circuit will be used instead for the energy measurement (Figure 6). The circuit consists on a programmable digitally-controlled peak detector, where the start of the sampling is set by the trigger on the fast discriminator output, and the sampling time can be set in steps of 25 ns. The digitisation of the voltage amplitude is performed with a 10-bit Wilkinson ADC, otherwise used for the fine time measurement of the slow shaper falling edge trigger. While this simpler strategy, in respect to a two-phase analogue peak detector, avoids the use of rail-to-rail input operational amplifiers, it is inherently more susceptible to the jitter and time-walk on the leading-edge discriminators. With the nominal expected jitter from simulations, we expect an error on the sampled voltage smaller than 1%, which is adequate for the purposes of the CGEM detector.

The very-front-end is optimised to the readout of signals in the range 1 - 50 fC, and targets a noise below 2000 electrons r.m.s. for a channel detector capacitance of 100 pF. A low-noise two-stage cascode charge sensitive front-end generates two replicas of the amplified signal, which is split for time and charge measurement branches in two dedicated shapers. The two shapers produce a semi-Gaussian output signal shape with a peaking time 60 and 170 ns, respectively for the time and charge branches. The maximum signal width expected is around 1  $\mu$ s on the energy shaper, thereby limiting the pile-up probability to less than 1% at 60 kHz. A baseline-holder circuit locks the DC voltage at the output of the amplifier to a voltage that can be set externally between 250 and 650 mV, typically set to 300 mV.

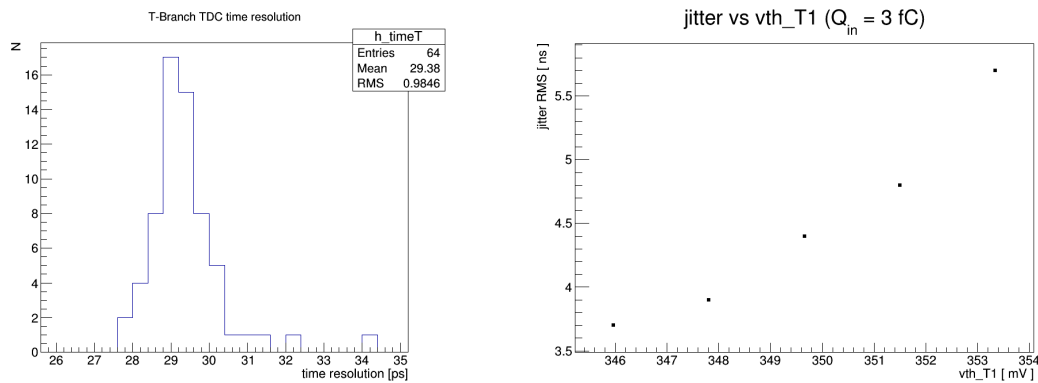
### 3.2 Electrical Characterisation Results

The first TIGER prototype was produced with a Multi-Project-Wafer (MPW) shuttle and the electrical characterisation campaign started in October 2016. Read/Write operations of channel/global configuration registers, data transmission and decoding, (dual-) TDC operation and fine calibration and the sample-and-hold circuit work as expected. Figure 7 shows the time resolution of the TDC on 64 channels after calibration. Such calibration, performed with a sweep of the test-pulse along one clock cycle, generates a look-up table (LUT) that stores the values of the interpolation factor and offset for each TDC/interpolator. The average 30 ps r.m.s. quantisation error is much lower than the required jitter on the measurement of the event, and the intrinsic time resolution of the channel is only affected by the noise of the front-end. For an input capacitance of 100 pF and a



**Figure 6.** Sample-and-Hold circuit for amplitude measurement; circuit implementation (*left*) and expected linear behaviour on the measurement of the signal peak and sampled amplitude as a function of the input charge (*right*).

signal level or 3 fC, the jitter on the time measurement is typically below 5 ns r.m.s. (refer to figure 7, right plot).



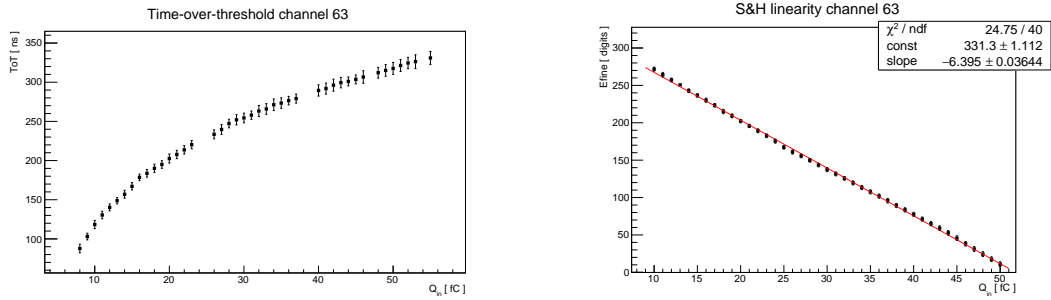
**Figure 7.** Time resolution of the TDC on the 64 channels (*left*); and jitter on the time measurement for  $C_d = 100$  pF and  $Q_{in} = 3$  fC as a function of the threshold (*right*).

The noise of the front-end is estimated after a threshold scan with a fixed input charge generated by the on-chip calibration circuit. A sigmoid fit to the resulting s-curve provides a r.m.s. value for the intrinsic noise, and this procedure is repeated for different input capacitance values or configuration and operation mode settings. The same method is used for the baseline scan, which results are saved into a per-channel threshold LUT that allows for the equalisation of the effective threshold.

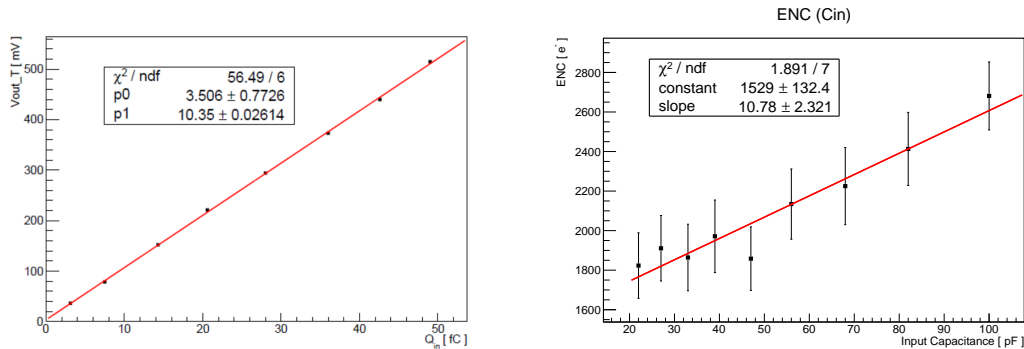
Figure 8 shows the charge measurement results on a single test channel, using ToT and the S&H circuit, and injecting a known input charge with an external programmable-amplitude pulse generator. The results match the expected linearity (better than 0.2%) of the sample and hold circuit up to an input charge of 50 fC. The characterisation with an external test pulse generator is used for the calibration of the internal calibration signal, which is afterwards used for systematic testing.

A set of probing points in one channel allows for a direct measurement of the pulse amplitude at the output of the fast shaper, as well as the LSB and offset of the discriminator threshold. This feature thereby allows for a direct measurement of the amplifier gain in one of the channels. The

average gain of 10 mV/fC is in good agreement with post-layout simulation results (refer to figure 9, left plot), and the residual channel-to-channel dispersion is below 0.2 mV/fC r.m.s. On the other hand, the equivalent noise charge (ENC) of 2600 electrons r.m.s. on the slow shaper output with an input capacitance of 100 pF is almost 30% higher than expected. However, the plateau of the noise characteristic at low input capacitance (refer to figure 9, right plot) seems to indicate that the measurement is affected by common-mode noise. Front-end board and test setup grounding and shielding, as well as power-supply rejection ratio (PSRR) of the front-end blocks are under study in order to understand the root cause of this increase.



**Figure 8.** Charge measurement with time-over-threshold (*left*); and sample-and-hold circuit (*right*).



**Figure 9.** Gain measurement on a debug output (*left*); and ENC of the slow shaper (*right*) as a function of the input capacitance.

## 4 Outlook and Conclusions

The analogue readout of the CGEM detector for the BESIII inner tracker upgrade calls for an innovative custom detector electronics. A dedicated 64-channel ASIC was designed to target the detector specifications. Electrical characterisation of the first prototype was performed between October 2016 and May 2017, and detector test campaigns with radioactive sources and cosmic rays are ongoing since March 2017. The volume production of the engineering version with minor revisions is planned for July 2017. The assembly and qualification of the TIGER with the on-detector Front-End Boards is expected to start by Fall 2017. System-level commissioning and

instrumentation of the full CGEM detector will be started in February 2018, and the installation of the tracker is forecast for Summer 2018.

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