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Advanced High Efficiency and Broadband Power Amplifiers Based on GaN HEMT for Wireless Applications

By

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

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2016

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

I would like to dedicate this thesis to my loving parents

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Abstract

In advanced wireless communication systems, a rapid increase in the mobile data traffic and broad information bandwidth requirement can lead to the use of complex spectrally efficient modulation schemes such as orthogonal frequency-division multiplexing (OFDM). Generally, complex non-constant envelope modulated signals have very high peak-to-average ratios (PAPR). Doherty Power Amplifier (DPA) is the most commonly used power amplifier (PA) architecture for meeting high efficiency requirement in advanced communication systems, in the presence of high PAPR signals. However, limited bandwidth of the conventional DPA is often identified as a bottleneck for widespread deployment in base-station application for multi-standard communication signals. The research in this thesis focuses on the development of new designs to overcome the bandwidth limitations of a conventional PA. In particular, the bandwidth limitation factors of a conventional DPA architecture are studied. Moreover, a novel design technique is proposed for DPA's bandwidth extension.

In the first PA design, limited bandwidth and linearity problems are addressed simultaneously. For this purpose, a new Class-AB PA with extended bandwidth and improved linearity is presented for LTE 5 W pico-cell base-station over a frequency range of 1.9–2.5 GHz. A two-tone load/source-pull and bias point optimization techniques are used to extract the sweet spots for optimum efficiency and linearity from the 6 W Cree GaN HEMT device for the whole frequency band. The realized prototype presented saturated PAE higher than 60%, a power gain of 13 dB and an average output power of 36.5 dBm over the desired bandwidth. The proposed PA is also characterized by QAM-256 and LTE input communication signals for linearity characterization. Measured ACPRs are lower than -40 dBc for an input power of 17 dBm. The documented results indicate that the proposed Class-AB architecture is suitable for pico-cell base-station application.

In the second PA design, an inherent bandwidth limitation of Class-F power amplifier forced by the improper load harmonics terminations at multiple harmonics is investigated and analyzed. It is demonstrated that the impedance

tuning of the second and third harmonics at the drain terminal of a transistor is crucial to achieve a broadband performance. The effect of harmonics terminations on power amplifier's bandwidth up to fourth harmonics is investigated. The implemented broadband Class-F PA achieved maximum saturated drain efficiency 60-77%, and 10 W output power throughout (1.1-2.1 GHz) band. The simulated and measured results verify that the presented Class-F PA is suitable for a high-efficiency system application in wireless communications over a wide range of frequencies.

In the third PA design, a single- and dual-input DPA for LTE application in the 3.5 GHz frequency band are presented and compared. The main goal of this study is to improve the performance of gallium–nitride (GaN) Doherty transmitters over a wide bandwidth in the 3.5 GHz frequency band. For this purpose, the linearity-efficiency trade-off for the two proposed architectures is discussed in detail. Simulated results demonstrate that the single- and dual-input DPA exhibited a peak drain efficiency (DE) of 72.4% and 77%, respectively. Both the circuits showed saturated output power more than 42.9 dBm throughout the designed band. Saturated efficiency, gain and bandwidth of dual-input DPA is higher than that of the single-input DPA. On the other side, dual-input DPA linearity is worse as compared to the single-input DPA.

In the last PA design, a novel design methodology for ultra-wide band DPA is presented. The bandwidth limitation factors of the conventional Doherty amplifier are discussed on the ground of broadband matching with impedance variation. To extend the DPA bandwidth, three different methods are used such as post-matching, low impedance transformation ratio and the optimization of offset line for wide bandwidth in the proposed design. The proposed Doherty power amplifier was designed and realized based on two 10 W GaN HEMT devices from Cree Inc. The measured results exhibited 42-57% of efficiency at the 6-dB back-off and saturated output power ranges from 41.5 to 43.1 dBm in the frequency range of 1.15 to 2.35 GHz (68.5% fractional bandwidth). Moreover, less than -25 dBc ACPRs are measured at 42 dBm peak output power throughout the designed band.

In a nutshell, all power amplifiers presented in this thesis are suitable for wideband operation and their performances are satisfying the required operational standard. Therefore, this thesis has a significant contribution in the domain of high efficiency and broadband power amplifiers.

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Chapter 1

Introduction

1.1 Motivation

Communication among the people has been dramatically changed by the mobile communication systems in the last two decades. Mobile communication systems have achieved an outstanding popularity in history of wireless communication. Figure 1.1 presents the evolution of wireless access technologies from the first mobile generation (1G) to the upcoming fifth generation (5G) with their capabilities and capacities. In advanced mobile communication systems, currently, 4G Long Term Evolution (LTE) networks are very well developed in terms of both mobile handset and the network infrastructure. Now, the eyes of the mobile telecommunications industry are turning towards the next generation of technology i.e. 5G [1-3]. Although, the first deployment is a few years away, however much work needs to be done to lay the ground for 5G. In order to satisfy the growing demand of capacity and capability of wireless communications, the new generation of mobile communications will clearly add more spectrum to the capacity. However, some of the capabilities are very important, for example high-speed video, low latency, ultra-reliability, and low power consumption.

A rapid increase in the mobile data traffic can be attributed to mobile internet devices such as tablet computers, wearable watches and smart phones. There are several internet devices, which are not operating to their full capacity due to the slow internet connection and mobile data limitation imposed by the telecom operators. Based on this argument, it is logical to say that the mobile data

requirement is much larger than what the mobile infrastructure is capable to provide. Moreover, it is more practical to calculate the amount of data consumption from the capacity and speed of the mobile infrastructure instead of estimating it from the capacity of mobile internet devices.

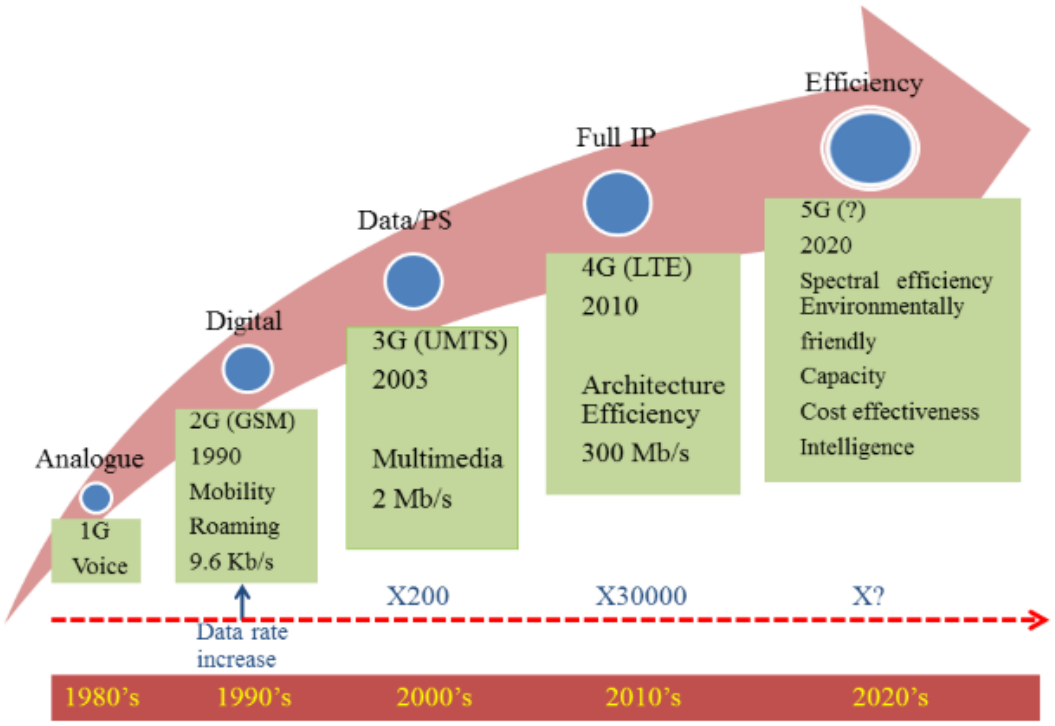


Figure 1.1: Evolution of wireless communications.

In the 4G mobile infrastructure, wireless standards such as Long Term Evolution (LTE) and Worldwide Interoperability for Microwave Access (WiMAX) were approved and the infrastructure based on these standards were implemented extensively throughout the world to satisfy the data requirements of mobile users. Both of these well known wireless standards make use of spectrally efficient modulation schemes such as orthogonal frequency-division multiplexing (OFDM). The system that utilizes OFDM modulation scheme is able to maximize the data throughput and network capacity. Figure 1.2 shows the extensive use of OFDM modulation scheme for different wireless communication standards for enhancing the data rate.

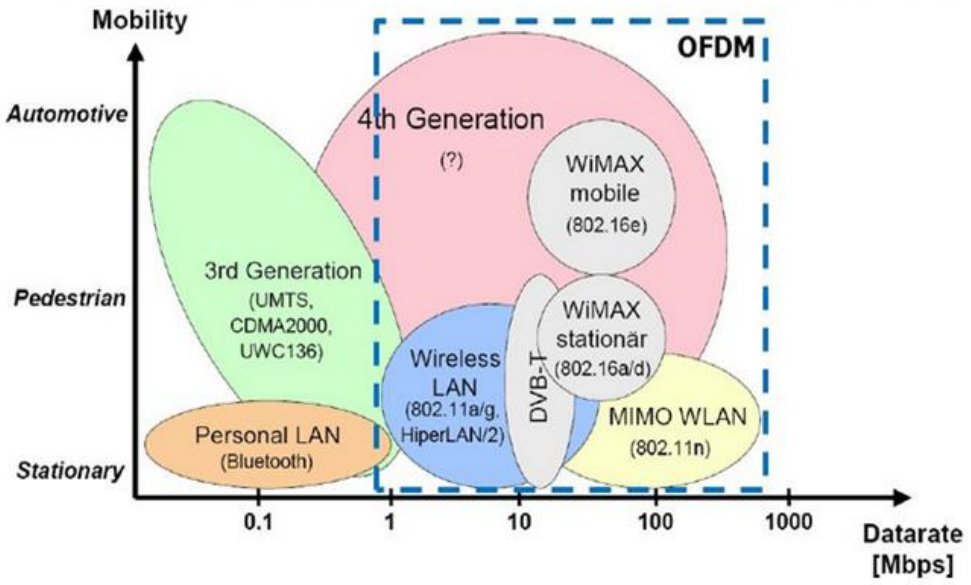


Figure 1.2: Use of OFDM modulation scheme in wireless communications.

If we look from the power amplifier (PA) perspective, a widespread use of higher order spectral modulation schemes to satisfy the growing demand of high data rate can also have significant effect on the power amplifier performance [2]. The most commonly used spectral modulation is OFDM and generally, it is based on four subcarriers, as depicted in Figure 1.3. An orthogonal frequency division multiplexing based system produces signals with a very high crest in the time domain subcarrier components, which are added through an inverse fast Fourier transformation (IFFT) operation. Consequently, when OFDM systems are compared with single carrier GSM systems, it has a very high peak-to-average power ratio (PAPR), as can be seen from Figure 1.4. Indeed, in an advanced wireless base-station, a signal with high peak-to-average power ratio is a major challenge for radio frequency PA designers; the reason of this is that power amplifier significantly reduces the average efficiency at the back-off power level.

High crest signal has fewer effects on the PA average efficiency during downlink frequency operation in a base-station. On the contrary, it has significant effects on the average efficiency of a PA during uplink frequency operation. This is due to the fact that the efficiency of the power amplifier is a major concern in mobile terminal devices and in base-stations due to the limited battery power and required expensive cooling setup, respectively. Moreover, a communication signal with high crest can also shrink the signal-to-quantization noise ratio (SQNR) of

the Analog to Digital Convertor (ADC) and Digital to Analog Convertor (DAC), while degrading the efficiency of the power amplifier in the transmitter [4].

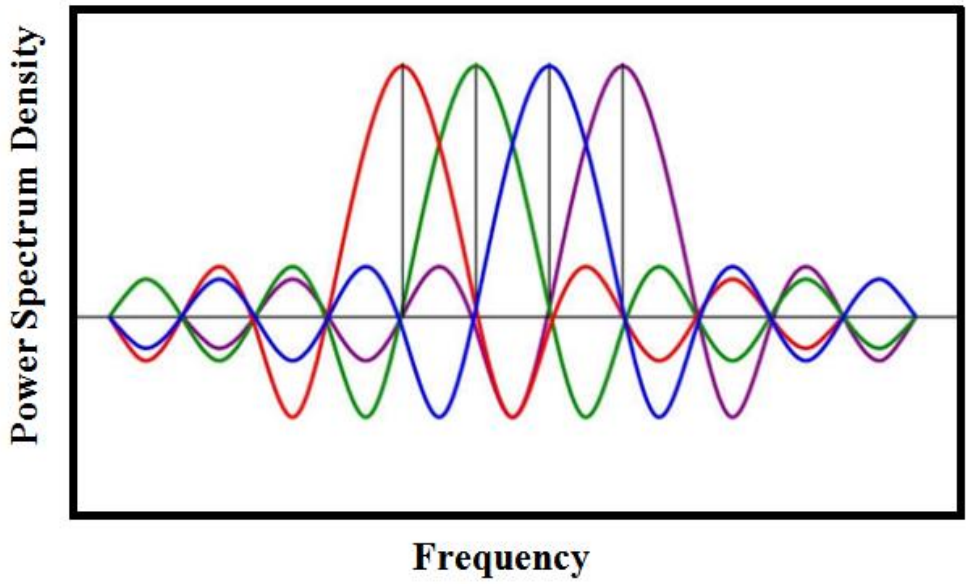


Figure 1.3: An OFDM modulation with four subcarriers.

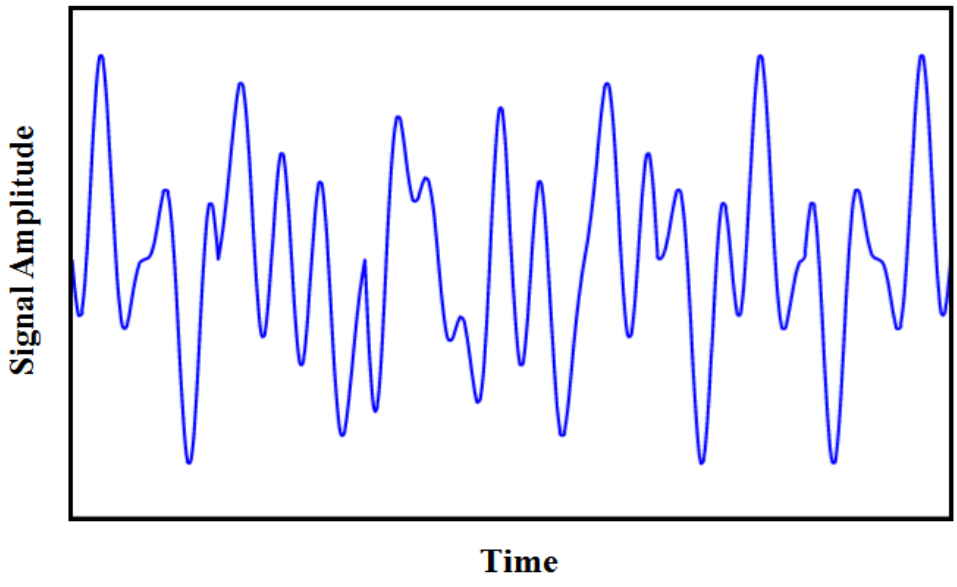


Figure 1.4: An OFDM waveform illustrating with high PAPR.

In emerging wireless standards, for maintaining high signal to noise ratio (SNR) and bit error rate (BER) at the receiver side of a base-station, a power amplifier with high linearity and high output power is required [5]. Furthermore, in the near future, the base-station PA design will be more complicated by the arrival of next generation standard in wireless communications. It is also required that the emerging and legacy standards must coexist for satisfying the data hanger of mobile devices. Generally, multiple narrowband radios are installed to support different standards such as WiFi, WiMAX, GSM and LTE. This approach is redundant in hardware and power inefficient as well.

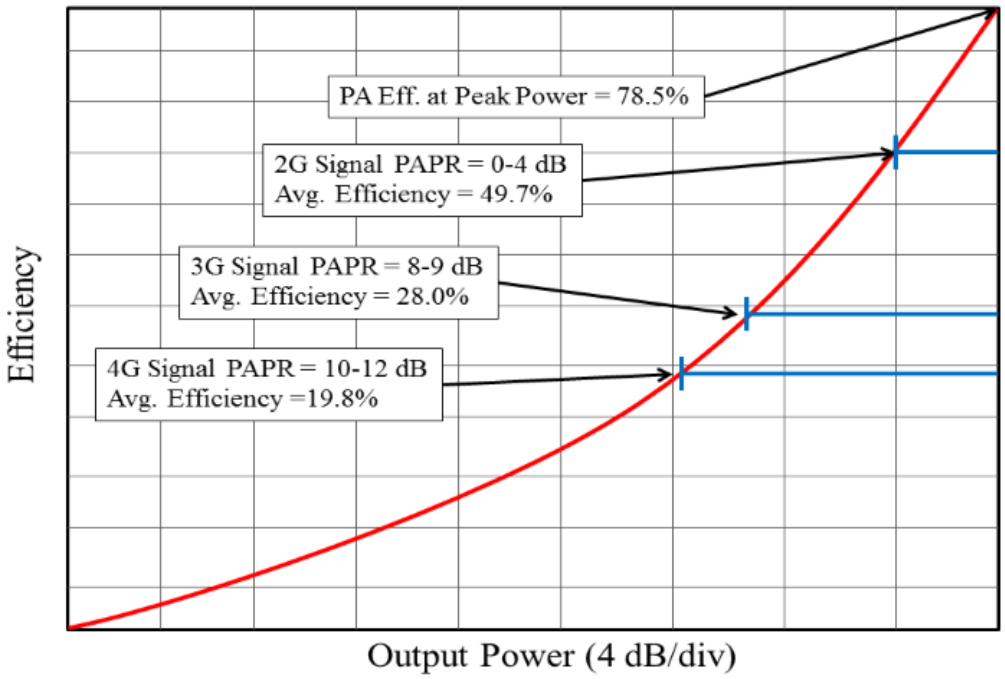


Figure 1.5: PAPR effect on power amplifier average efficiency.

Figure 1.5 shows the typical power amplifier efficiency versus output power; with the passage of time, the progress from the 1G to the 4G modulated signal's PAPR raised from 0 dB to 12 dB and the drain efficiency reduced from 78.5% from 19.8%, respectively. Finally, there are also environmental and ecological challenges and the power utilization should be as low as possible. It is presented in [6] that mobile networks alone contribute to 0.2% of the global CO_2 emissions and it is predicted that this Figure will rise to 0.4% in 2020.

1.2 Problem statement

As discussed in the previous section, the advanced base-station power amplifier needs to meet multiple criteria including efficiency, linearity, output power, and bandwidth. In particular, the amplifier must be highly efficient in terms of drain efficiency when operated with a high PAPR signal. To obtain high efficiency in power amplifier at back-off level, many advanced techniques have been proposed in the literature such as H. Chireix [7], Doherty power amplifier (DPA) [8] and the envelope-tracking amplifier (ET) [9]. The Doherty amplifier has been widely adopted in the industry thanks to its ease implementation and better average efficiency.

Unfortunately, the conventional Doherty power amplifier has a limited bandwidth. Therefore, even if it is capable of fulfilling the linearity and power output requirement of the modern base-station, the conventional DPA is not capable to satisfy the bandwidth requirement of modern base-station. The limited bandwidth means that more Doherty amplifiers are distributed in a single base-station, one for each standard that a mobile service provider uses. This could leads to inefficient power usage and surplus hardware.

In contrast to the outphasing power amplifier, the conventional DPA is based on a static phase between the sub-amplifier output signals. As an alternative, the load modulation is achieved by changing the amplitude of their relationship. The advantage of the DPA over the other advanced efficiency enhancement techniques is that mainly accurate amplitude ratios can be achieved using a single RF-driver combination with an analog power splitter and sub-gate-bias amplifier. This advantage ascertains the DPA as the best candidate for efficiency enhancement purpose without using any additional control circuitry.

Because of high efficiency and high linearity, DPA has become the prime choice of today's commercial RF transmitters for mobile communications. However, it has limited bandwidth. For example, Cripps in [10] reported that DPA has only 10% fractional bandwidth. Therefore, a number of solutions have been proposed to overcome the bandwidth limitation. The DPA has a hard time in meeting the wideband requirement. In the near future, with the arrival of new technology (5G), bandwidth requirements of a PA will be more demanding. In order to reduce the time to market for new technology and PA operation for multi-standards communication signals such as WiFi, WiMAX and LTE, a wideband PA is highly demanded.

In this thesis, we propose a new Class-AB PA with the extended bandwidth and linearity for the LTE communication band. In the second proposed design, an ultra-wide band Class-F PA is designed and implemented. In the third PA design, a single- and dual-input DPA for LTE application in the 3.5 GHz frequency band are presented and compared. Moreover, a novel design technique is proposed to extend the bandwidth of the conventional Doherty power amplifier. In order to validate the proposed technique, it is also applied on two 10W GaN HEMT devices and the designed PA presented satisfactory results. The proposed DPA is implemented and it meets all the requirements of a modern base-station. The advanced design technique is a fundamental reference point towards the construction of a single power amplifier capable of simultaneously support multiple wireless communication standards, reducing the complexity and the cost of the transmitter.

1.3 Thesis organization

The thesis is organized as follows. Chapter 2 provides the background and theory of conventional RF power amplifiers. All the fundamental figure-of-merits of the power amplifier are discussed in detail. Furthermore, operating classes of traditional and high efficiency power amplifiers are introduced based on the study of voltage and current waveforms. The input and output requirements of the matching network practices are outlined with the design of the widely adopted load-pull technique.

Chapter 3 outlines the design of a highly linear and broadband single-ended power amplifier using two-tone load-pull simulation and bias optimization technique to synthesize the matching networks. The design of a 5 W Class-AB PA for 1.9 to 2.5 GHz LTE communication band based on GaN HEMT active device is discussed in detail.

Chapter 4 proposes a novel design with ultra-wide bandwidth of the Class-F power amplifier based on 10 W GaN HEMT from Cree Inc. The conventional Class-F PA has high drain efficiency. However, it is a narrow bandwidth PA. Multiple harmonics termination is exploited for high drain efficiency and maintaining ultra-wide bandwidth as well.

Chapter 5 introduces the single- and dual-input Doherty amplifier, which uses two devices in parallel to obtain the improvement of the efficiency in power level of back-off. Derivations based on the concept of load modulation and the

conventional Doherty amplifier shows that it has a narrow bandwidth. The widely adopted traditional technique is outlined and a review of the literature shows the limited bandwidth of conventional Doherty amplifier. A conventional GaN HEMT based Doherty amplifier, with 600 MHz bandwidth is designed and implemented at 3.5 GHz for the LTE communication signal.

In chapter 6, a novel design technique is proposed to overcome the conventional Doherty power amplifier bandwidth limitation. The reasons of limited bandwidth of the widely adopted traditional technique are outlined. Moreover, it is explained that by regulating the offset-line of the auxiliary PA, it is possible to control the bandwidth of the proposed DPA. In order to validate the proposed technique, it is applied on two 10 W GaN HEMTs devices. The realized DPA exhibited satisfactory results as expected. The measured results show a good agreement with the simulated results.

Finally, in the last chapter of this thesis, a summary of the entire research work is presented. In addition to this, a future work to extend the practicability of the anticipated theory to higher frequencies is described.

Chapter 2

Power Amplifiers Overview

2.1 Introduction

In this chapter, we describe the underlying theory and design of a RF power amplifier for front-end transmitters. Key figure-of-merits (FOM) of a typical power amplifier (PA) and various classes of operations are briefly discussed as well. In addition to this, the practical design considerations of a single-ended PA such as the parasitic effects of a device, the package effect on load impedances, stability, input and output matching network designs are presented. The study in the subsequent chapters provided the basis for understanding the advanced circuit design techniques for high efficiency PA such as Class-F and Doherty power amplifiers.

2.2 Power amplifier and FOM

A PA is a non-linear system that has an output power level equal to the input power multiplied by gain at a specified frequency [11]. A transmitter is a backbone of modern wireless communication system. In front-end transmitter, an information input signal is modulated at a specific high frequency. After that, the modulated input signal is amplified by using a PA and then the amplified signal is radiated from the antenna [12]. A simplified block diagram of the front-end transmitter is shown in Figure 2.1.

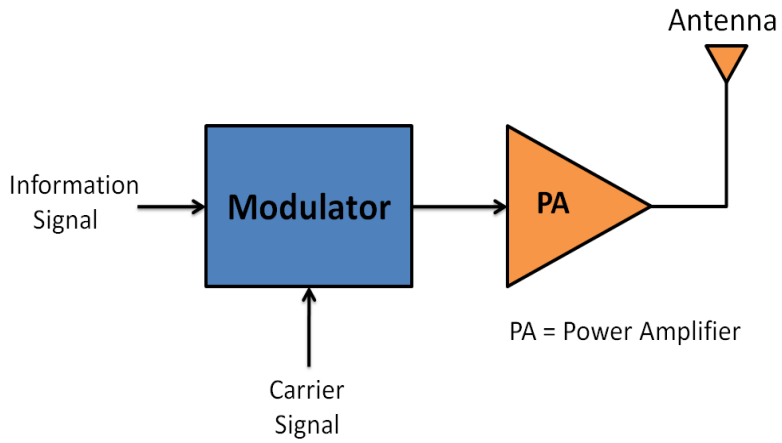


Figure 2.1: A simplified block diagram of a front-end transmitter.

A PA is a critical module in frond-end transmitter architecture. The working class of a PA can be described such as Class-A, Class-AB, Class-B, Class-C, and Class-F. In addition to the working class, there are some important FOM for PA characterization, for instance gain, output power, linearity and efficiency. Whereas, PA efficiency is straightway linked to the DC power consumption. If a PA operational efficiency is not adequate, a large amount of power is consumed instead of passing to the antenna. As a result, PA increases the cost of transmission in wireless communication. Moreover, other depraved effects in the form of shorter device life, required addition cooling setup and week compactness. Three important FOM of a PA gain, efficiency and intermodulation are described in following sub-sections.

2.2.1 Gain and gain compression point (P1dB)

The gain of an amplifier is defined as the ratio of its output power to the input power

$$G = 10log_{10}\left(\frac{P_{OUT}}{P_{IN}}\right) \qquad (2.1)$$

Where in equation 2.1, G is the gain of an amplifier in dB, P_{OUT} and P_{IN} are output power and input power in watt, respectively. When a PA is supplied with comparatively small input power signal, the gain of the PA is flat and independent of input signal power level up to certain point. On the other hand, the PA gain "drop" depends on the selected class of operation, when it is driven with comparatively a large input power signal due to transistor nonlinearities, a curve

of typical PA gain response is shown in Figure 2.2 (b). As a matter of fact, the proposed analysis is strictly correct only under Class-A operation.

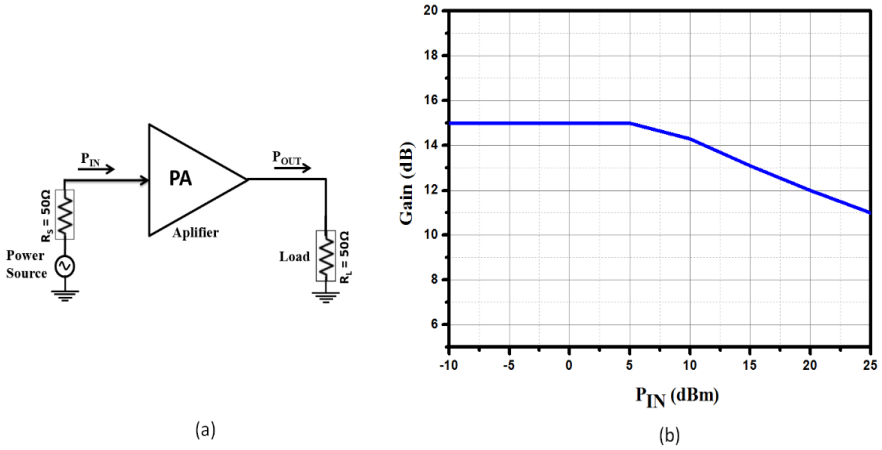


Figure 2.2: (a) PA gain measurement schematic and (b) gain vs. input power plot.

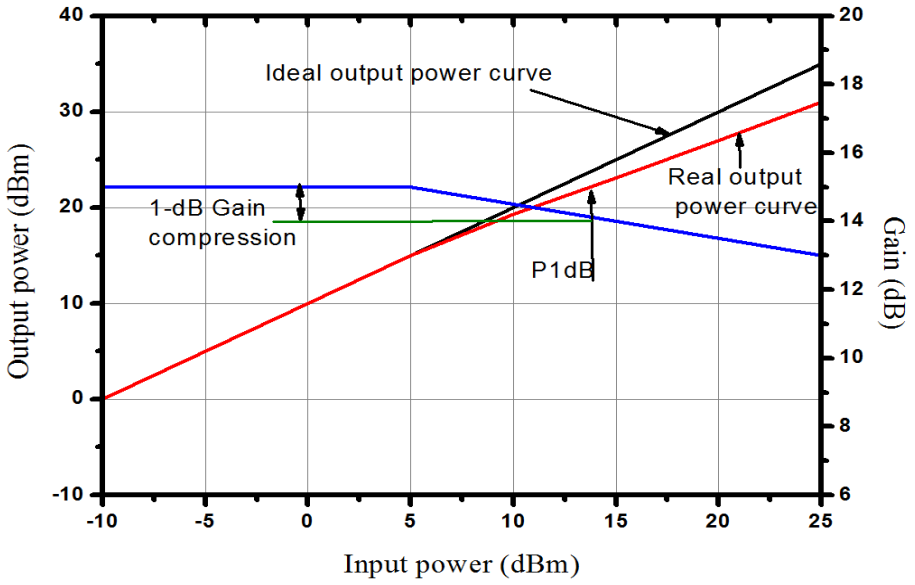


Figure 2.3: Plot for 1dB compression point of a Class-A power amplifier.

As described above, when the supplied input power of a PA reaches to certain power level, the gain of a PA start to drops due to the presence of nonlinearities in transistor. In order to describe the linearity of an amplifier, 1 dB compression point (P_{1dB}) is considered, that is the point where gain of a PA declined 1 dB lower than its small signal gain, as it is presented in Figure 2.3. In real system

application, in order to get higher gain sometime two or more PAs are cascaded. For two cascaded PAs, the gain of the PA is depend on second PA and the effect of P1dB on system can be formed

$$G = G_0 - e^{\frac{P_{IN} - P_{IN1dB}}{5}} \qquad (2.2)$$

Where in equations 2.2, G is the gain of the single-stage amplifier. G_0 and P_{IN} are small-signal gain (dB) and input power (W) of the amplifier, respectively. Therefore, P_{1dB} of the cascaded amplifier is (P_{IN1dB} + G_0 - 1).

2.2.2 Power efficiency

An amplifier efficiency can be defined as the ratio of radio frequency (RF) output power to the injected DC power. In wireless applications, we mostly concerned with output power at the fundamental frequency. Efficiency of an amplifier can also be completely determined by the time domain voltage and current waveforms at the device intrinsic drain terminal. PA should provide high efficiency, when its drain and current voltage waveforms have minimum overlap as in Class-F power amplifier. Conversely, PA has low efficiency in case of Class-A amplifier due to large overlap exists in current and voltage waveforms.

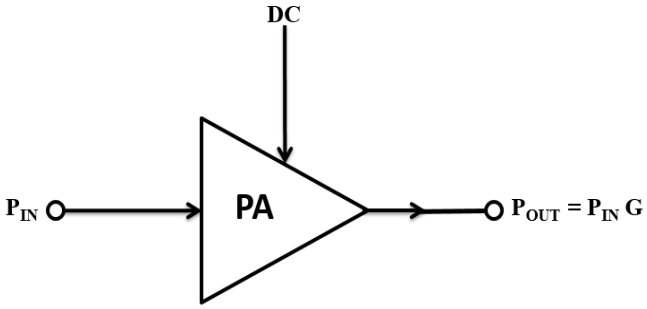


Figure 2.4: Power amplifier concept.

At any given frequency gain of an amplifier can be calculated by given equation (2.3) below

$$G\,(f_0) = \frac{P_{OUT}(f_0)}{P_{IN}(f_0)} \qquad (2.3)$$

In equation 2.3, P_{IN} and P_{OUT} are the input and output power of the PA at a specific frequency, respectively. As explained above, power amplifiers increase the power of the input signal and transforms the DC power into RF power at a fundamental frequency (f_0). Unfortunately, some quantity of the injected DC power to the PA is dissipated in the form of heat from the active device and some quantity of the injected power is sent to the harmonics at drain terminal. Total DC power consummation can be described by equation 2.4 given below

$$P_{DC}(f_0) = P_{OUT}(f_0) + P_{DIS} + \sum_{n=2}^{\infty} P_{OUT}(nf_0) \qquad (2.4)$$

where, $P_{OUT}(f_0)$ is the output of the amplifier at a specified frequency. P_{DIS} is the dissipated power from the active device and last term in the equation is the harmonics power. PA efficiency can be defined as Drain efficiency (DE) and Power Added Efficiency (PAE). Drain efficiency is the ratio between output powers to the supplied DC power [10]

$$\eta = \frac{P_{OUT}}{P_{DC}} \qquad (2.5)$$

where P_{OUT} is the output power and P_{DC} is the DC power consumption of the amplifier. Power Added Efficiency (PAE) is the ratio of difference between output and input power to the DC power consumption [10]

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}}{P_{DC}}\left(1 - \frac{1}{G}\right) \qquad (2.6)$$

In equation 2.6, P_{OUT} is the output power, P_{IN} is the input power, P_{DC} is the DC power consumption and G is the gain of an amplifier.

2.2.3 Intermodulation distortion

The intermodulation distortion (IMD_3) is another figure-of-merit used to describe the linearity of a power amplifier. IMD_3 involves the use of a two-tones stimulus. If the power of two-tones is equal, then it is the difference between the power of the fundamental signal and the third-order products. IMD_3 can be calculated from the subsequent equation [13]

$$IMD_3 = P_O - P_{3O} \qquad (2.7)$$

where P_O is the output power of the fundamental signal of the DUT, and P_{3O} is the output power level of third-order products. IMD_3 should be as low as possible for a linear power amplifier or it should be within the limit of communication standard. Intermodulation distortion products are spaced too close to the fundamental frequency stimulus, as can be seen from Figure 2.5. These upper and lower intermodulation distortion products should be perfectly filtered for noise free communication. In order to measure the IP3 performance of a system, the two fundamental tones powers are set at the same power level. A 1 dB change in the fundamental tones results in a 3 dB change in the third-order distortion products.

In addition to IMD_3 and IP3, linearity of a power amplifier can also be determined by ACPRs, also known as Adjacent Channel Leakage Ratio (ACLR). ACPR linearity metric is used in many wireless standards such as UMTS or 3GPP LTE to define the power amplifier and system linearity. ACPR can be defined by the ratio of power in a modulated signal versus power emitted into an adjacent channel [14]. In order to measure ACPR, one must provide the device under test (DUT) with a modulated stimulus.

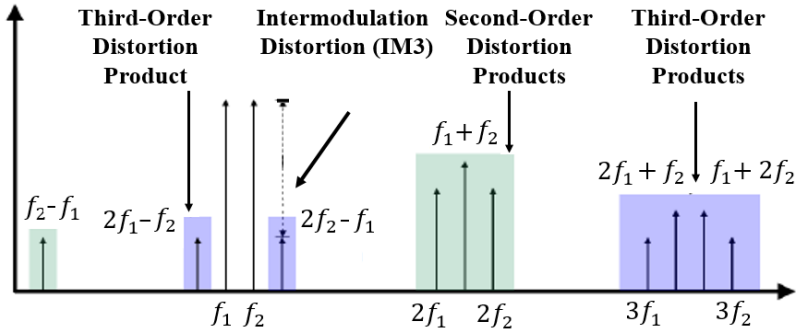


Figure 2.5: Intermodulation lower and upper tones due to non-linear device [14].

2.3 Power amplifier classes

Transconductance power amplifiers are non-linear systems that have an output power level equal to the input power multiplied by gain at a specified frequency [11]. A transconductance power amplifier is used as a controlled current sources and can be described by their working class such as Class-A, Class-AB, Class-B, and Class-C amplifiers. These amplifiers are extensively deployed in wireless transmitters and have been discussed in detail in number of

books/articles [10], [15-17]. Figure 2.6 shows a simplest circuit diagram of Class-A, Class-AB, Class-B, Class-C amplifiers. The PA circuit is single-ended. It is assumed that the RF choke, DC-coupling capacitor and the filter are all ideal component or circuit.

The easiest way to describe the transconductance amplifiers classes is the conduction angle. Class-A amplifier has a conduction angle of $\theta_C = 2\pi$, Class-AB amplifier has a conduction angle of $\pi < \theta_C < 2\pi$, Class-B amplifier has a conduction angle of π, and Class-C amplifier has a conduction angle of $0 < \theta_C < \pi$. In Figure 2.6, current-voltage waveforms at the drain and gate terminal of the amplifier are drown for a Class-A amplifier. The Class-A amplifier is a highly linear and also the most "well-behaved" amplifier.

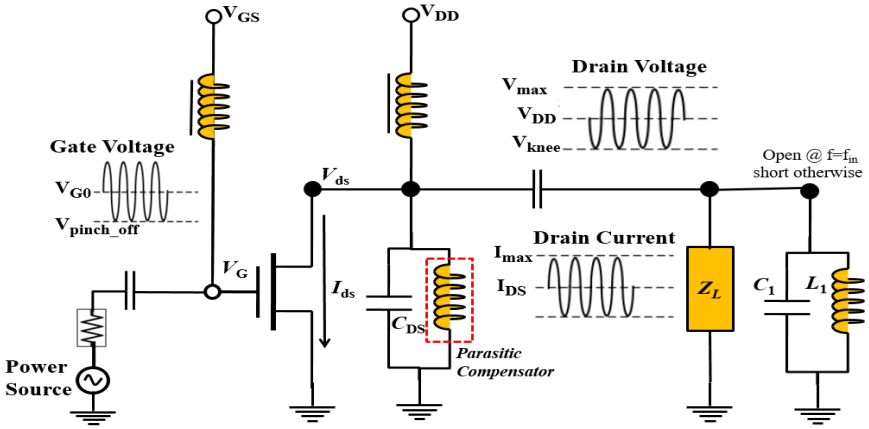


Figure 2.6: Simplified diagram of Class-A, -AB, -B and –C amplifier.

2.3.1 Class-A amplifier

Regardless of the Class-A amplifier's simplest architecture, it also offers efficiency and linearity benchmark for other advanced classes of operation. Moreover, the concept of load line analysis that is easily illustrated using a Class-A amplifier; is applicable to other classes of operation as well. Class-A PA has a conduction angle of $\theta_C = 2\pi$, and its voltage-current waveforms are presented in Figure 2.7. The maximum output power of a Class-A PA can be calculated by given equations [10]

$$P_{Max} = \frac{(V_{max} - V_{knee})\, I_{max}}{8} \qquad (2.8)$$

Where in equation (2.8), V_{max} and V_{knee} are the breakdown voltage and the knee voltage of Class-A PA, respectively. I_{max} is the maximum bearable current of the elected transistor. Although, Class-A amplifier has high linearity and output power compare to other classes. However, it has a major disadvantage. Theoretically, the maximum possible efficiency is only 50%. In practice, Class-A efficiency is significantly reduced to about 30-35% for L-band applications. If we assume practical possible efficiency's value is 33% from a PA. In this case, the amount of heat produced by a transistor can be higher than the heat-handling capability of a common-source transistor package. Because of this reason, Class-A amplifier is not an appropriate choice for L-band high power application.

Nowadays, Class-A amplifiers are only used at upper microwave frequency from 5 GHz to millimeter-wave region. The reasons of using Class-A PA at high frequency is that it requires comparatively less input power to drive the PA and it has higher small-signal gain compare to other classes as well. Since at microwave and millimetre frequencies, the power gain is typically the restrictive feature in PA design, Class-A is consider an appropriate choice.

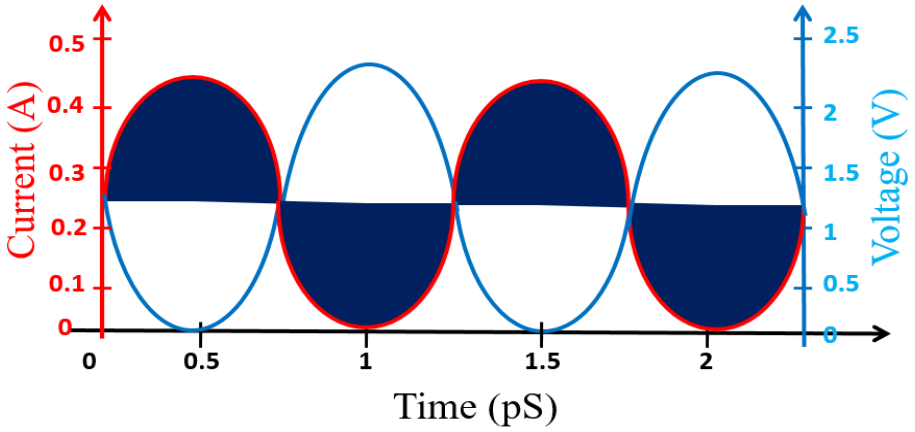


Figure 2.7: Current and voltage waveforms of a Class-A power amplifier.

2.3.2 Reduced conduction angle modes: Class -AB, -B, -C

In order to increase the drain efficiency of an amplifier, the ratio of the fundamental signal output power to the DC power consumed must increase, as defined in equation (2.5). One way to enhance the drain efficiency is to regulate the gate bias (V_{GG}) of the transistor; as a result, conduction (θ_C) of the active device is reduced accordingly. For reduced conduction angle modes amplifiers, a

part of the gate voltage waveform dips underneath the zero level into the non-conducting area. Based on conduction angle, amplifier can be classified into different classes, which are described in the following paragraphs.

The current and voltage waveforms of a Class-AB amplifier are shown in Figure 2.8. Since, the gate bias voltage (V_{GG}) of a Class-AB amplifier is reduced from Class-A amplifier, the current clipping occurs. Even though the current clipping produces harmonics and nonlinear effects, Class-AB amplifier is still a running horse for L-band wireless application due to fair compensation between linearity and drain efficiency. Class-AB has higher efficiency and lower linearity compare to Class-A amplifiers. Many PA designers use Class-AB amplifiers as a starting point, and apply harmonic control techniques to improve efficiency. We designed a 5 W Class-AB amplifier by terminating second and third harmonics at the drain terminal of the active device. The detail of the proposed Class-AB amplifier is given in the subsequent chapter.

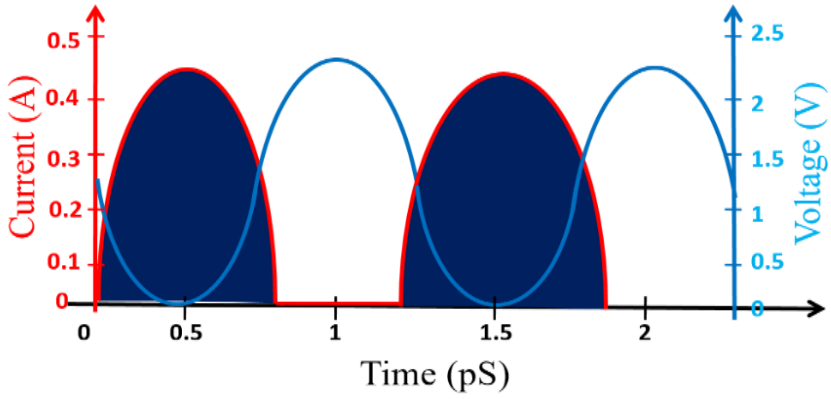


Figure 2.8: Current and voltage waveforms of a Class-AB power amplifier.

The current and voltage waveforms of a Class-B amplifier are shown in Figure 2.9. Class-B amplifier is a transition in the middle of the Class-AB and the Class-C amplifiers. The theoretical possible maximum drain efficiency of a Class-B amplifier is 78.5%, which is significantly higher than the Class-A amplifier. In practice, Class-B amplifier can achieve a drain efficiency of 60% in L-band. Since, the gate bias voltage (V_{GG}) of a Class-B amplifier is reduced from Class-AB amplifier; the more current clipping happens compared to Class-AB amplifier. The Class-B amplifier efficiency is much higher than the Class-A amplifier. Therefore, there is no more need of a sophisticated and expansive cooling setup. Consequently, it is a low cost amplifier. However, its linearity is worse compared to Class-A and Class-AB modules.

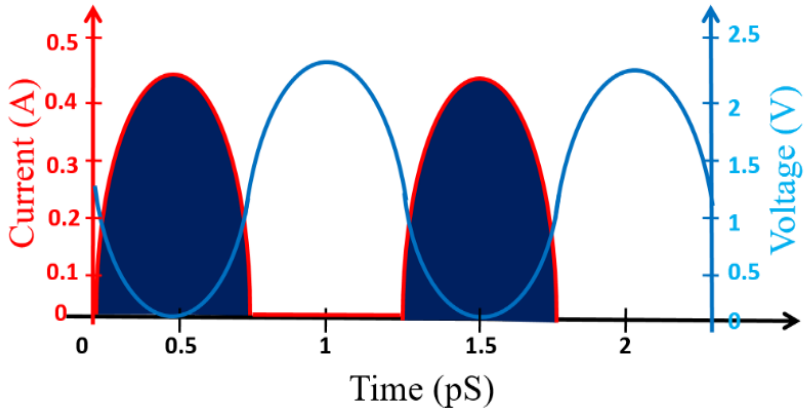


Figure 2.9: Current and voltage waveforms a of Class-B power amplifier.

The current and voltage waveforms of a Class-C amplifier is shown in Figure 2.10. Class-C amplifier is an efficient amplifier compared to other reduced angle amplifiers. Theoretically, it has drain efficiency from 78.5 to 100%. However, there are several drawbacks to implement Class-C amplifier in the L-band application. The first disadvantage is the high drain efficiency originates at the cost of the power gain. The other disadvantages is that the amplifier is highly nonlinear. Consequently, it can be exploited only for highly nonlinear systems, or will require additional complex linearization techniques to improve linearity. Theoretically, maximum possible efficiency of different classes of amplifier operation are presented in Table 2.1.

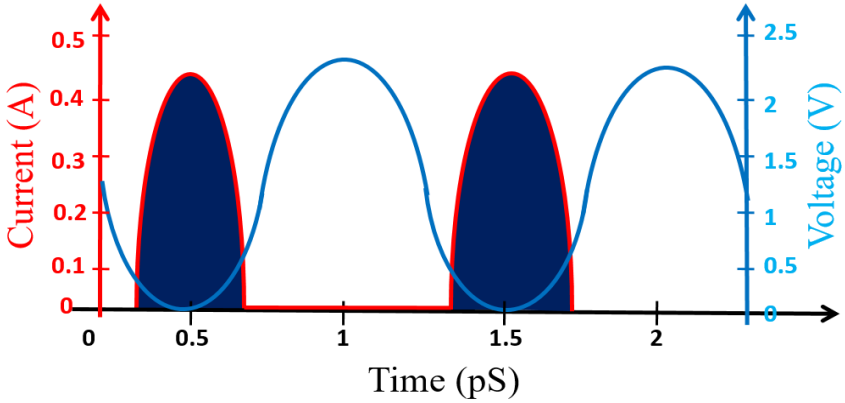


Figure 2.10: Current and voltage waveforms a of Class-C power amplifier.

Table 2.1: Theoretically efficiency of different classes of amplifier operation.

Class of operation	Peak drain efficiency ($\boldsymbol{\eta}$)
Class-A	$\eta = 50\%$
Class-AB	$50\% < \eta < 78.5\%$
Class-B	$\eta = 78.5\%$
Class-C	$78.5\% < \eta < 100\%$

2.3.3 Switch-mode Class-F and F^{-1} power amplifier

Switching-mode power amplifiers use active transistor as a switch. Active device is ideally fully on (short-circuit) or fully off (open-circuit). Switching-mode PA are very common in switch-mode power supply (SMPS). However, recently these circuits have been exploited for RF power amplifiers as well, because of the availability of commercial active devices with sufficient gain and power at microwave frequencies. The theoretical maximum drain efficiency for Class-E and Class-E/F amplifiers is 100%; in practice many published articles reported maximum drain efficiencies from 70-85% [18-20]. Class-F and Class-F^{-1} amplifiers are built on waveform shaping technique by properly terminating the harmonics in output-matching network.

Typically, Class-F power amplifier is biased in Class-B mode and active device is precisely loaded with harmonics terminations at fundamental and harmonic frequencies. For an ideal Class-F operation open-circuit terminations at all the odd harmonics and short-circuit terminations at all the even harmonics are required, and vice versa for Class-F^{-1} amplifier, as shown in Figure 2.11. Due to the switching nature of the active device, harmonics will be generated within the transistor and harmonics control network is presenting the ideal short-circuits at the even harmonics and open-circuits at the odd ones. Ideal Class-F PA drain waveforms consist of squared drain voltage and truncated sinusoidal drain current. The Class-F power amplifier drain voltage waveform comprises fundamental signal and odd harmonics, which is approximately exhibit a square wave and drain current waveform consist of even harmonics, respectively. Figure 2.12 shows the ideal drain and voltage current waveforms of the Class-F PA at the intrinsic drain terminal of the active device. Moreover, in an ideal Class-F PA

load impedance at all odd harmonics should be tuned to open circuit (Z = ∞) and the load impedance at all even harmonic should be tuned to short circuit (Z = 0). The third harmonic of the drain voltage has to be out-of-phase with the fundamental to generate the Class-F -like drain voltage waveform.

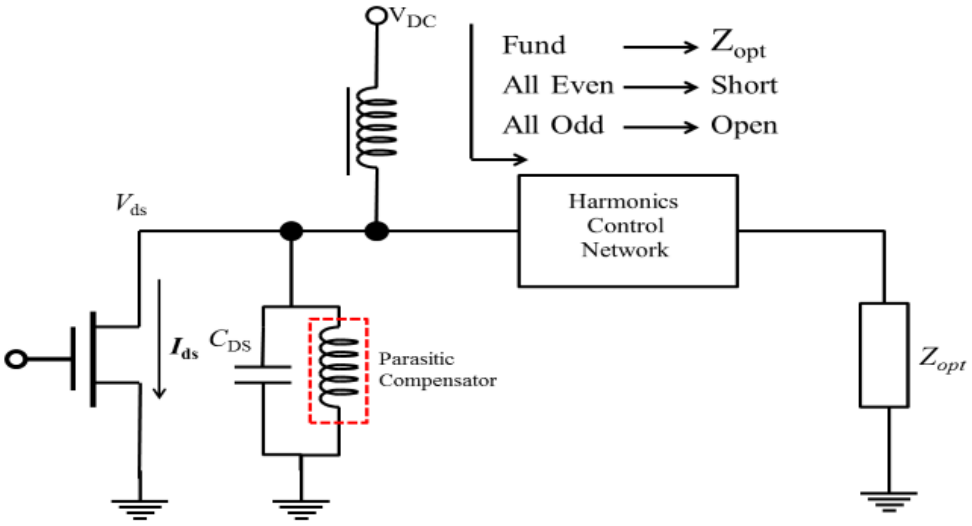


Figure 2.11: Class-F power amplifier topology with ideal infinite harmonic termination.

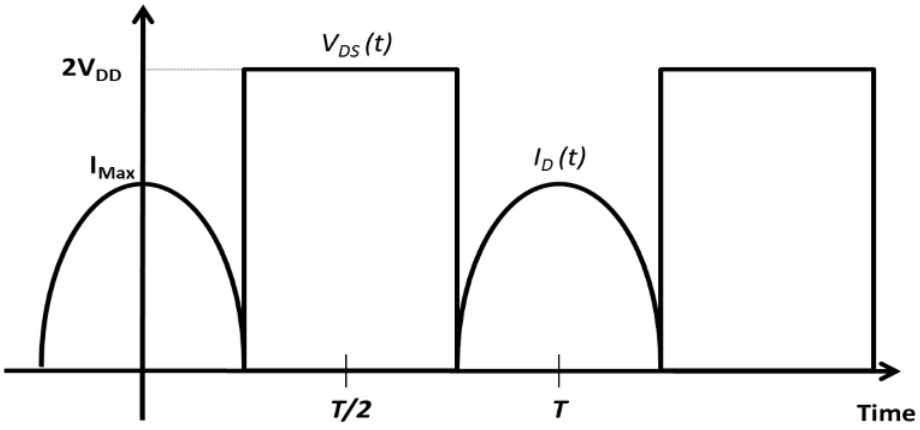


Figure 2.12: Ideal drain voltage and current waveforms for a Class-F power amplifier [22].

The general equations of Class-F PA for current and voltage waveforms are reported in [21]. These equations are (2.9) and (2.10), where ∅ is the phase difference between the fundamental signal and harmonics

$V(t) = V_{ds} + V_1\cos(w_o t+\emptyset_1) + V_2\cos(2w_o t+\emptyset_2) + V_3\cos(3w_o t+\emptyset_3) + ...$ (2.9)

$I(t) = I_{dd} + I_1\cos(w_o t+\emptyset_1) + I_2\cos(2w_o t+\emptyset_2) + I_3\cos(3w_o t+\emptyset_3) + \ldots\ldots$ (2.10)

Class-F PA can only maximize efficiency and output power, if no overlap exists between current and voltage waveforms at intrinsic drain terminal of the active device. No overlap between current and voltage waveforms means less power dissipation in active device. Furthermore, no power is sent to harmonics.

$$i_D(\theta) = \begin{cases} I_{Max}.\cos(\theta) & If \quad -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 0 & otherwise \end{cases} \quad (2.11)$$

$$v_{DS}(\theta) = \begin{cases} 0 & If \quad -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 2.VDD & otherwise \end{cases} \quad (2.12)$$

As it can be seen from expression (2.11) and (2.12), current ($i_D(\theta)$) and voltage ($v_{DS}(\theta)$) components with the same order does not exist [22]. Moreover, it also clear from Figure 2.12 that ideally drain current and voltage waveforms do not overlap at any point. As a result null power dissipation in the active device and the first condition for maximizing the efficiency is achieved [22].

$$P_{diss} = \frac{1}{T}\int_0^T V_{DS}(t).\, i_D(t)dt = 0 \quad (2.13)$$

From the Fourier analysis of drain current and voltage waveforms, their harmonic components are expressed as:

$$i_D(\theta) = \sum_{n=0}^{\infty} I_n.\, cos(n\theta) \quad (2.14)$$

Where

$$I_n = \begin{cases} \frac{I_{Max}}{\pi} & n = 0 \\ \frac{I_{Max}}{2} & n = 1 \\ \frac{2}{2} \cdot \frac{I_{Max}}{n^2 - 1} \left(-1\right)^{\frac{n}{2}+1} & n \ even \\ 0 & n \ odd \end{cases}$$

And

$$v_{DS}(\theta) = \sum_{n=0}^{\infty} V_n . cos(n\theta) \qquad (2.15)$$

Where

$$V_n = \begin{cases} V_{DD} & n = 0 \\ -\frac{4 \cdot V_{DD}}{2} & n = 1 \\ 0 & n \ even \\ \frac{4 \cdot V_{DD}}{\pi} \frac{(-1)^{\frac{n+1}{2}}}{n} & n \ odd \end{cases}$$

As it can be noted from the expressions above, current and voltage, Fourier components with the same order n are alternately not present. As a result, the power delivered at harmonic frequencies (Pout, nf = 0, n > 1) is zeroed, thus also fulfilling the remaining condition to achieve maximum efficiency. In summary, both conditions maximizing the efficiency are simultaneously fulfilled and a theoretical 100% drain efficiency is achieved.

On the other hand, however, previously described ideal waveforms must be generated via a proper output network, able to synthesize all the requested loading conditions for the output current harmonic content. The values of terminations are easily inferred as the ratio between the respective Fourier components Vn and In, i.e.

$$Z_n = \frac{V_n}{I_n} = \begin{cases} \frac{8}{\pi}.\frac{V_{DD}}{I_{Max}} & n = 1 \\ 0 & n\ even \\ \infty & n\ odd \end{cases}$$

In particular, the terminating impedance at fundamental frequency must be purely resistive (R_F), since it results from perfectly phased behaver of the other harmonics.

$$R_F = \frac{4}{\pi} . \frac{2 . V_{DD}}{I_{Max}} \qquad (2.16)$$

The requested set of terminations, including harmonics, has to be synthesized by a purely passive output-matching network. As anticipated, it results in a short-circuit condition for even harmonics and an open-circuit for odd ones. Finally, a comprehensive comparison is presented in Table 2.2 based on theoretically performance in terms of efficiency, output power and linearity of all the amplifiers classes.

Table 2.2: Summary of amplifier classes of operation.

Class	Efficiency	Power	Linearity	Conduction angle
A	50% Max.	High	Best	100%
AB	< 68%	High	Some Distortion	< 100%
B	< 78.5%	High	More Distortion	50%
C	78.5%	Low	Poor	< 50%
D	< 100%	Medium	Moderate	50%
E/F	100%	Low	Poor	0%

2.4 Power amplifier design flow

PA design specifications and selection of an appropriate device is the first step toward power amplifier design, as shown in Figure 2.13. The key parameters to consider for selecting a transistor are gain, power capability and input/output impedances. After the selection of the appropriate transistor, stability at in-band and out-of-band frequencies should be determined. If the selected transistor is not unconditionally stable, lumped component based stability networks are inserted at the input of the transistor in order to achieve stability. After making transistor

stability at operating frequencies, optimum load and source impedances are extracted for achieving best power and gain performance. In this research work, optimum load and source impedances are decided through the load- and source-pull simulations in ADS. From the power and efficiency contours on a Smith chart of the selected device, the optimum impedances can be selected for required performance. In final step, biasing networks are designed for required band and impedance transformation. The designed procedure and practical design constrains of a PA from the first to final step of realization are discussed in detail in next section.

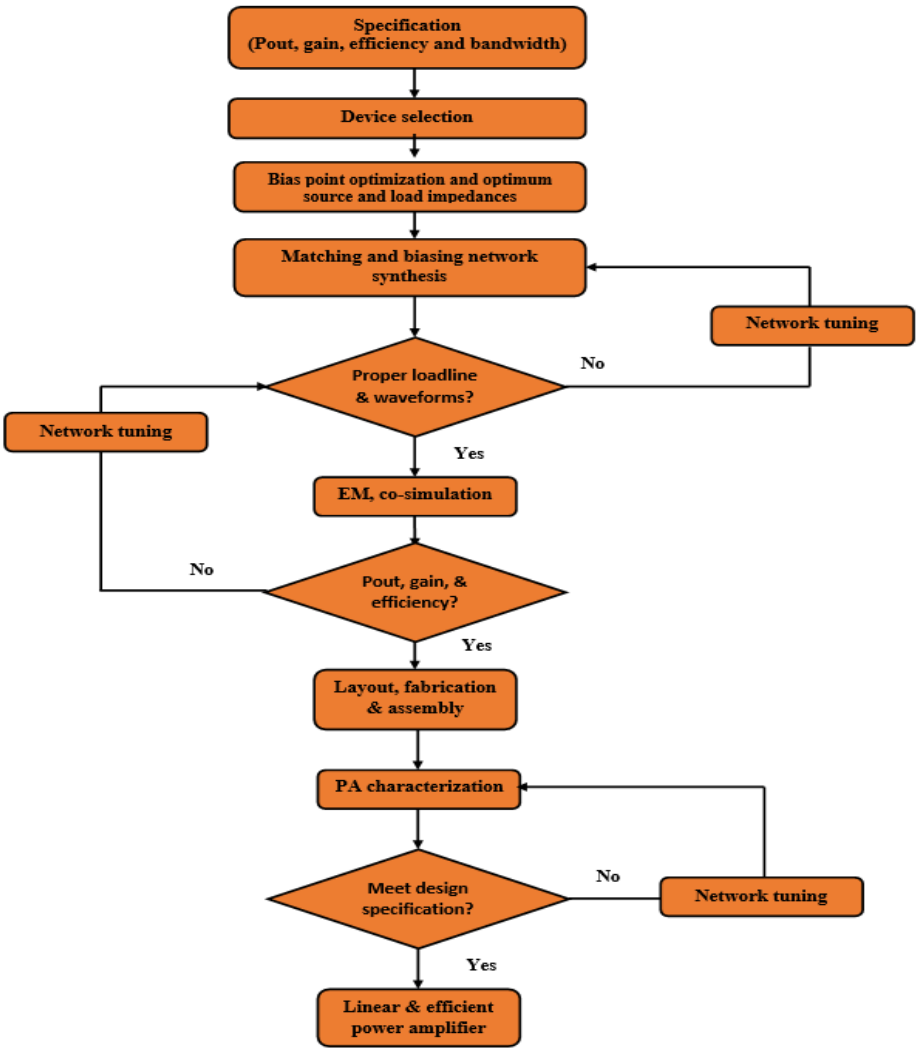


Figure 2.13: Flow chart of a typical power amplifier.

2.5 Power amplifier design

The power amplifier theory, classes and design flow described in above section primarily focused on the ideal working environments that predict a highly efficient amplifier operation and relaxed strategy to develop a faultless amplifier. However, in practice there are many challenges of applying these concepts in practical power amplifiers. In the following sections, we will present these issues and the solutions for applying theoretical concepts. Figure 2.14 shows the main modules of a real-world RF power amplifier.

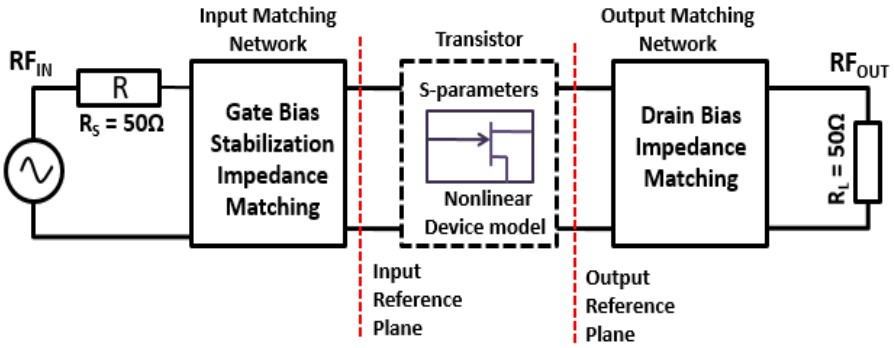


Figure 2.14: Generic block scheme of a single-stage Microwave amplifier.

2.5.1 Device package & de-embedding prasitics

Usually, hybrid RF PAs use packaged devices, in order to protect the bare device from external environment and to help the thermal dissipation as well. Limited number of designs are available in the literatures that uses pre-matched transistors. For enhancing the design flexibility, many PA designer use classically unmatched transistor. Figure 2.14 is presenting a conventional packaged, unmatched active device after removing the top cover. The transistor die is fixed on thermal conductivity flange, which also works as source terminal for an electrical ground. The bond-wires are exploited for drain and gate terminal connection to the external world. The model of a typical active device based on lumped and distributive components depicted in Figure 2.16. Figure 2.15 shows the bare die generic signal model reported in [13]. Where major parasitics are on the drain side of the device and represented L1 and TL1 respectively. When accounting the package effect, the packaged device has a narrower matching bandwidth and more frequency dispersive effects compare to a bare die device. Due to the impedance alteration produced by the device and package parasitics is

required to address the impedance shift compensation in the matching network design, the reference plane of interest may shift from the current generator plane to the package reference plane. Multi-harmonics termination in the output matching networks at the intrinsic drain is problematic due to inaccuracy in the active device parasitics model. At microwave frequencies, the harmonics termination is even worse, particularly at the intrinsic drain terminal.

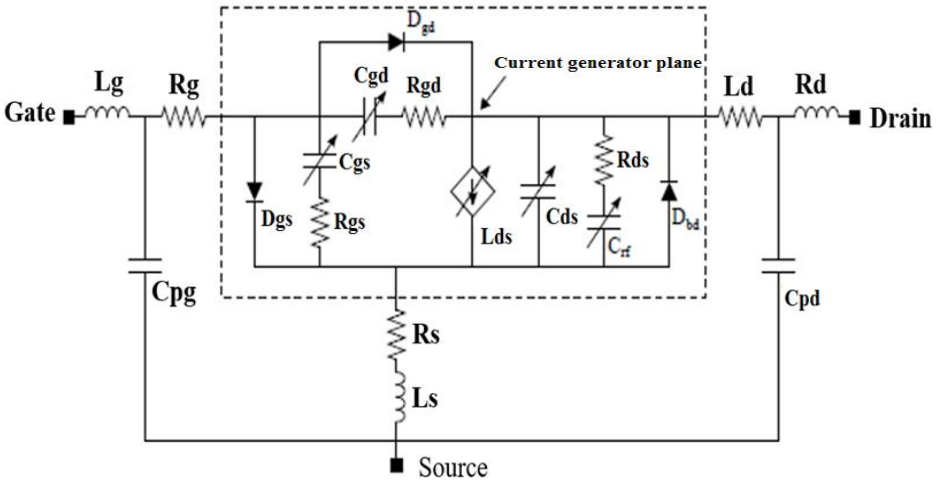


Figure 2.15: A generic signal model [23].

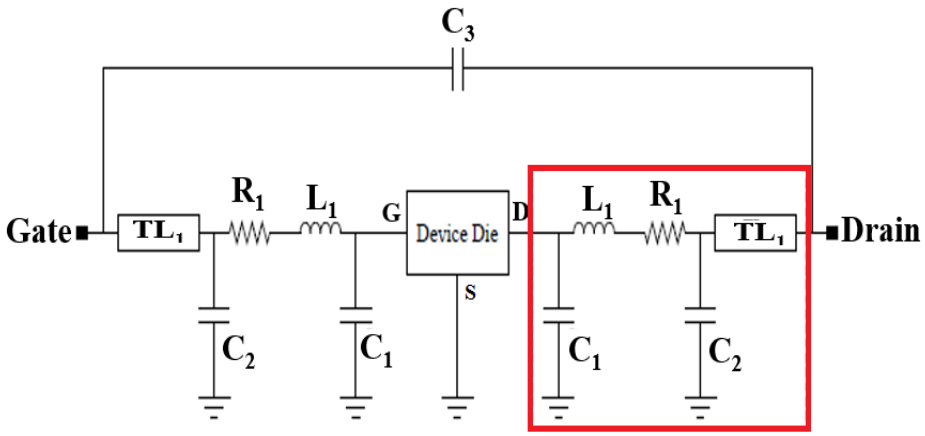


Figure 2.16: A typical device package model.

2.5.2 Bias network and stability

Biasing networks are used to supply the gate and drain voltages to the active device for maintaining the drain current at predefined bias voltages. Generally, PA is required two biasing circuits to supply the drain and gate voltages to the active device. Gate and drain biasing circuits should be capable to block the RF signal for entering into the power supplies throughout the desired band of interest and should presents low impedance at lower frequency. To stop the RF signal from entering into the DC supply, an RF choke is connected between the DC supply and the transistor. The RF choke can be a large inductor or a short-circuited λ/4 transmission line at the designed frequency. Both, RF choke and quarter-wave transmission line should present a very high resistance to the RF input signal at the fundamental frequency. A λ/4 transmission line can also work as second harmonics short stub as well.

Moreover, both the drain and gate basing networks should provide high impedance to the RF input signal for a required bandwidth to stop the bias modulation. The RF input and output should be DC-decoupled to stop interference. Therefore, DC blocking capacitors are placed in series with the matching networks. The value of the blocking capacitors is chosen so that the capacitors behave as a short circuit at the fundamental frequency. The most commonly used biasing network in the literature is based on a λ/4 transmission line at the designed frequency with 50 Ω impedance characterization for the both drain and gate biasing circuits in the RF power amplifier. A short circuit λ/4 transmission line transforms the short into open at RF frequency. The input impedance of a short circuit transformer can be calculated from transmission line theory by using equation (2.17) given below [24]

$$Z_{in} = jZ_0 \tan\beta l \approx j2\pi Z_0 \sqrt{\frac{\varepsilon_{eff}(f_0)\, f_0 l}{C_0}} \qquad (2.17)$$

Where $\beta = 2\pi/\lambda_g$ is the propagation coefficient, l is the physical length, $\varepsilon_{eff}(f_0)$ is the effective dielectric constant at the f_0, and Z_0 is the characteristics impedance of the λ/4 transmission line. After the selection of an appropriate device and adding the biasing networks, most important step in the PA design is to make transistor stable. A stability test should be performed on the selected

transistor. If the selected device is not stable at the designed frequency, amplifier will start oscillating and high power can damage the device. There are several ways to verify the PA stability, the details of stability parameters and stability circuits are presented in this paper [25]. In this thesis, three key parameters are considered to ensure stability in-band and out-band stability. The first considered parameter is stability factors, which can be calculated from two-port S-parameters. Equation 2.18 gives the value for Rollet stability factor 'K', which has to be greater than or equal to unity (K ≥ 1) for unconditionally stable condition. Some additional stability factors such as Δ, B_1, and B_2 are also considered in this thesis and their crossponding expressions are given below

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad (2.18)$$

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| < 1 \qquad (2.19)$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \qquad (2.20)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 > 0 \qquad (2.21)$$

For unconditional stability, the PA should satisfy the equation 2.18 and either equation 2.19, 2.20 or 2.21. In some conditions, even satisfying Rollet stability factor K ≥ 1 may not assure the unconditional stability throughout the frequency band form two port S-parameters [25]. Due to this reason, two more stability factors μ_{source} and μ_{load} are also taken into the account and their corresponding equations are expressed by 2.22 and 2.23, respectively. For unconditional stability either μ_{source} or μ_{load} should be greater than one.

$$\mu_{source} = \frac{1 - |S_{11}|^2}{|s_{22} - \Delta(S_{11}^*)| + |S_{21}S_{12}|} \geq 1 \qquad (2.22)$$

$$\mu_{load} = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta(S_{22}^*)| + |S_{21}S_{12}|} \geq 1 \qquad (2.23)$$

In order to avoid low frequency oscillations, the device stability is analysed from 200 MHz to 6 GHz. In this thesis to make an active device stable, a series resistor and inductor added in the gate bias path is used for low frequency stability. In addition to this, a parallel RC circuit to the series of transistor's gate is also used to ensure in and out of band stability. An amplifier stability factor K is calculated from two-port S-parameters and insured K is greater than one. In addition to K factor, the load stability circles also plotted on smith chart from 100 MHz to 6 GHz frequency band, which should be outside the unity circle.

2.5.3 Load-pull and source-pull

After determining the DC bias condition and analysing the stability of a PA, next goal is to take out the optimum source/load impedances at fundamental and harmonics by performing load/ source-pull simulation. PA theory presents that the gate/drain current and voltage waveforms at the intrinsic gate and drain terminals are critical to understand the behaviour of an amplifier, as well as for the design of IMN/OMN. However, in real world for designers, it is rarely possible to access intrinsic waveforms due to device parasitic and package. Therefore, load-pull or source-pull simulation at the die or package reference plane are performed for fundamental and harmonic impedances. Load and source impedances are randomly tuned at fixed bias point and input power level, while waiting for the device shows the wanted gain, efficiency, and output power. A basic diagram of load/source pull system is shown in Figure 2.17.

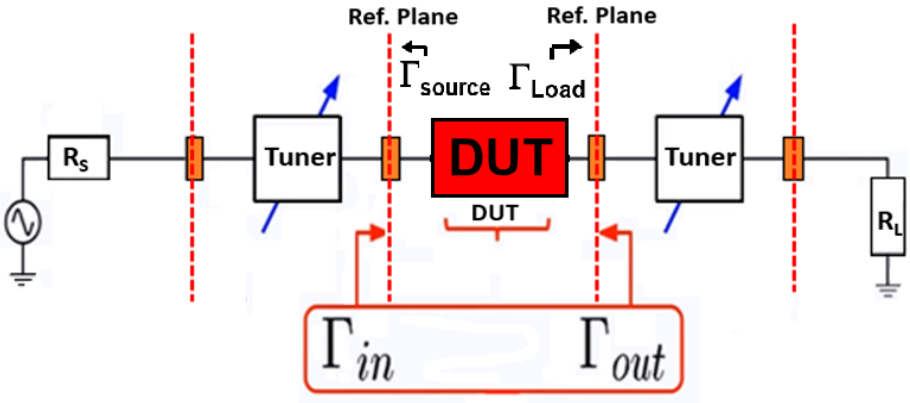


Figure 2.17: A simplified load and source-pull setup.

Load- and source-pull technique can be applied to large signal models in ADS simulation or real device by tuning the impedance at the input and output of the device with impedance tuner. Although , load-pull technique is extensively exploited in industry, but still it has some back draws such as without knowing the intrinsic waveforms difficult to find the linearity and drain voltage may exceed from the breakdown voltage.

2.5.4 Input matching requirements

The main purpose of the input matching network (IMN) is to transform the optimum source impedance to system level impedance (50 Ω) for maximum power transfer from source to the gate of a transistor. The input impedance offered to the active device mainly affects the gain of an amplifier. A proper impedance matching network can boost the gain of a power amplifier. As it is presented in recent study [26], that input matching network can enhance efficiency and output power of a Class-F PA. A study in [27] shows that IMN also affects other Figure-of-merits as well, such as linearity and efficiency.

IMN is demanding in PA for varying input impedance with frequency due to the device parasitic and package. At microwave frequencies, normally the input impedance of the active device has low values, if the power device is connected directly to the 50 W source (V_S) without any IMN, the available input voltage will be very small compare to applied source voltage, due to voltage division rules for 50 Ω impedance and very small value of R_{OPT}. As a result, a small amount of drain current will be produced and amplifier will produce a very small gain. Therefore, there should be an impedance matching network between source and the input impedance device, as shown in Figure 2.18.

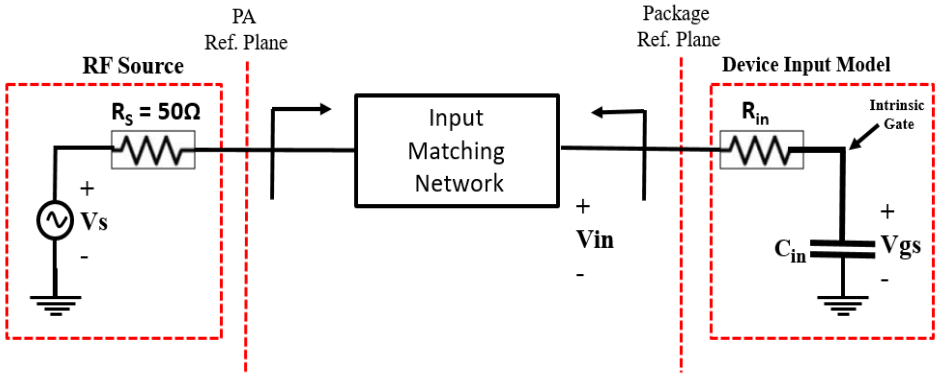


Figure 2.18: Input matching network between RF source and input side active device [4].

In a typical base-station power amplifier an input matching network is fabricated on a high frequency substrate. In the Figure 2.18, series resistance (Rin) and a capacitance (Cin) shows the input side of the model of an active device. From equation 2.24, input impedance of the device can be calculated

$$Z_{in} = R_{in} + \frac{1}{j2\pi f C_{in}} = R_{in} - jX_{in} \qquad (2.24)$$

After adding the stability circuit in the input matching network, the optimum input impedance of a transistor is determined again from a source-pull simulation. A complex conjugate of the small-signal impedance is taken from the simulated input reflection data S_{11}. In order to check the validity of small-signal gain of power amplifier S_{21} is compared with maximum available gain (MAG) of the device. For the perfect match condition, the transmission coefficient should be equal to the MAG at the design frequency and required bandwidth.

2.5.5 Multi-harmonics output matching network design

RF PA performance strongly influences entire wireless system's performance. Due to this reason, PA should be carefully designed for improving efficiency and linearity. Moreover, in order to achieve minimum output reflection losses and ensure power amplifier integration into the RF transmitter system output impedances should matched to 50 Ω. At the output of the device, matching network optimum impedance depends on the amplifier performance requirements. OMN of the power amplifier should transform the selected optimum output

impedance of the transistor to standard working level impedances. The optimum output impedance for optimum efficiency and output power can be selected from load-pull data of the active device.

For highly efficient PA such as Class-F amplifier, it requires the harmonics termination in the output-matching network; it could be either a short or an open circuit at the intrinsic drain terminal for proper harmonics termination. Figure 2.19 demonstrates a matching topology that can autonomously control the fundamental, second harmonic and third harmonic impedances. Harmonics control outside the third harmonic is hardly possible due to a complexity of output circuit of PA and reduced efficiency enhancement. For real to complex impedance transformation, usually two-section transformers are used in IMN/OMN matching networks. The transformer will resolve real impedance matching problem. However, for complex impedance matching additional network is required. The supplementary network topology for complex impedance matching is subject to requirements.

As soon as the optimum impedances at the package or intrinsic reference plane are selected from load-pull data, a corresponding matching network is designed to transform the optimum impedance to 50 Ω load. A detail theoretical explanation for single frequency matching based on lumped component is given in [28-29]. For OMN design, two key factors should be consider carefully, that can degrade the amplifier efficiency and output power. The first one is the qualify-factor (Q) of the lumped components; selected lumped component Q factor should not be too low. The other one is the impedance discrepancy that happens when the impedance transformation ratio is too high and the matching network is not capable to matching the two nodes perfectly.

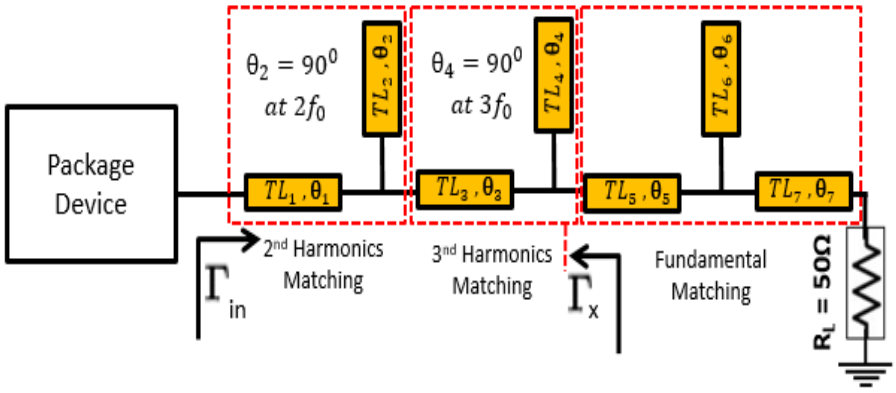


Figure 2.19: A multi-harmonic output-matching network with harmonics control.

2.6 Summary

In this chapter, power amplifier theory and its role in transmitter architecture is investigated. Key figure-of-merits of a power amplifier and various classes of operation are described. In addition to this, important factors for practical design considerations such as the parasitic effects device, effect of device package on load impedances, stability, input and output matching network designs are explained in detail.

Chapter 3

5 W Class-AB Power Amplifier

3.1 Introduction

In advanced mobile communication systems, growing demand of capability such as high speed video, low latency and low power consumption gives rise to extensive research and development efforts towards low cost circuit designs with the best trade-off between linearity and efficiency [30]-[32].

In this chapter, a Class-AB power amplifier (PA) design for 4G LTE 5 W pico-cell base station over the frequency range of 1.9-2.5 GHz with the aim to achieve optimum linearity from the Cree GaN HEMT device for whole frequency band is presented. Part of the work described in this chapter has been previously published in “A 5 Watt Class-AB power amplifier based on GaN HEMT for LTE communication band” [33]. We used nonlinear device model of the Cree transistor in Keysight Advanced Design System (ADS) software for large signal simulations. A two-tone load- and source-pull simulation is performed to extract optimum impedances for best efficiency and linearity. A prototype of proposed PA is implemented. After that, PA is characterized by two different communication signals (QAM-256 and LTE) for system level characterization throughout the frequency band.

3.2 Class-AB theory

Figure 3.1 shows the basic block diagram of a single-stage Class-AB amplifier. This design comprises on input and output matching networks as well as drain and gate bias networks. The gate bias level of a Class-AB is reduced from a Class-A amplifier bias point, therefore current waves start to clip (the detail theory of Class-AB PA is given in chapter 2 section 2.5). Usually, a Class-AB PA generates harmonics current clipping and nonlinear effects at the drain terminal of the active device.

Class-AB PA has higher drain efficiency and lower output power compared to Class-A PA. The use of harmonics control circuit is also very common in the output matching network for improving the PA drain efficiency (DE). In our proposed PA, harmonic terminations up to third harmonics are utilized for maximizing the DE. In L- and S-communication band, Class-AB PA can produce 60-70% DE. The ideal voltage and current waveforms of a typical Class-AB amplifier is shown in Figure 3.2. In the following sections, a practical design of 5 W Class-AB PA is discussed.

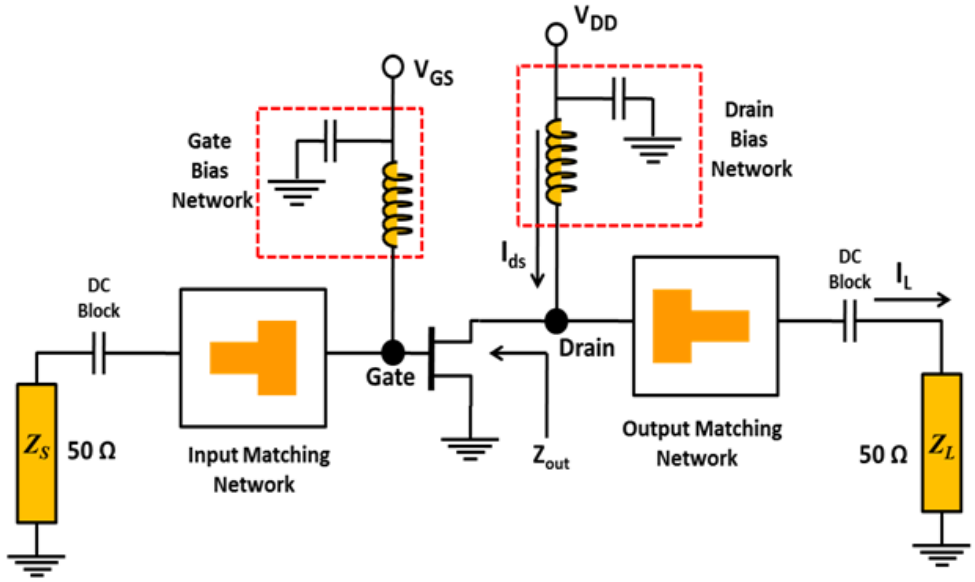


Figure 3.1: Block diagram of a single-stage Class-AB power amplifier circuit.

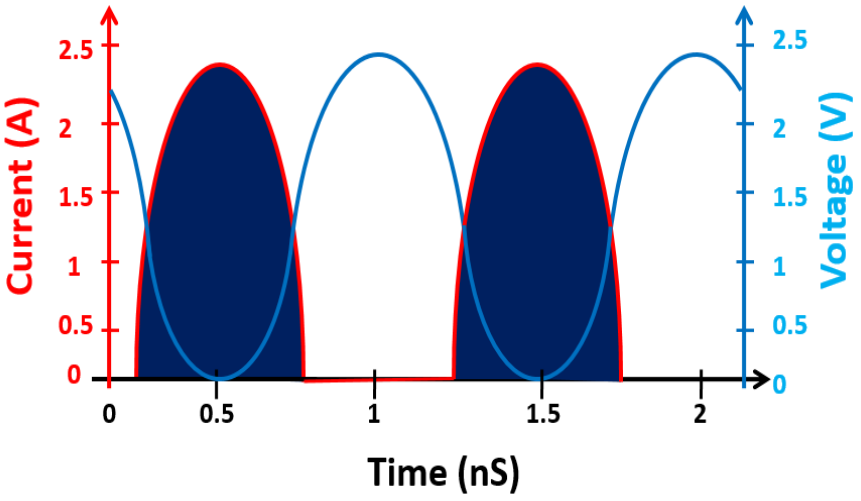


Figure 3.2: Voltage and current waveforms of an Ideal Class-AB PA.

3.3 Design specification

Design of a power amplifier starts with a set of specification and the selection of an appropriate active device. The specifications of targeted power amplifier are listed in Table 3.1. The requirements of high linearity, high drain efficiency, and wider bandwidth of the targeted PA design can be very challenging.

Table 3.1: Amplifiers specifications.

Parameters	**Value**
Operating frequency	1.9 - 2.5 GHz
Output power	5 W
Efficiency	60%
Linearity	30 dBc
Gain	15 dB

A 6 W GaN HEMT transistor (CGH40006P) from Cree is selected for this design. According to the datasheet of the elected device [34], the GaN HEMT transistor can work up to 6 GHz and is also capable to provide a output power of 9

W at V_{DD} = 28 V and I_{DQ} = 100 mA. Some of the important specifications of the selected device are listed in Table 3.2.

Table 3.2: Specifications of the selected active device.

Parameters	**Value**
Maximum Drain-Source Voltage ($V_{DS,max}$)	28 V
Maximum Gate-Source Voltage ($V_{GS,max}$)	$\pm$ 5 V
Maximum Forward Gate Current ($I_{GS,max}$)	2.5 mA
Maximum Forward Drain Current ($I_{DS,max}$)	0.75 A
Gate Threshold Voltage (V_{th} at V_{DS} = 10 V, I_D = 2.1 mA)	-3.8 V
Output Capacitance (C_{DS} at V_{DS} = 28V, F = 1 MHz)	1.1 pF
Output Power (P_{OUT}) at P_{IN} = 32 dBm V_{DD} = 28 V, I_{DQ} = 100 mA	9 W

3.4 Device stability analysis

After the selection of an appropriate device, most important step in the PA design is to make transistor stable. A stability test is performed on the selected active device. The device is unstable over a wide range of frequencies even at the designed frequency; therefore, the stabilization network is included in the input side of the active device.

There are several ways to verify the PA stability (details are given in chapter 2 section 2.5.4). In this design, one key parameter is considered to ensure stability. The considered parameter is stability factors (K), which can be calculated from two-port S-parameters. Equation 3.1 gives the value for Rollet stability factor 'K', which has to be greater than unity ($K > 1$) for unconditionally stable condition.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad (3.1)$$

A 47 Ω series resistor and 18 pH inductor added in the path of gate bias to ensure low frequency stability. Moreover, a parallel RC (R = 23 Ω and C = 4.7 pF) circuit to the series of transistor's gate is also used to ensure in and out of band stability of the power amplifier. An amplifier stability factor K is calculated from two-port S-parameters and insured K is greater than one. In addition to K factor, the load stability circles also plotted on smith chart from 100 MHz to 4 GHz frequency band, which are outside the unity circle as can be seen from Figure 3.3.

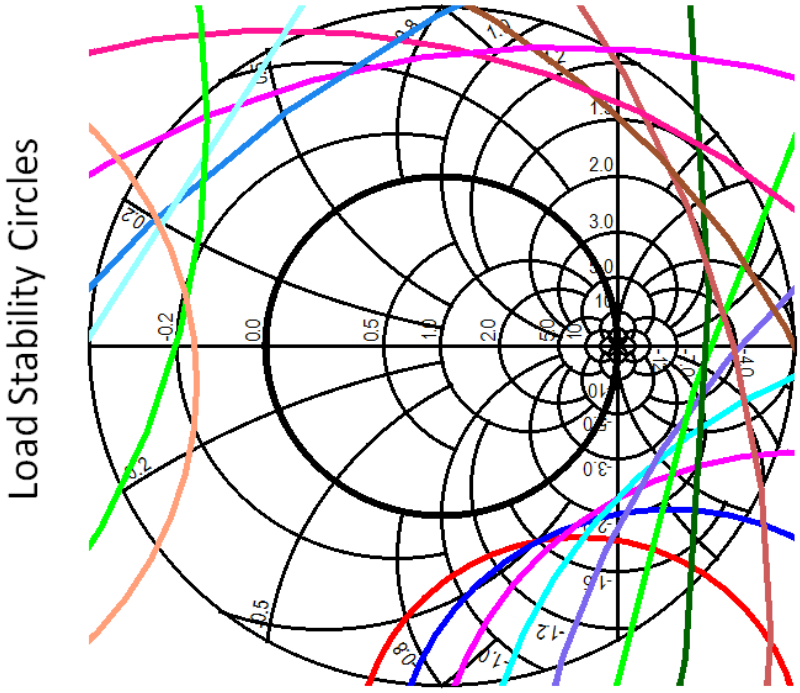


Figure 3.3: Load stability circle of the designed PA after adding stability circuit and optimization with industrial standard component.

3.5 Matching network design

RF PA performance strongly influences entire wireless system's performance. Due to this reason, PA must be properly designed to improve its drain efficiency and linearity. Moreover, in order to achieve minimum input and output reflection losses and ensure power amplifier integration into the RF transmitter system, its input and output impedances match to 50 Ω. In the output matching network optimum impedance depends on the amplifier performance requirements. Input

and output matching networks of the power amplifier should transform the input and output impedances of the transistor to standard working level impedances. The first step in the design of matching networks is to determine the optimum impedance of the selected active device for best performance.

3.5.1 Output matching network

In this section, an output-matching network design (OMN) for the frequency range of 1.85–2.55 GHz, with the aim to achieve optimum linearity and reasonable efficiency from a 6 W GaN device is presented. The main goal of this design is to making PA more linear for the whole frequency band and in particular at the designed frequency 2.3 GHz. There are two well-known approaches for achieving optimum linearity at the center frequency of a PA. Both the approaches are described below.

Determining the optimum output impedance (R_{opt}) for the best linearity from a selected active device using a two-tone load-pull technique. However, it is possible that R_{opt} could affect the output power and efficiency trade-off [35].

Determining the R_{opt} for maximum output power of the selected active device using a two-tone load-pull technique and localize the linear operating region of a PA (minimum IMD_3 point) through bias point optimization. This method requires proper optimization of bias point together with proper termination of out-of-band nonlinearities, particularly envelope and second harmonics [36].

In this design, the second approach is adopted to design a 5 W linear Class-AB PA by using the a 6 W GaN HEMT device provided by Cree for the frequency range of 1.9–2.5 GHz. In the high efficiency PA, OMN should delivered maximum power (P_{Max}) to the load (R_L), for maximum power delivery power matching and efficiency matching conditions are required. The efficiency and power matching condition are achieved, when power device is terminated with R_{opt} for maximum output power and R_{opt} for maximum efficiency. Similarly, optimum matching condition for best linearity is also required for linear amplifier. Therefore, the first step in OMN design is to determine optimum impedances of the selected active device for best efficiency, output power and linearity. The R_{opt} can be determined by using the load-pull technique.

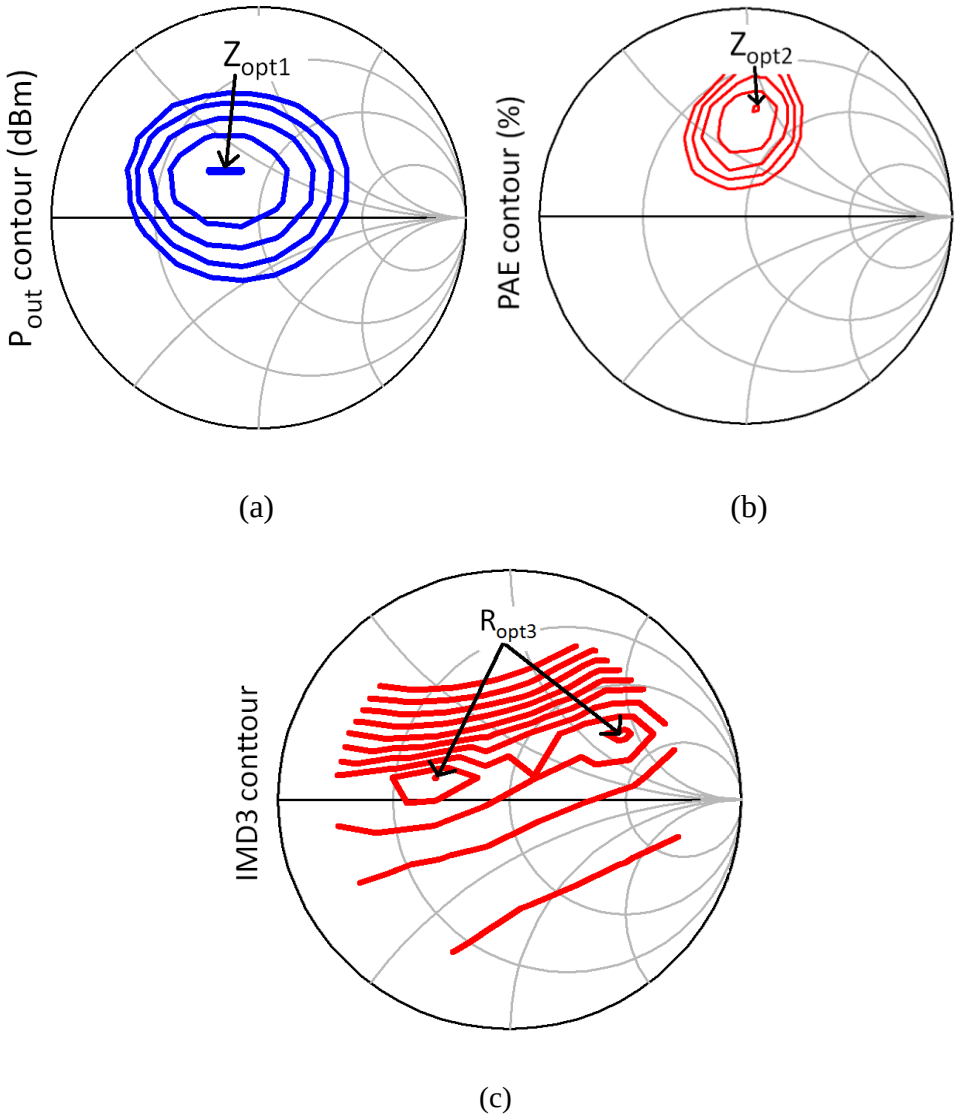


Figure 3.4: Simulated load-pull contours of the investigated 6 W GaN device (at V_{DS} = 28 V, V_{GS} = -3.1 V, I_{DS} = 35 mA-10% and Pin = 25 dBm): (a) output power (b) PAE and (c) IMD_3.

The load-pull can be performed either experimentally or through non-linear simulation. In the load-pull method impedance at the device package plane or intrinsic $I_{gen.plane}$ are tuned to get an optimum performance in terms of output power, efficiency and linearity. In this design, the optimum impedance of the selcted device is extracted through non-linear simulation using large-signal non-linear device model provided by Cree at the package plane. This non-linear simulation is low cost compared to the load-pull measurements and require less effort too. Nevertheless, model accuracy should be carefully assessed. After load-

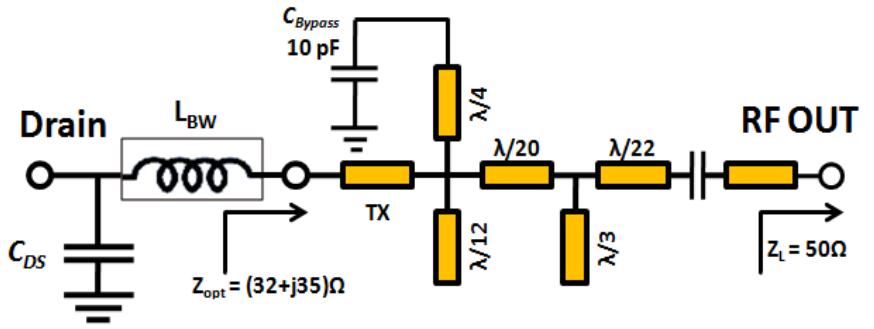
pull analysis, the OMN design is developed in the Keysight Advanced Design System (ADS) and simulation for OMN is carried out for the desired frequency band with 50 Ω reference impedance.

In the first step, the source-pull harmonic balances (HB) simulations are performed for optimum source impedance at the fundamental frequency. The extracted optimum source impedance is Z_S = 10+j*10.9 Ω at the bias point (V_{DS} = 28V, V_{GS} = -3.1V) with a drain current of 35 mA at 2.3 GHz. Then, the load-pull simulations are performed for the optimum load impedances of output power and efficiency with the same bias point at fundamental frequency (data is given in appendix A). The power and PAE elliptical output contours in a step of 0.5 dB and 4% are shown in Figure 3.4 (a) and (b), respectively. The power contours delivered an optimum output power of 36 dBm at an output impedance of Zopt1 = 28.2 + j*39.2 Ω and the PAE contours delivered an optimum efficiency of 70% at an output impedance of Zopt2 = 30.6 + j*45.4 Ω. However, the location of optimum output power and optimum PAE is slightly away on smith chart. On the other hand, there are two optimum impedances values for best IMD_3 Zopt3 = 35.8 + j*44.5 Ω and Zopt3 = 24 + j*12 Ω, both are faraway form the optimum impedances locations of power and PAE, as it can be seen form Figure 3.4. The maximum achievable efficiency is 70% and the output power is of 36 dBm. An evaluation board has been designed for the impedances where the efficiency is around 60% and output power is 36 dBm at 1 dB compression point. The selected optimum output impedance is Z_{opti} = 32+35*j Ω for optimum linearity and efficiency.

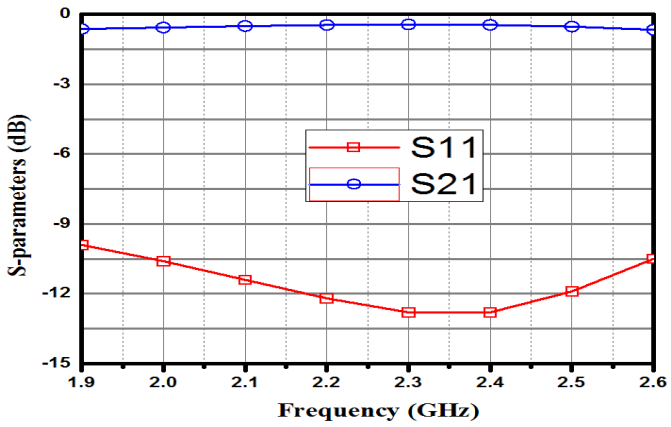
By having R_{opt} value of the selected device, the OMN can be designed to match 50 Ω load. Output and input impedance networks can be designed analytically or graphically using smith chart utilities available in ADS. The selection of the particularly technology depends on the system requirement for example frequency of operation, bandwidth, size and the realization resolution. In wireless communication system in L- and S-band matching networks, normally consist of lumped and distributed elements. The particular requirements of the matching network depend on the mode of operation of power amplifier. For example, Class-AB required multi-harmonic terminations at the output matching network, which provides optimum matching at the fundamental and short circuit at higher order harmonics. Moreover, the bandwidth requirements of the matching network depend upon the system requirements. For instance, an amplifier to be used for LTE application, it should be mandatory for OMN to have 100 MHz

bandwidth and hence the matching networks should provide the respective bandwidth [24].

The Figure 3.5 (a) shows the used output matching network topology and reflection/insertion losses for the proposed PA. In this adopted topology short circuit for second and third harmonics at the device extrinsic drain terminal point is achieved by using a short circuit $\lambda/4$ stub and a $\lambda/12$ open stub, respectively. A T-section matching network is used to provide fundamental frequency matching as shown in Figure 3.5. After the fundamental matching is achieved, a $\lambda/4$ transmission line used for second harmonics short will also be used as bias line. A tuneable line is inserted between the short and the open stubs for compensating the parasitic reactance, and also to achieve a good short circuit for the second and third harmonics.



(a)

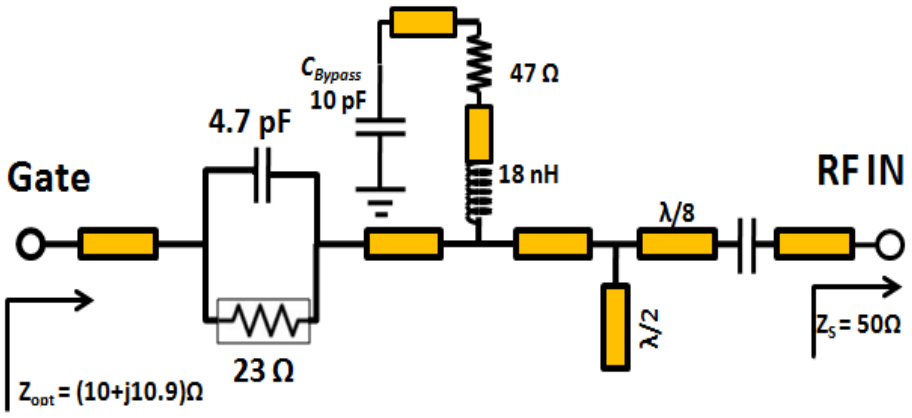


(b)

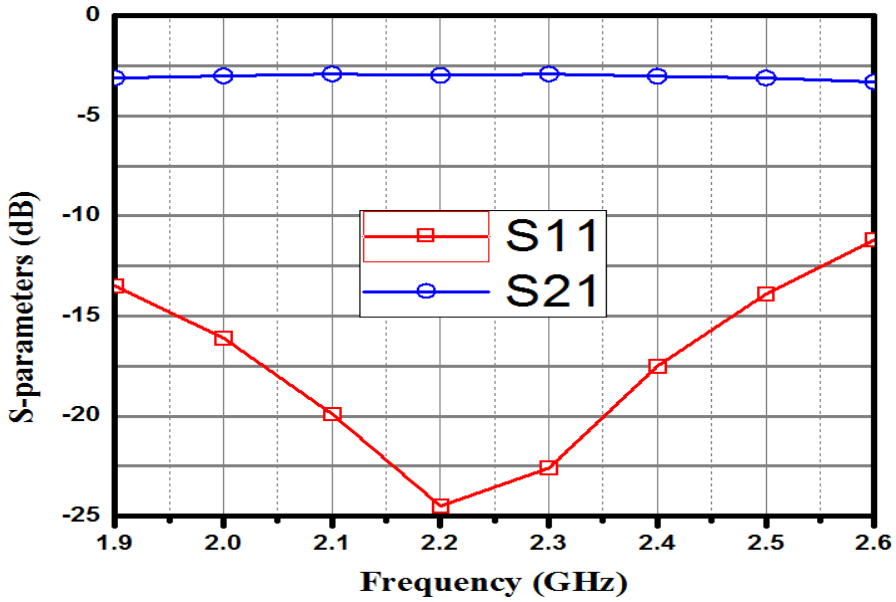
Figure 3.5: Output matching network: (a) schematic and (b) simulated transmission coefficient S_{21} and input reflection coefficient S_{11}.

3.5.2 Input matching network

The main purpose of input matching network (IMN) is to transform the optimum source impedance to system level impedance 50 Ω for maximum power transfer from source to the gate of the transistor. Input matching network can also be used to boost the overall gain of the power amplifier. After adding the stability circuit in the input matching network, the optimum input impedance of transistors is determined again from a source-pull simulation. A complex conjugate of the small-signal impedance is taken from the simulated input reflection data S_{11}. In order to check the validity of a small-signal gain of the PA (S_{21}) is compared with maximum available gain (MAG) of the device. For the perfect match condition, the transmission coefficient S_{21} should be equal to the MAG at the design frequency and required bandwidth. Figure 3.6 (b) shows the simulated S_{21} of the input matching network for desired bandwidth. The next step is to design the input matching network to transform the input of Zin = 10+j*10 Ω to 50 Ω. The input matching network has been designed using an L-section low pass matching. The schematic and the small-signal response of the designed input matching network is shown in Figure 3.6 (a). This matching network is then implemented with TLs, the same as outlined in the output network. The result in Figure 3.6 (b) of final input matching network shows satisfactory reflection and insertion losses throughout the designed band.



(a)



(b)

Figure 3.6: Input matching network: (a) topology and (b) simulated transmission coefficient S_{21} and input reflection coefficient S_{11}.

3.5.3 Bias point optimization

In bias point optimization, the main goal is to extract sweet spots for optimum carrier to intermodulation ratio (C/I) by performing extensive circuit simulations in ADS at different gate biasing. The sweet points are the particular area of interest of the active device operation, where it shows higher intermodulation distortion (IMD_3) compare to the other biased points. C/I ratio is very well known method to determine the non-linear behaviour of the device and can be calculated by following equation [37]

$$\frac{C}{I} \approx \frac{P_{out}}{P_{IMD}} \qquad (3.2)$$

For this purpose, the proposed PA is biased at four different bias levels and excited with a two tone input signal at f_1 GHz and f_2 GHz, with same input power sweep from 0 to 25 dBm with the increment of 1 dB . The selected operating frequencies are f_1 = 2.25 GHz and f_2 = 2.35 GHz with 10 MHz of bandwidth. The optimum C/I ratio is achieved from the PA when the device was biased with a drain voltage (V_{DS}) of 28 V and a gate voltage (V_{GS}) of -3.1V. Figure 3.7 shows the C/I ratios for all the bias points from 0 to 25 dBm input power.

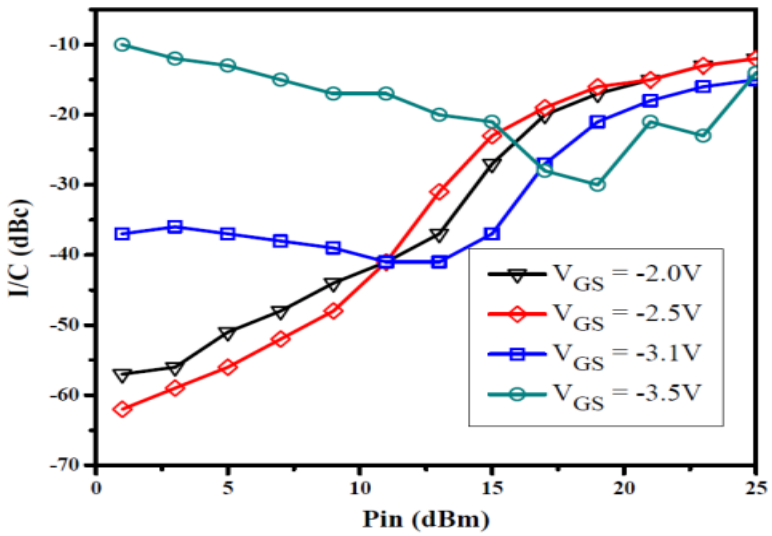
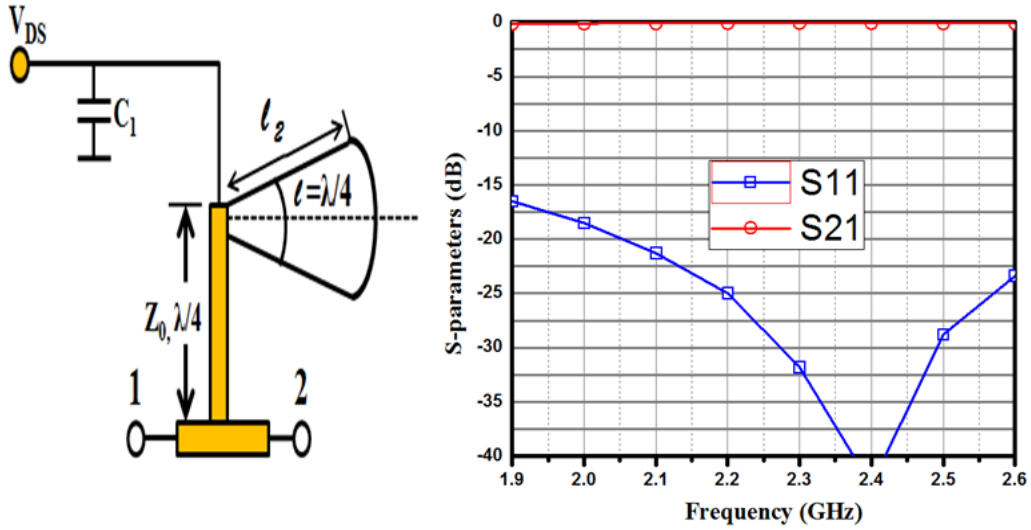


Figure 3.7: Simulated carrier to intermodulation ratio versus input power level for V_{GS} = -3.5 V, V_{GS} = -3.1 V, V_{GS} = -2.5 V and V_{GS} = -2 V. The results are obtained with a drain voltage of 28 V.

3.6 Bias network design

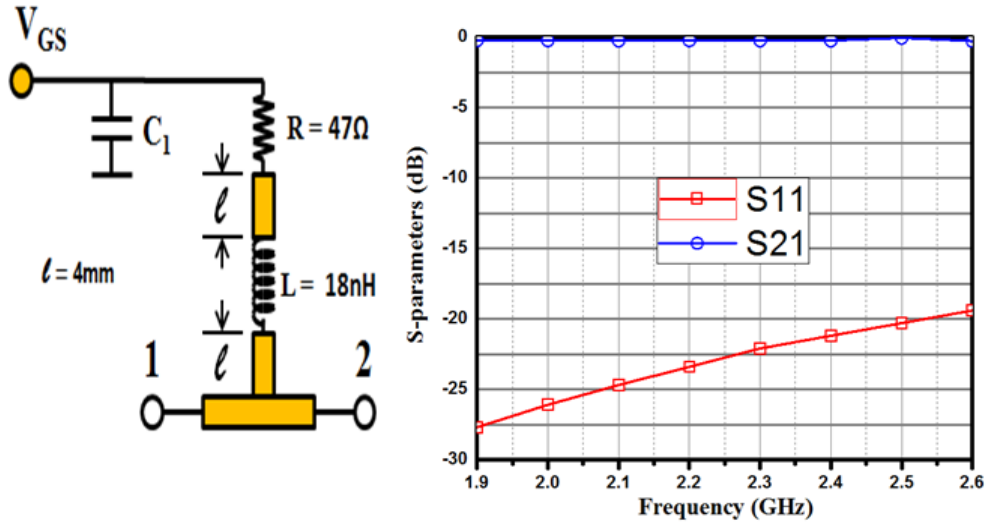
Biasing networks are used to supply the gate and drain voltages to the active device for maintaining the drain current at predefined voltages. Both the biasing circuit should be capable block the RF frequency though the frequency band and for lower frequency by pass capacitors are used to provide short circuit. The most commonly used biasing network is based on a λ/4 transmission line at the designed frequency with 50 Ω characteristics impedance for the both drain and gate biasing circuits of RF power amplifier. A short circuit λ/4 transmission line transforms the short into open at RF frequency.

For our proposed PA, in order to enhance the bandwidth of biasing network, in the drain biasing a radial stub is used at the end of λ/4 transmission line. The input and output reflection of the drain biasing network from 1.9-2.6 GHz are depicted in Figure 3.8. On the other side, in the gate biasing network instead of using a conventional λ /4 line a series resistor and inductor are used in the gate biasing network for reducing the gate current and absorb the noise from the power supply. Figure 3.9 is showing the adopted topology and the corresponding S-parameters over the desired bandwidth. We also used a set of bypass capacitors [1 pF, 22 pF, 100 pf and 4.7 μF] to effectively terminate the envelope to short circuit [38-40].



(a) (b)

Figure 3.8: Radial-stub drain bias network: (a) topology (b) simulated transmission coefficient (S_{21}) and input reflection coefficient (S_{11}).



(a) (b)

Figure 3.9: Gate bias network: (a) topology (R = 47 Ω, L = 18 nH and l = 5 mm) (b) simulated transmission coefficient (S_{21}) and input reflection coefficient (S_{11}).

3.7 Final design

The final schematic of the 2.3 GHz Class-AB PA has been assembled in simulator by using all the sub-circuits described in the previous sections. A microwave substrate in the design environment of ADS has been chosen with laminate FR4 of thickness 0.8 mm. The synthesized biasing and matching networks are implemented using transmission lines (TLs). At 2.3 GHz, on this FR4 substrate, a quarter-wavelength translates to approximately 17.52 mm length and width 1.43 mm impedance microstrip line.

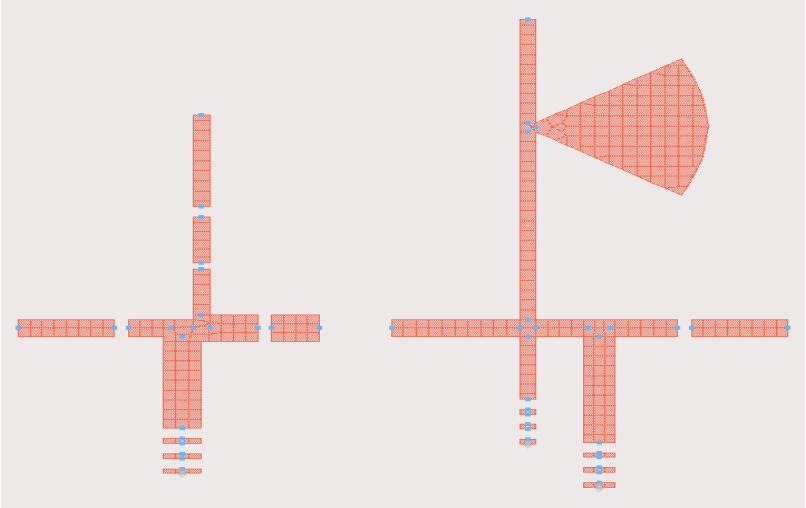


Figure 3.10: EM simulation of proposed PA in ADS simulator.

On final schematic of PA, various small- and large-signal simulations have been performed to optimize the input and output return losses, small-signal gain, bandwidth and stability factor. In order to optimize the large-signal performance extensive harmonic balance simulation is used. In the last step of simulation and for also verification purpose, an electromagnetic simulation has been performed for distributed network such as biasing and matching networks, as shown in Figure 3.10. A good agreement in circuit and electromagnetic simulation has been observed for the whole band. Figure 3.11 shows the final dimension of the transmission lines of the proposed PA. The final step in Class-AB PA design is to realized the prototype circuit using the specified material and components. The fabricated amplifier is based on hybrid technology as shown in Figure 3.12. Lumped components and device has been soldered on printed circuit board (PCB) carefully in order to minimized fabrication errors.

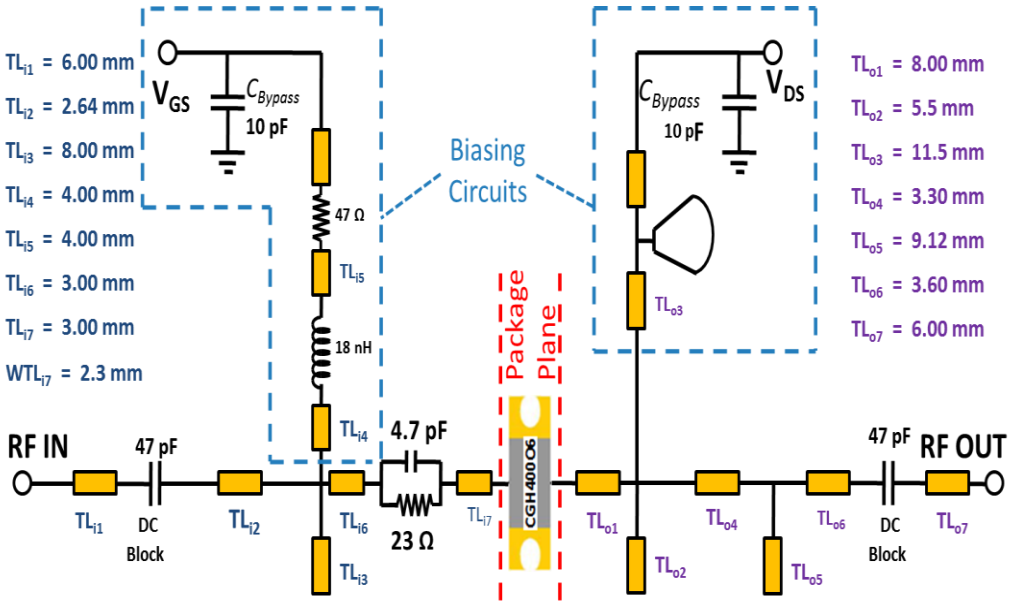


Figure 3.11: Schematic circuit of 2.3 GHz Class-AB Power Amplifier.

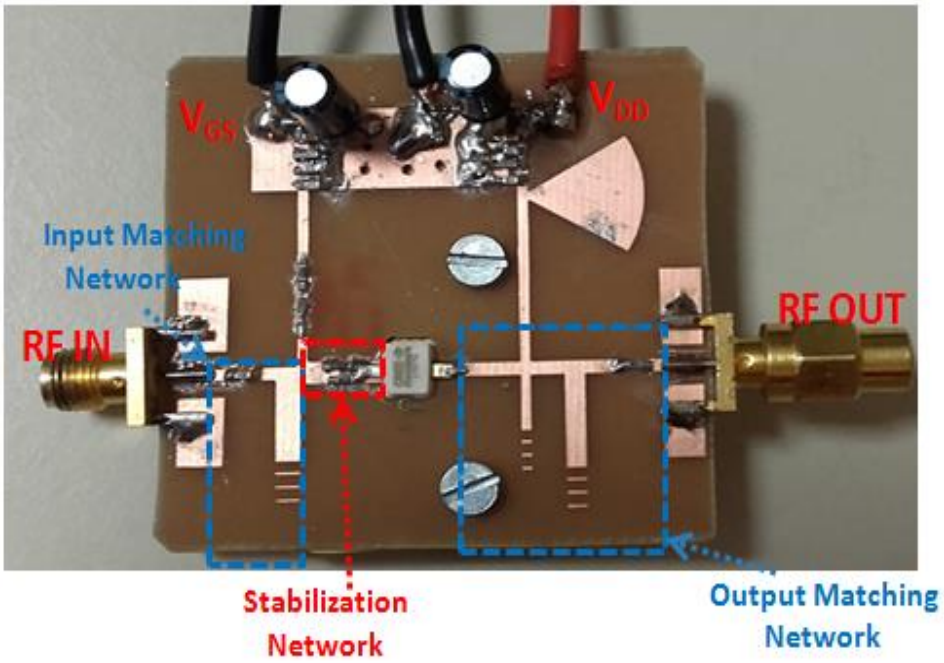


Figure 3.12: Photo of realized 5 W Class-AB Power Amplifier.

3.8 Performance evaluation

This section will report the simulated and measured results of the final design of power amplifier. The first of which are the small-signal S-parameters swept from 1.8 to 2.8 GHz shown in Figure 3.13.

3.8.1 Small-signal testing

The small signal gain and the return loss of the realized power amplifier are measured using a Vector Network Analyzer (VNA), calibrated using a LRM technique [42]. Measurement results are compared with simulated results over the frequency range of 1.8 to 2.8 GHz at V_{DS} = 28 V and I_{DS} = 35 mA. As it can be seen from Figure 3.13, the measured and simulated results show good agreement throughout the band of interest. However, fabrication errors during the implementation such as changes of the width and length of the transmission line lead to the small frequency shift. This is mainly due to inaccuracies in the modelling and fabrication.

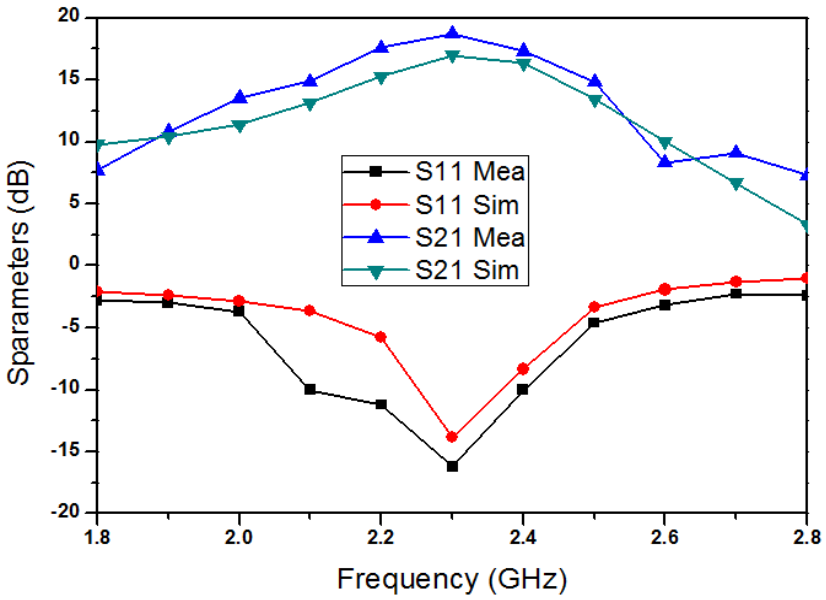


Figure 3.13: Measured and simulated S-parameters of 5 W Class-AB Power Amplifier (S_{11} and S_{21}, at a bias point of V_{GS} = -3.1 V, V_{DS}= 28 V and I_{DS} = 35 mA).

3.8.2 Single-tone power sweep

Characterizations of Power amplifier in terms of efficiency, gain and output power are also carried out with single-tone input signals at different input power levels. The measurements setup for power characterization includes the Vector Network Analyzer (VNA), power generator, power supplies and power meter. Before single-tone measurements, the measurement bench has been fully calibrated.

Figure 3.14 compared the simulated and measured results of 5 W Class-AB power amplifier at 2.3 GHz, when active device is biased at V_{DS} = 28 V and I_{DS} = 35 mA. The input power is swept from 10 dBm to 25 dBm in 1 dB increments. The measured results show saturated PAE and PAE at 1 dB compression point are approximately 68% and 53.4%, respectively. The measured PAE is slightly higher than the simulated PAE because of some inaccuracies of the passive models used in this simulation. The linear transconductance gain is approximately 18.9 dB and maximum output power is 36.9 dB at 2.3 GHz.

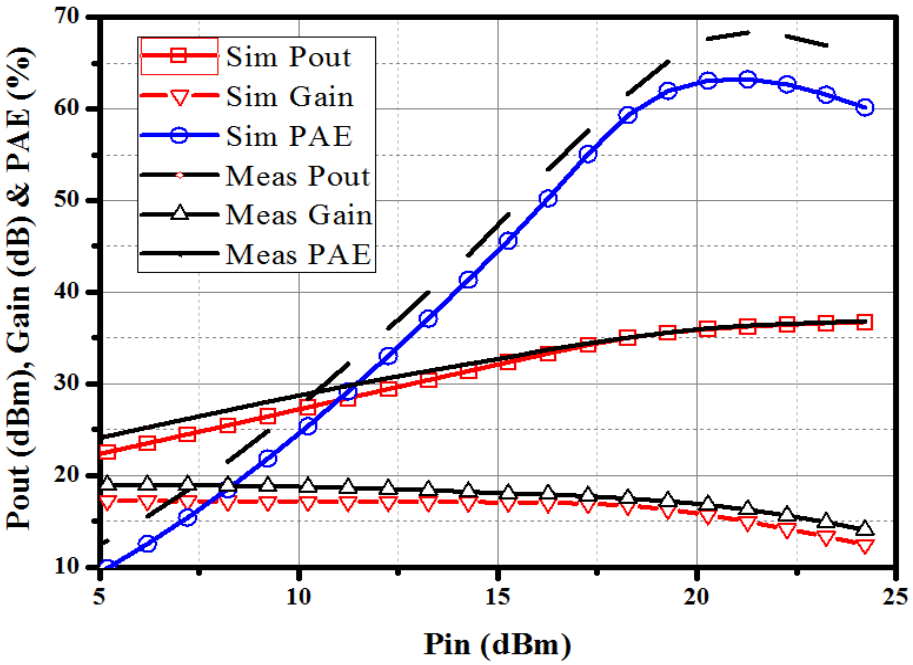


Figure 3.14: Measured and simulated gain, PAE and Pout at the V_{DS} = 28 V and I_{DS} = 35 mA for 2.3 GHz.

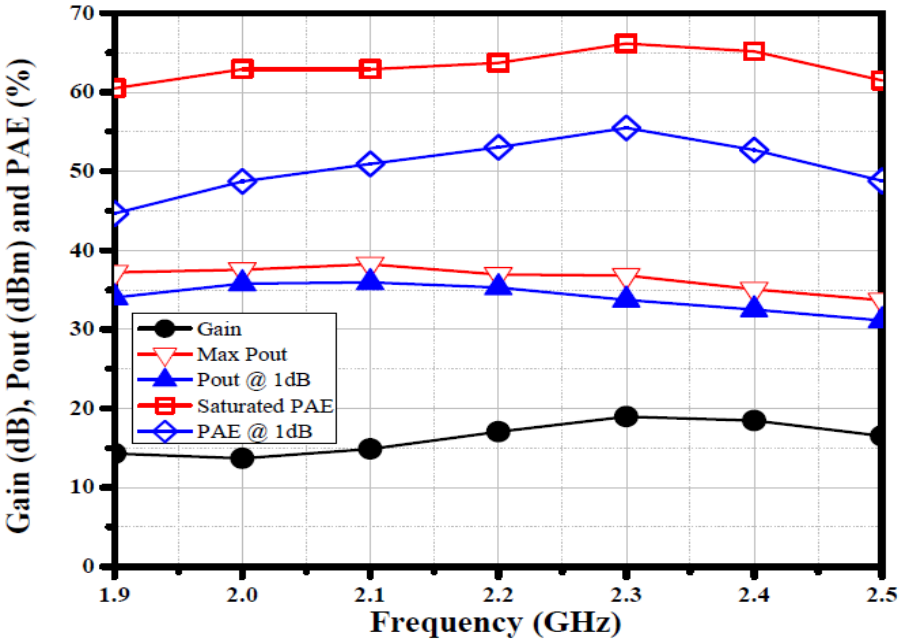


Figure 3.15: Measured gain, PAE, and Pout versus frequency at the V_{DS} = 28 V and I_{DS} = 35 mA.

To evaluate the bandwidth response of the proposed PA, a single-tone testing is performed from 1.9 to 2.5 GHz. Measured parameters such power gain, PAE, gain and output power at saturation and 1 dB compression point of the Class-AB PA are plotted in Figure 3.15, ranges from 1.8 to 2.5 GHz. Measured data show a peak PAE of 68% at 2.3 GHz with an output power of 35.4 dBm and a power gain of 18.4 dB. Moreover, the PA maintain a saturated PAE higher than 60% and higher than 44% at 1dB compression point over the whole frequency band. Furthermore, PA also maintains a power gain higher than 13 dB and an average output power of 36.5 dBm over the whole frequency band.

The proposed PA is a potential candidate for a RF power amplifier of an envelope tracking systems, its performance in terms of efficiency and gain is recorded at different drain bias voltages. To this purpose drain bias is swept from 20 to 32 V and corresponding gain and efficiency are recorded. The PA is fed with 2.3 GHz input signal and gate bias voltage is fixed at -3.1 V. The simulated gain and PAE of the proposed of the power amplifier over a wide range of output power levels at four different bias levels are shown in Figure 3.16. As can be seen from the results, the PA shows excellent performance for an envelope tracking systems in terms of gain and PAE variation with different drain bias voltages.

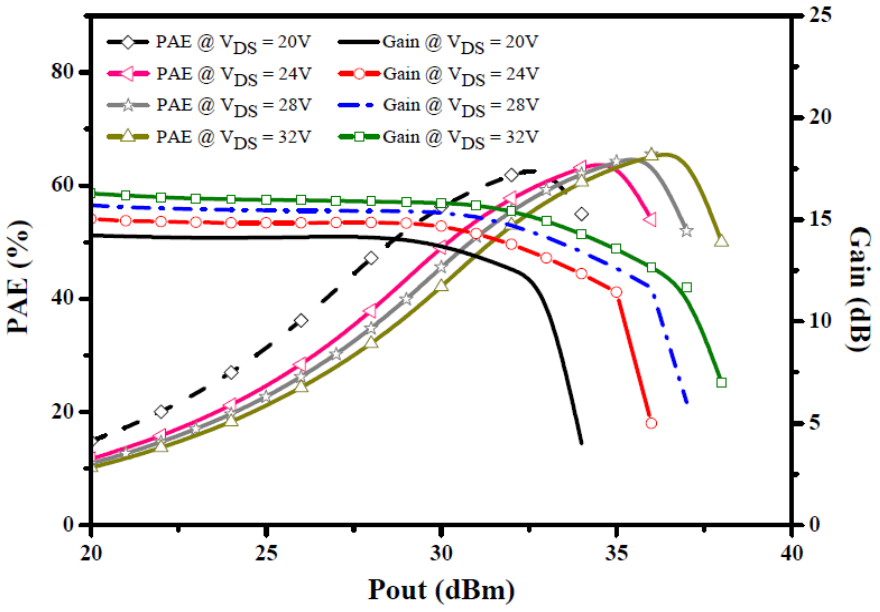


Figure 3.16: The PAE and gain of the proposed PA at different drain bias voltages (V_{DS} = 20 V, V_{DS} = 24 V, V_{DS} = 28 V, and V_{DS} = 32 V).

3.8.3 Two-tone test

The most commonly used method to determine the nonlinear behaviour of a PA is Carrier-to-Intermodulation ratio (C/I). C/I can be define as, it is the measure ratio between the desired output power and IMD_3 output power. The quantity can be calculated by given equation below [40]

$$C/I \triangleq \frac{P_{out}}{P_{IMD}} \tag{3.3}$$

In this work equation (3.3) is used to calculated the C/I ratio. Moreover, a two-tone harmonic balance simulation is performed to record the two-tone IMD_3 measurements reported. During two-tone measurement two closely spaced input tones with equal amplitudes were applied to the proposed power amplifier at 2.25 GHz and 2.35 GHz, respectively, where 10 MHz is the frequency spacing between the two-tones. The third-order distortion between fundamental component and lower third order component (IMD_3_left) and between upper fundamental component and upper third order component (IMD_3_right) versus Pin are shown in Figure 3.17. It can be observed, that the IMD_3 increases with the input power. The IMD_3 is worse than -20 dB for input power levels above Pin =

25 dBm. Please observe that the C/I no longer meets the 30 dBc specification from approximately 18 dBm to 25 dBm input power, when PA operates in deep compression region.

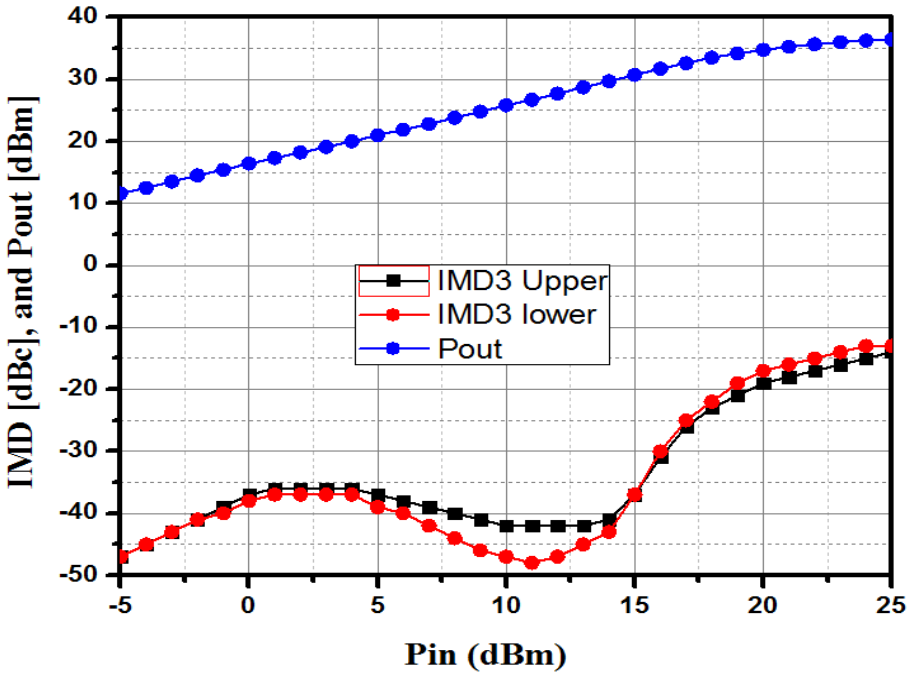


Figure 3.17: Simulated output spectrum, when the PA is excited with a two-tone input signal (16 dBm each of them) at a center frequency of 2.3 GHz and spacing of 10 MHz.

Table 3.3: Lower and upper carrier to intermodulation ratios for different frequency spacing at 2.3 GHz. The simulations are made for two-tone input signal of 16 dBm power each.

Δf	$(C/I)_L$	$(C/I)_U$
2.5 MHz	-34.5 dBc	-32.8 dBc
5 MHz	-33.4 dBc	-32.2 dBc
10 MHz	-33.1 dBc	-31.2 dBc
15 MHz	-32.9 dBc	-30.7 dBc
20 MHz	-32.2 dBc	-30.1 dBc

The C/I ratio is measured using a two-tone input signal. The two-tones have equal amplitude and they are centred around 2.3 GHz. The C/I is also calculated for different frequency spacing (f = f2 - f1) between the two-tones (2.5 MHz, 5 MHz, 10 MHz, 15 MHz, 20 MHz). Each of the tones has a power of Pin[f1] = Pin[f2] = 16 dB . The $(C/I)_L$ and $(C/I)_U$ for different frequency spacing are shown in Table 3.3 demonstrating a good performance even though the device is not operating in its linear region. It is recorded that for a spacing of 5 MHz the power amplifier demonstrates a carrier to intermodulation ratio better than 25 dBc. The asymmetry between the lower and upper carrier to intermodulation ratios is attributed to the measurement setup. To know the bandwidth response of proposed PA, single-tone testing also performed from 1.9 to 2.5 GHz. The measured parameters such power gain, PAE, gain and output power at saturation and 1 dB compression point of the Class-AB PA are plotted in Figure 3.15, ranges from 1.8 to 2.5 GHz. The measured data showed a peak PAE of 68% is revealed at 2.3 GHz with an output power of 35.4 dBm and a power gain of 18.4 dB. Moreover, PA maintains a saturated PAE higher than 60% and higher than 44% at 1dB compression point over the whole frequency band. Furthermore, PA also maintains a power gain higher than 13 dB an average output power of 36.5 dBm over the whole frequency band.

3.8.4 Modulated signal characterization

The performance of the power amplifier under real communication signals has also been measured over the proposed frequency band. A fully calibrated frequency domain measurement setup is used to measure the Adjacent Channel Power Ratio (ACPR) of the implemented power amplifier. Figure 3.18 shows the measurement setup used to measure the Adjacent Channel Power Ratio (ACPR) with an input LTE signal and QAM-256 communication signal. Measurement setup compromised on power supplies, spectrum analyzer, attenuator, driver amplifier and signal generator. Power amplifiers are affected by amplitude and phase distortion, caused by nonlinear active device behaviors and thermal memory effects. For increasing the PA linearity and to ensure the compliance with the LTE standard, we introduce a digital predistorter (DPD) using a Matlab code.

Figure 3.18 shows the measured output spectrum of the fabricated power amplifier at 2.3 GHz for an input QAM-256 signal with an input power of 17 dBm and bandwidth of 7 MHz (PAPR 7.4 dB). The lower adjacent channel power ratio (ACPRL) is defined as the ratio between the total output power measured in the fundamental zone around the carrier, and the total power in the lower adjacent-

channel power (Pout_L). The same applies for the upper ACPR (ACPRU), which is defined as the ratio of the Pout and the upper adjacent-channel power (Pout_U). It can be noted that the values of the ACPRL and ACPRU are higher than 40 dBc for an input power of 17 dBm. The PA ACPRs are also measured with a predistorterd input signal. It shows slight improvement in ACPRs compared to the case without digital predistorterd signal.

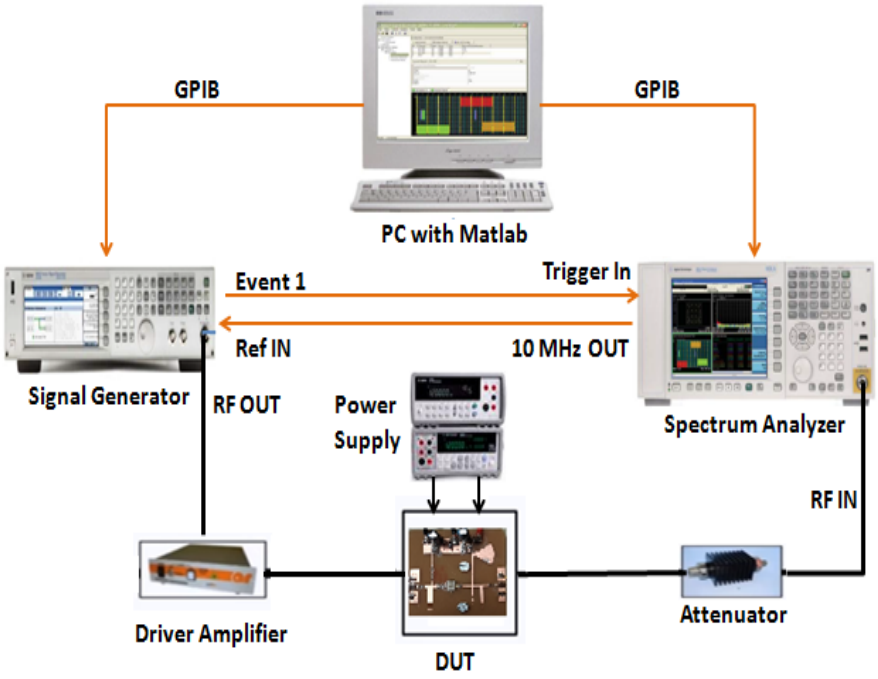


Figure 3.18: Linearity characterization setup.

Figure 3.19 shows the measured output spectrum of the fabricated power amplifier for an input LTE signal with an input power of 17 dBm and bandwidth of 15 MHz at two different frequencies. Adjacent channel leakage measurements (ACLR) where conducted using a LTE signal with a bandwidth of 15 MHz. At an output power of approx. 30 dBm, ACPRs of – 30 dBc, and – 31 dBc are measured at 2.1 GHz, and 2.4 GHz, respectively. The ACPR measurement results of the proposed PA closely follow the two-tone test results. We see an increase in the ACPR at an output power of about 17 dBm, which is consistent with the sudden raise in IMD_3 at an input power of 17 dBm. The PA ACPRs are also measured with a predistorterd input signal. It shows good improvement in ACPRs compared to without digital predistorterd signal. As it can be observed in Figure 3.20, the

values of lower- and upper-sideband ACPRs are higher than 40 dB for an input power of 17 dBm, which is close to 1-dB compression point.

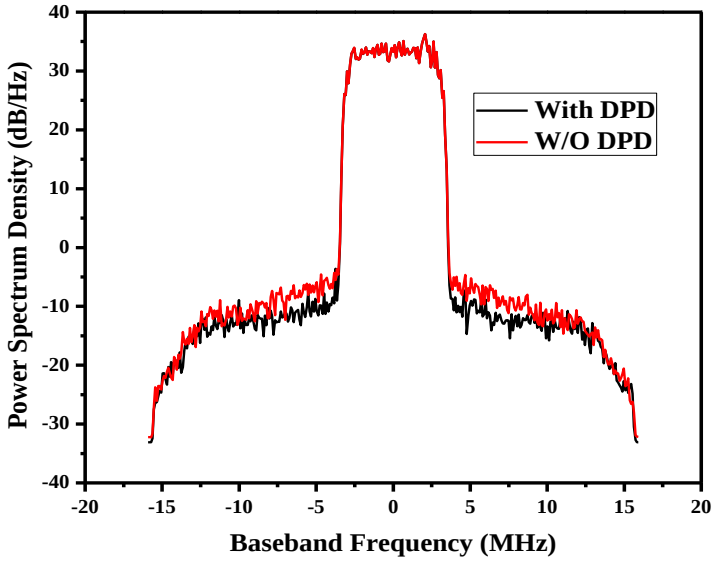
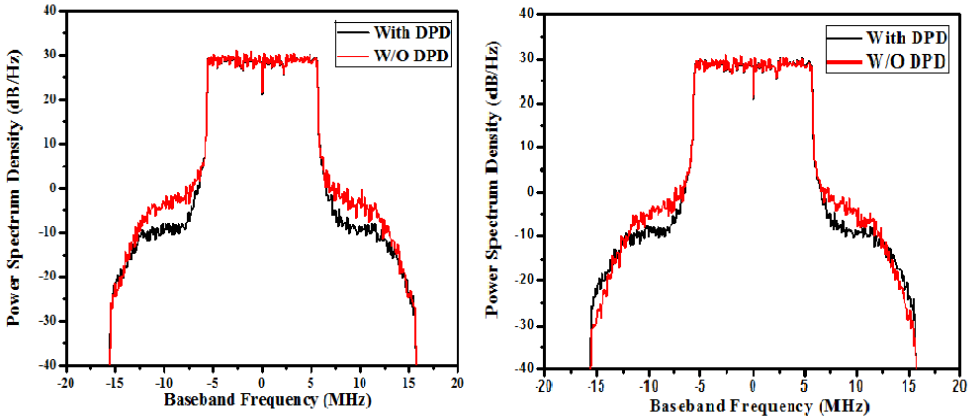


Figure 3.19: Output spectrum of the power amplifier when excited with a QAM-256 at 2.3 GHz.



(a) (b)

Figure 3.20: Linearity of proposed PA with LTE communications signal (a) 2.1 GHz and (b) 2.4 GHz.

Finally, a comparison between the recently published broadband PAs and state-of-the-art Class-AB PA made, as shown in Table 3.4. From the best of authors' knowledge, the simulated and measured bandwidth with high efficiency of proposed broadband Class-AB PA are better than the other published results with respect to Class-AB power amplifiers.

Table 3.4: Performance compression with state-of-the power amplifier.

RF Devices	Freq. (GHz)	Power (dBm)	Gain (dB)	PAE/DE (%)	Ref.
Si MOSFET	1.3	50	20	47/--	[41]
SiGe HBT	1.8	28	13	51/--	[42]
Si- LDMOS	1.2	50	40	20/--	[43]
SiC MOSFET	1-2	47	10	25/--	[44]
GaN HEMT	1.25	46	12	--/50	[45]
GaN HEMT	2.11- 2.17	37	12.6	--/52.8	[46]
Si LDMOS	2.69	36	13.6	--/44	[47]
GaN HEMT	1.9-2.5	36.5	19	68/--	This work

3.9 Summary

A 5 W Class-AB power amplifier circuit is designed and implemented using a GaN HEMT (CGH40006P) active device from Cree Inc for LTE communication band. Before implementation, extensive simulations were performed in ADS using accurate device model and component's model to achieve required linearity and efficiency. Load-pull techniques with bias optimization method were utilized to determine the optimal load impedance and best biasing points for optimum C/I ratio. The input and output matching networks for best performance were optimized and electromagnetic simulation was performed with the Momentum simulator. To efficiently deal with the parasitics of the packaged device and perform harmonic control up to the third order, a multi-stage transmission-line is used. The simulation and measurement results verify that the Class-AB amplifier is suitable for a high-efficiency linear PA over a frequency range for 1.9-2.5 GHz. These results indicate the potential application of the Class-AB architecture for envelop tracking system.

Chapter 4

Ultra-wideband Class-F Power Amplifier

4.1 Introduction

In a modern wireless communication system, growing demand of higher data rate and wider bandwidth keep pushing the researcher to develop a new system that can fulfill the communication requirement. Besides this, if we look from the PA perspective, the base-station transceivers require power amplifiers with increasingly high efficiency, low operational cost and wider bandwidth. The challenges of meeting all these requirements simultaneously motivate researchers to optimize PA designs and introduce innovative circuit topologies. A small improvement in the efficiency of a PA leads to lower power consumption, smaller battery size, relaxed cooling requirements and also lower operating cost of the base-station. In order to overcome efficiency enhancement challenges, two mostly widely adopted solutions are Class-F and -E power amplifiers (PA). However, both of these topologies are facing internal bandwidth limitation which is not still fully addressed [48-50].

It has been presented in [51] at least in theory; it is possible to achieve 100% drain efficiency from a Class-F PA by using infinite harmonics termination in the OMN to shape the intrinsic drain voltage and current waveforms. However, in practice it is unrealistic to realize a Class-F power amplifier with infinite number of harmonic terminations and PA efficiency degrade from 100%, due to limited

number of harmonics terminations and non-idealities of the components such as transistor parasitic.

In this chapter, a successful design and implementation of highly efficient broadband Class-F power amplifier (PA) is discussed using a commercial GaN HEMT transistor for the frequency range of 1.1-2.1 GHz. The impedance tuning of the second, third, and fourth harmonics at the drain terminal of the transistor is crucial to achieve broadband performance. The effect of harmonics terminations on PA bandwidth up to fourth harmonics is emphasized in this design. A microstrip hybrid circuit technology with 10 W packaged GaN HEMT is used for implementing proposed design. The realized power amplifier showed 13-15 dB gain and 60-73% of drain efficiency in the 1.1-2.1 GHz frequency band. For the same frequency range, the amplifier demonstrates a maximum output power between 39.5 and 41.5 dBm. Part of the work described in this chapter has been previously published in "GaN HEMT based Class-F Power Amplifier with Broad Bandwidth and High Efficiency" [52].

4.2 Class-F theory

Typically, Class-F power amplifier is biased in Class-B mode and active device is precisely loaded with harmonics terminations at fundamental and harmonic frequencies. Due to the switching nature of the active device, harmonics will be generated at the intrinsic drain terminal of the active transistor. Therefore, a harmonics control network should be utilized for the short circuits at even harmonics and open-circuits at the odd ones. It has been shown in Figure 4.1 an ideal Class-F PA includes open-circuit terminations at all odd harmonics and short-circuit terminations at all even harmonics. The Class-F power amplifier drain voltage waveform comprises fundamental signal and odd harmonics, which approximates a square wave and drain current waveform consists of even harmonics, respectively. Figure 4.2 shows the ideal drain voltage and current waveforms of the Class-F PA at the intrinsic drain terminal of the active device.

Furthermore in ideal case, Class-F PA load impedance at all odd harmonics should be tuned to open circuit ($Z = \infty$) and the load impedance at all even harmonic should be tuned to short circuit ($Z = 0$). The third harmonic of the drain voltage has to be out-of-phase with the fundamental frequency to generate the Class-F -like drain-voltage waveform.

Any periodic signal can be expressed as a sum of sinusoidal components at different frequencies with DC term and integer terms, as expressed in equation (4.1). Moreover, harmonics term can be find by integrating the function multiplied by harmonic sine and cosine signal in the time domain over a fundamental periods, their comparative equations are (4.2), (4.3) and (4.4), respectively. Which is the lowest frequency occurs in a signal level that we are analyzing. So adding on harmonics in correct phase causes sinusoidal waveform to become square wave and also more harmonics we add the better approximation we get for perfect square wave.

$$\mathrm{f}(t) = a_0 + \sum_{n=1}^{\infty} (\mathrm{a_n}\cos(\mathrm{n}\omega_o \mathrm{t}) + \mathrm{b_n}\sin(\mathrm{n}\omega_o \mathrm{t})) \qquad (4.1)$$

Where

$$a_0 = \frac{1}{T_0}\int_{T_0} f(t)dt \qquad (4.2)$$

$$a_n = \frac{2}{T_0}\int_{T_0} f(t) * \cos(\mathrm{n}\omega_0 \mathrm{t})\, dt \qquad (4.3)$$

$$b_n = \frac{2}{T_0}\int_{T_0} f(t) * \sin(\mathrm{n}\omega_0 \mathrm{t})\, dt \qquad (4.4)$$

$$T_0 = {}^{2\pi}/_{\omega_0}, \qquad n = 1,2,3, \ldots$$

On the other hand, however, previously described ideal drain voltage and current waveforms must be generated via proper output network, which is also able to synthesize all the requested loading conditions for the output current harmonic content. The values of terminations are easily inferred as the ratio between the respective Fourier components Vn and In, i.e, the requested set of terminations, including harmonics, has to be synthesized by a purely passive

output-matching network. As anticipated, it results in a short-circuit condition for even harmonics and an open-circuit for odd ones.

For Class-B case

$$\mathrm{f}(t) = a_0 + \sum_{n=1}^{\infty} (\mathrm{a_n}\cos(\mathrm{n}\omega_o \mathrm{t}) + \mathrm{b_n}\sin(\mathrm{n}\omega_o \mathrm{t})) \tag{4.6}$$

$$I_p = \begin{cases} I_{p\,Cos\theta}, & {}^{-\pi}/_{2} < \theta < {}^{\pi}/_{2} \\ 0, \quad -\pi < \theta \leq {}^{-\pi}/_{2}; & {}^{\pi}/_{2} \leq \theta \leq \pi \end{cases} \tag{4.7}$$

The given following expression in (4.7) represents the half-sinusoidal current waveforms in Class-B bias condition.

The general equations of Class-F PA for current and voltage waveforms are reported in [48], when harmonics terminations up to fourth harmonics are considered. The corresponding equations for current and voltage up to fourth harmonics are (4.8) and (4.9), where ∅ is the phase difference between the fundamental signal and harmonics

$$i_{ds}(\theta) = \frac{1}{\pi} + \frac{1}{2}cos\theta + \frac{2}{3\pi}cos2\theta + \frac{2}{15\pi}cos4\theta \ldots \tag{4.8}$$

In practice, it is impossible to realize output matching network (Filter) with infinite harmonics terminations, so control of up to the third or fourth harmonic is customary.

$$V_{ds}(\theta) = 1 - \frac{1}{\sqrt{3}}cos\theta + \frac{2}{3\sqrt{3}}cos3\theta \ldots. \tag{4.9}$$

The above equations predicted to deliver 90.7% efficiency at the maximum power level. Class-F PA can only maximize efficiency and output power, if there is no overlap exist between current and voltage waveforms at intrinsic drain terminal of the active device. Minimum overlap between current and voltage

waveform means less power dissipation in the active device. Furthermore, no power sent to the harmonics.

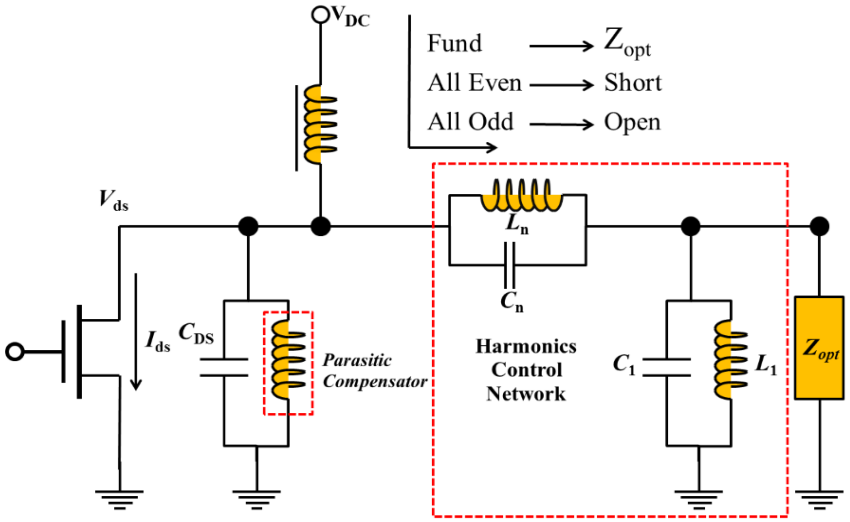


Figure 4.1: Class-F power amplifier topology with ideal infinite harmonic termination.

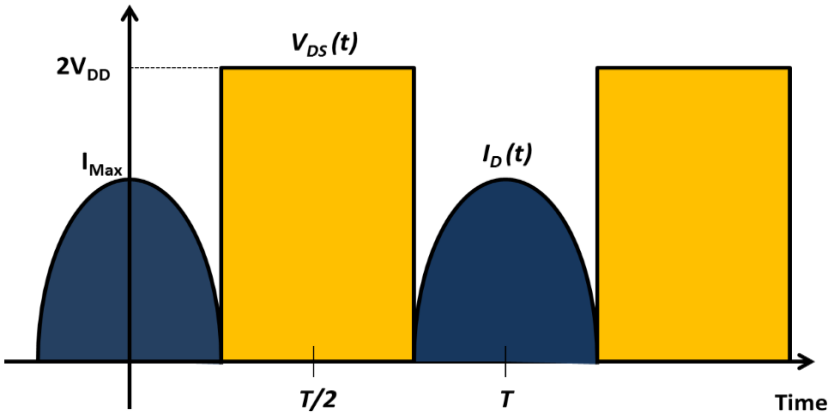


Figure 4.2: Ideal drain voltage and current waveforms for a Class-F power amplifier.

Although, by utilizing high breakdown voltage device technologies such as GaN, and SiC, large voltage waveform excursions can be sustained. To exploit these modes over a desired bandwidth, it becomes necessary to determine the required frequency-domain impedances with respect to variables. The load impedance to be presented at each harmonic can be expressed as

$$Z_{nF} = -\frac{V_{ds,n}}{I_{ds,n}} \tag{4.10}$$

$$R_{opt} = -\frac{V_{ds} - V_{knee}}{I_{max}/2} \tag{4.11}$$

The harmonic impedances are then found from following equations:

$$Z_F = R_{opt}\sqrt{\frac{4}{3} + \gamma^2} < tan^{-1}\left(\frac{\sqrt{3\gamma}}{2}\right)$$

$$Z_{2F} = -j\frac{7\sqrt{3}\pi}{24}\gamma R_{opt}.$$

$$Z_{3F} = \infty$$

$$Z_{4F} = -j\frac{5\sqrt{3}\pi}{24}\gamma R_{opt}.$$

As explained above, at least in theory, it is possible to achieve 100% drain efficiency from a Class-F PA. In practice, it is unrealistic to realize Class-F PA with infinite number of terminations. However, it is possible to minimize the voltage and current waveforms overlap by carefully designing the load network in the PA. In load network, it is also recommended to carefully handle the transistor parasitics, whose impact on PA design grows with frequency and power. In a typical Class-F/F-1 PA design [49]–[52], parasitic compensation unit and harmonic control circuit (HCC) are utilized, which are complicated and not straightforward. The output matching network must absorb C_{DS} and the interconnect inductance while providing the correct fundamental and harmonic resistances at the intrinsic drain of the transistor. In particular, this may leads to inaccuracies in high-frequency designs using packaged devices and with harmonic control above the third harmonic [49]. In number of published papers, it has been shown that the Class-F power amplifiers can achieve efficiency up to 80% with GaN HEMT transistors up to the frequency of 2 GHz, but with very limited bandwidth [56]–[58].

4.3 Design specification

Design of a power amplifier starts with a set of specification and the selection of an appropriate device. The specifications of power amplifier targeted are listed in Table 4.1. The requirements of high linearity, efficiency, and wideband bandwidth make this PA design very challenging.

Table 4.1: Class-F amplifier specifications.

Parameter	**Value**
Operating frequency	1.1-2.1 GHz
Output power	10W
Drain Efficiency	60%
Gain	12 dB

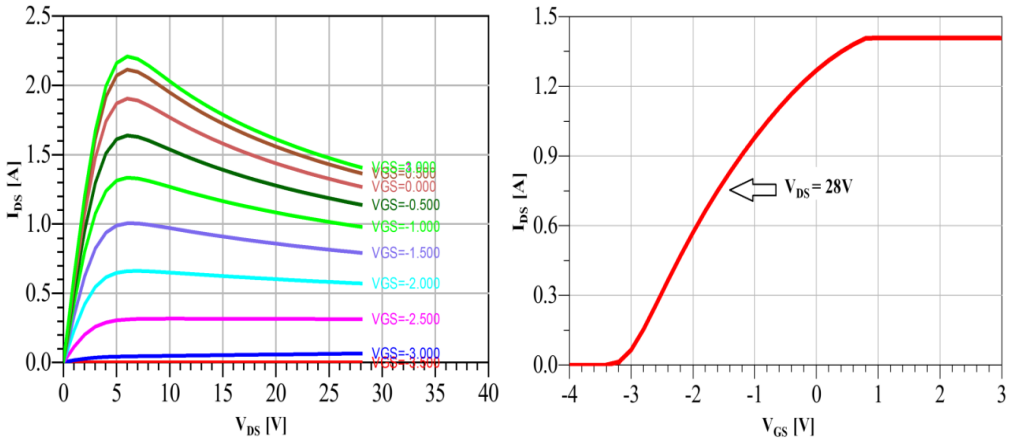
A 10 W GaN HEMT transistor from Cree (CGH40010F) is selected for this design. According to the datasheet of the selected device [59], the 10 W GaN HEMT transistor can work up to 6 GHz and is also capable to provide a output power of 40-41.5 dBm for V_{DS} = 28 V at 2.3 GHz. Some of the important specifications of the selected device are listed in Table 4.2.

Table 4.2: Active device specifications.

Parameters	**Value**
Maximum Drain-Source Voltage ($V_{DS,max}$)	84 V
Maximum Gate-Source Voltage ($V_{GS,max}$)	-10 V to $+$ 2 V
Maximum Forward Gate Current ($I_{GS,max}$)	4 mA
Maximum Forward Drain Current ($I_{DS,max}$)	1.5 A
Gate Threshold Voltage (V_{th} at V_{DS} = 10 V, I_D = 3.6 mA)	-3.8 V
Output Capacitance (C_{DS} at V_{DS} = 28V, F = 1 MHz)	1.3 pF
Output Power (P_{OUT}) V_{DD} = 28 V, I_{DQ} = 200 mA	10-12 W

4.4 Device characteristics and model

In this proposed PA design, a Cree GaN HEMT (model CGH40010) is used to implement the broadband Class-F power amplifier. Figure 4.3 shows the active device current and voltage (IV) characteristics and transfer characteristics with gate bias voltage swept from -4 to 1 V and drain voltage swept from 0 to 28 V. The simulated I-V characteristics are also compared with data sheet S-parameters. The data sheet S-parameters show very good agreement with the simulated S-parameters extracted from the device model. Ideally, for Class-F PA operational active device is biased in Class-B mode. However, in this design, it is biased at 28 V drain voltage and -2.8 V gate voltage is selected for I_{DS} = 200 mA, in order to reduce design complexity and sacrifice a smaller amount of linearity. The selected bias point is a very appropriate choice and it is also known as overdriven Class-B bias point.



(a) (b)

Figure 4.3: Cree 10W GaN HEMT active device (a) simulated current and voltage curve, and (b) simulated transfer characteristics at V_{DS} = 28 V and V_{GS} = -2 V.

An approximated large-signal device model given in [55] is used for this design as shown in Figure 4.4. The model offers an inside of 10 W Cree CGH40010F GaN HEMT device to overcome the design tradeoffs for Class-F broadband operation. In order to see the time-domain voltage and current waveforms, this model also helps to get access to the internal drain terminal. The parasatics model of the active device is quite accurate and it is supportive for presenting the second harmonic short and third harmonic open reflection coefficients at both the current generator and package reference planes of the CGH40010F device. The package-plane complex impedances correspond to 2

GHz operational frequencies, as intended for the PA designs in the following section of this chapter. With the help of the active device model, it is possible to access the internal drain terminal. Therefore, it is very clear where the drain voltage and current waveforms of interest exist. Now, we start the development of a Class-F PA at desired operating frequency.

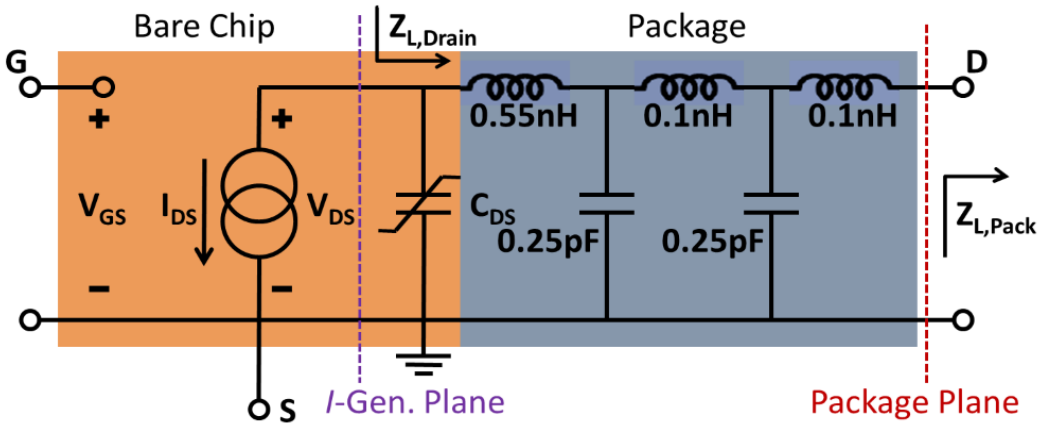


Figure 4.4: Approximated equivalent network of device output parasitics for DUT CGH40010F [55].

4.5 Device stability analysis

First step in power amplifier design approach is to perform prior stability analysis of the active device and ensure its in-band and out-of-band stability of the PA. In fact prior stability analysis is a key stage in the development of any high power amplifiers. There are many ways to verify the PA stability. In this design, three important parameters are considered to ensure the stability. First parameter is the stability factors (K), which can be calculated from two-port S-parameters. Equation 4.12 gives the value for Rollet stability factor 'K', which has to be greater than unity (K > 1) for unconditionally stable condition.

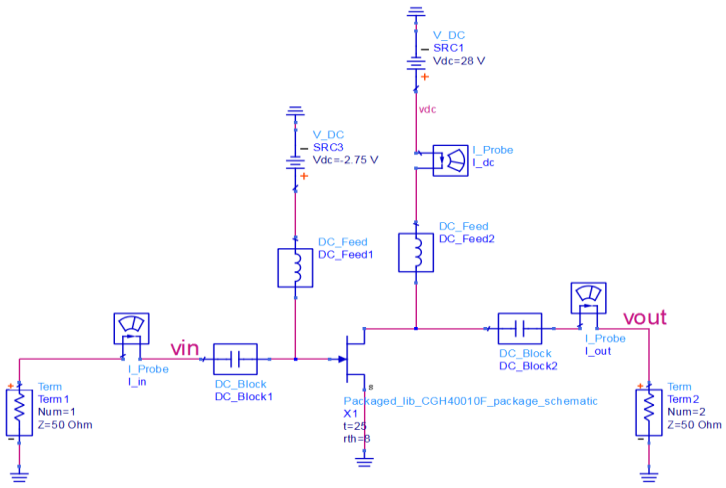
$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad (4.12)$$

In some conditions, even satisfying Rollet stability factor K > 1 may not assure the unconditional stability throughout the frequency band form two port S-parameters [25]. Due to this reason, additionally, stability factors μ_{source} and μ_{load} are taken into the account. Where equations 4.13 and 4.14 are representing

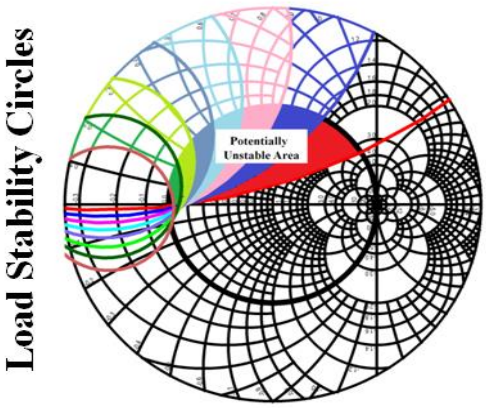
the μ_{source} and μ_{load}, respectively express their corresponding equations. For unconditional stability either μ_{source} or μ_{load} should be greater than one.

$$\mu_{source} = \frac{1 - |S_{11}|^2}{|s_{22} - \Delta(S_{11}^*)| + |S_{21}S_{12}|} \geq 1 \tag{4.13}$$

$$\mu_{load} = \frac{1 - |S_{12}|^2}{|S_{11} - \Delta(S_{22}^*)| + |S_{21}S_{12}|} \geq 1 \tag{4.14}$$



(a)

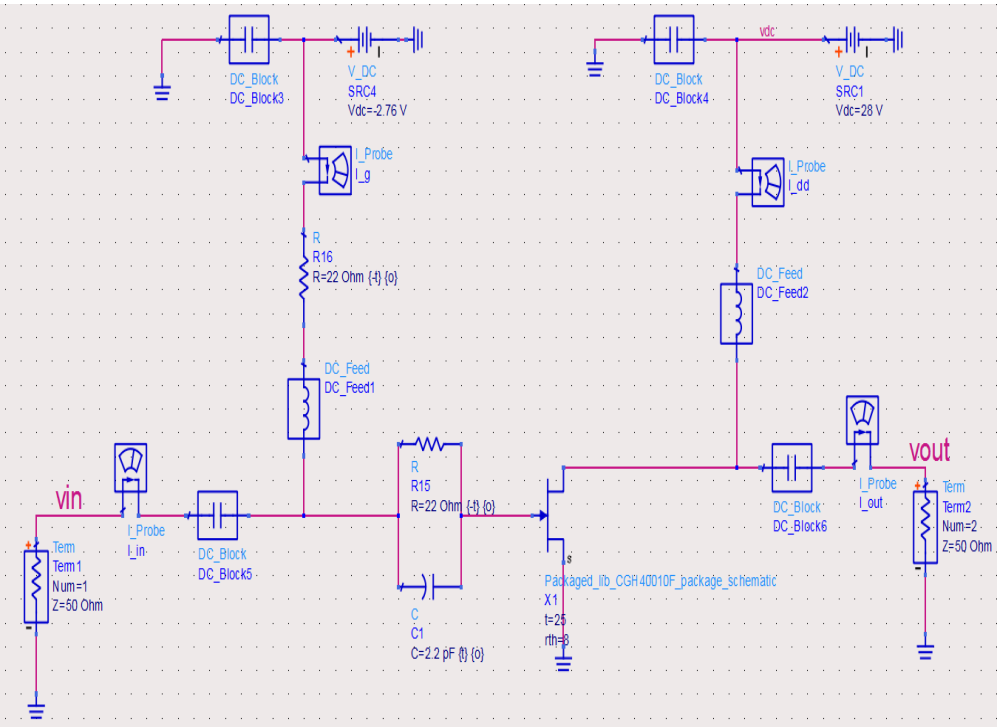


(b)

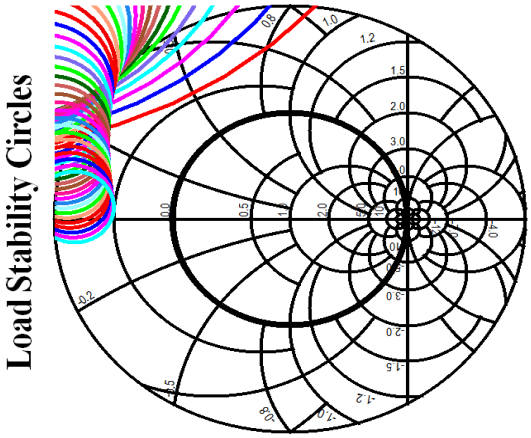
Figure 4.5: (a) Simulation setup in ADS for stability measurement and (b) simulated wideband active device load stability circles without stabilization network, highlighting the potentially unstable area in unity circle from 500 MHz to 4 GHz.

Keysight's ADS CAD environment is used to calculate and plot the stability factor 'K', as well as μ_{source} and μ_{load} stability for each frequency of interest. Figure 4.5 (a) shows the ADS circuit setup for performing stability analysis. The S-parameters simulation was performed on DUT (CGH40010F) model provided by Cree GaN biased at V_{GS} = -2.8 V and V_{DS} = 28 V from 500 MHz to 6 GHz with steps of 10 MHz. Figure 4.5 (b) shows the potentially-unstable region inside the unity circle for the frequency band upper limit of approximately 3.5 GHz, as well as in the intended device operational frequencies band of 1.1 to 2.1 GHz.

Power amplifier is stabilized through the use of a series 47 Ω resistor with gate bias and parallel RC circuit at the input of an active device as described in Figure 4.6 (a). The CGH40010F stability factors are simulated again after the stabilization network has been updated with industrial standard component value. The simulated results showed source, (μ_{source}), load (μ_{load}) and Rollet Stability Factors (K) are greater than one, which means unconditionally stable condition exist for active device throughout the entire range of frequencies. The load stability circles are shown in Figure 4.6 (b).



(a)



(b)

Figure 4.6: (a) Simulation setup after adding the stability circuit and (b) simulated wideband active device load stability circles with the stabilization network, highlighting the removal of potentially unstable region from the frequency range of 500 MHz to 4 GHz.

4.6 Source-pull /load-pull analysis for harmonics

In this design, harmonics termination up to fourth harmonic is considered. Because higher order harmonics termination only improved a little efficiency, however, it increases the circuit complexity. Even, it is very difficult to terminate higher harmonics properly at the intrinsic drain terminal of the device due to the effect of parasitics components. Therefore, only the 2nd, 3rd, and 4rth harmonics are terminated in the output matching network for shaping the waveforms.

After determining the DC bias condition and analyzing the stability analysis as explained in the previous sections. Next goal is to take out the optimum source and load impedances at fundamental and harmonics by performing load- and source-pull simulation. According to the design requirement, only the efficiency is targeted for ultra-wideband operation. Therefore, only single-tone load pull simulation is performed up to fourth harmonics with constant input power for extracting optimum impedances. Table 4.3 shows the ideal Class-F reflection coefficient required for proper harmonics termination at current generation plane. In addition to this, phase rotation occurred due to the parasitics of the active device is also shown.

In the first step, the source- and load-pull analysis is performed at fundamental for maximum efficiency with 28 dBm input power at 2 GHz. The

extracted impedances are at device package plane for optimum load and source impedances are Z_L = 20 + j*20 Ω, and Z_S = 10 + j*20 Ω, respectively. In the second step, source- and load-pull for simulation for the 2nd, 3rd, and fourth harmonics are performed. The optimum extracted impedance at package plane is shown in Table 4.3. The second and fourth harmonic impedances are set to be slightly capacitive for achieving the highest PAE, mainly due to the non-linear behavior of the output capacitor [60].

Table 4.3: Class-F PA harmonic load reflection coefficients at current generator and package-plane at 2 GHz.

Frequency	**Ideal Class-F reflection coefficient at l_{Gen}-plane**	**Ideal Class-F reflection coefficient at package plane for f_0=2GHz**
$2f_0$	$1\angle 180^o$ (short)	$1\angle -170^o$
$3f_0$	$1\angle 0^o$ (open)	$0\angle -0^o$
$4f_0$	$1\angle 180^o$ (short)	$1\angle -170^o$

4.7 Output multi-harmonic matching network

The output matching network design is developed in the Keysight Advanced Design System (ADS) and simulation for output matching network is carried out at desired frequency with 50 Ω reference impedance. By defining a microwave substrate in the design environment, the chosen laminate (FR4 of thickness 0.8 mm) was modeled enabling an implementation of the output matching architecture. The synthesized output-matching network is implemented using transmission lines (TLs), quarter and half-wavelength stubs to provide the appropriate phase shifting and, their respective short and open terminations at the harmonic frequencies. For output matching network design, the inductors are realized by high-impedance TLs, while the capacitors are replaced by low-impedance O.C. STs. At 2 GHz, on this FR4 substrate, a quarter-wavelength translates to approximately 19 mm length and width 1.458 mm impedance microstrip line.

The process of designing the output-matching network start from the provided model of the active device, and step by step design procedure is presented in the following segments: The desired current generator-plane loads (Table 4.4) are rotated by the DUT output parasitics to the measured package plane loads (Figure

4.7). These are the loads for which to design the harmonics termination and external matching network.

Table 4.4: Optimum harmonics load impedances of Class-F PA at current generator and embedded package-plane at 2 GHz.

$I_{GEN.}$ Plane	
Harmonics	**Impedances Values [ohm]**
F0	61.5Ω
2F0	short-circuit
3F0	open-circuit
4F0	short-circuit

Package Plane	
Harmonics	**Impedances Values [ohm]**
F0	19.2 + j*22.8Ω
2F0	752.3 + j*22.8Ω
3F0	2.7 - j*4.5Ω
4F0	4.2 + j*5.3Ω

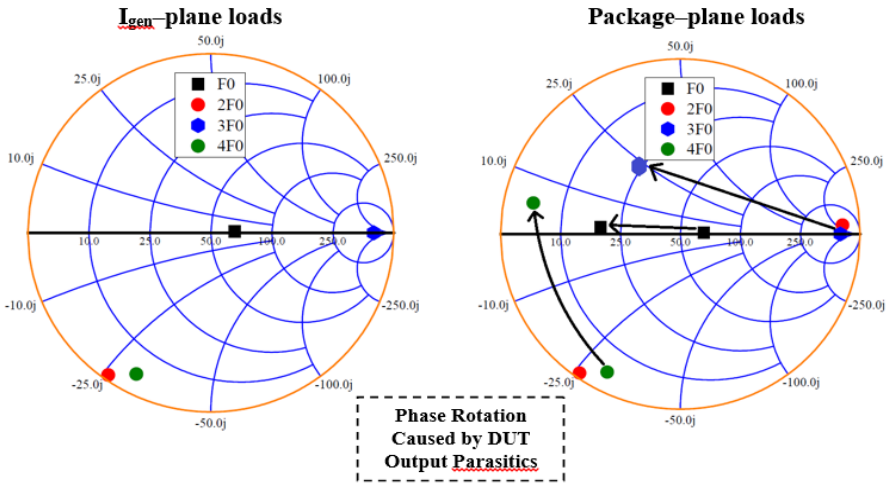


Figure 4.7: Smith charts showing effect of the output parasitics on the desired optimum lgen.-plane Class-F loading translation to the device package-plane.

In the first step of OMN design, working back from the device package plane, we require a length of line that, when we added to the parasitic-induced rotation of the second harmonic phase, will be a total of a $\lambda/2$ at $2f_0$ (wavelength). At the end of the $\lambda/2$ at $2f_0$ line, a $\lambda/2$ at $2f_0$ shorted stub was used (which also enables a route for DC bias introduction) and a $\lambda/4$ at $2f_0$ open stub is also required to provide open circuit at the DUT lgen.-plane, as shown in Figure 4.8.

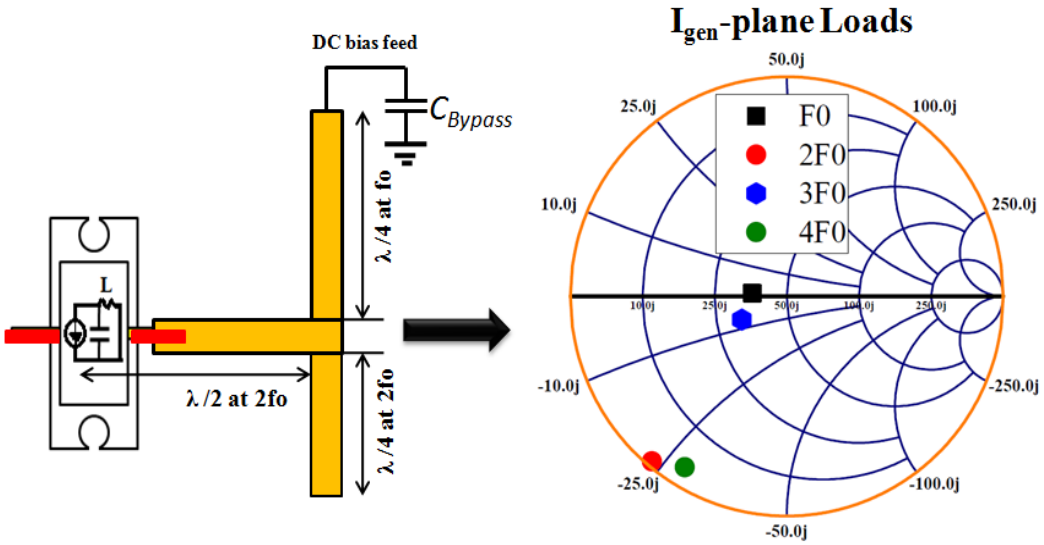


Figure 4.8: Matching the second harmonic load (short) with a λ/2 at $2f_0$ shorted stub and λ/4 at $2f_0$ open stub, with the effect of this on the third and fundamental loads shown.

In the second step, $3f_0$ loading at the end of the λ/2 at $2f_0$ line, approximately a λ/4 at $3f_0$ line is added. In order to provide an open circuit at the lgen-plane for Z3f0 at the end of λ/4 at $3f_0$ line position two open stubs with length of λ/4 at $3f_0$ line are placed (Figure 4.9).

In the third step, the fundamental matching network is designed by using a T-matching network following the open and short matching of the third and second harmonic loads, as can be seen from Figure 4.10. In the final step of OMN design, before realizing the PA, OMN is connected to the parasitic model of the GaN transistor. As a result, parasitic network become part of the OMN. The length of each TL section is finely tuned to properly align the OMN impedance trajectory to the target impedances at both the fundamental and harmonic frequencies. The tuned OMN is finally optimized together with the actual transistor model to achieve maximum efficiency. The output matching network topology is a particularly good fit for this GaN transistor with a C_{DS} of about 1.2 pF. The results in Figure 4.12 show both the target package-plane loads impedances and achieved impedance are closely matched.

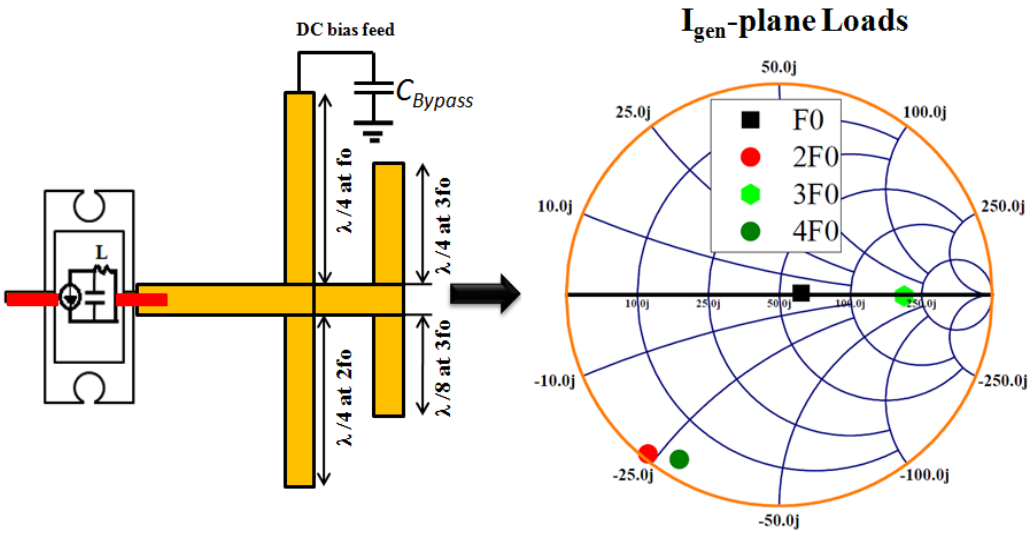


Figure 4.9: Third (open) and second harmonic loads now matched with the addition of a λ/4 at $3f_0$ open stubs. The effect of this on the fundamental load is also shown.

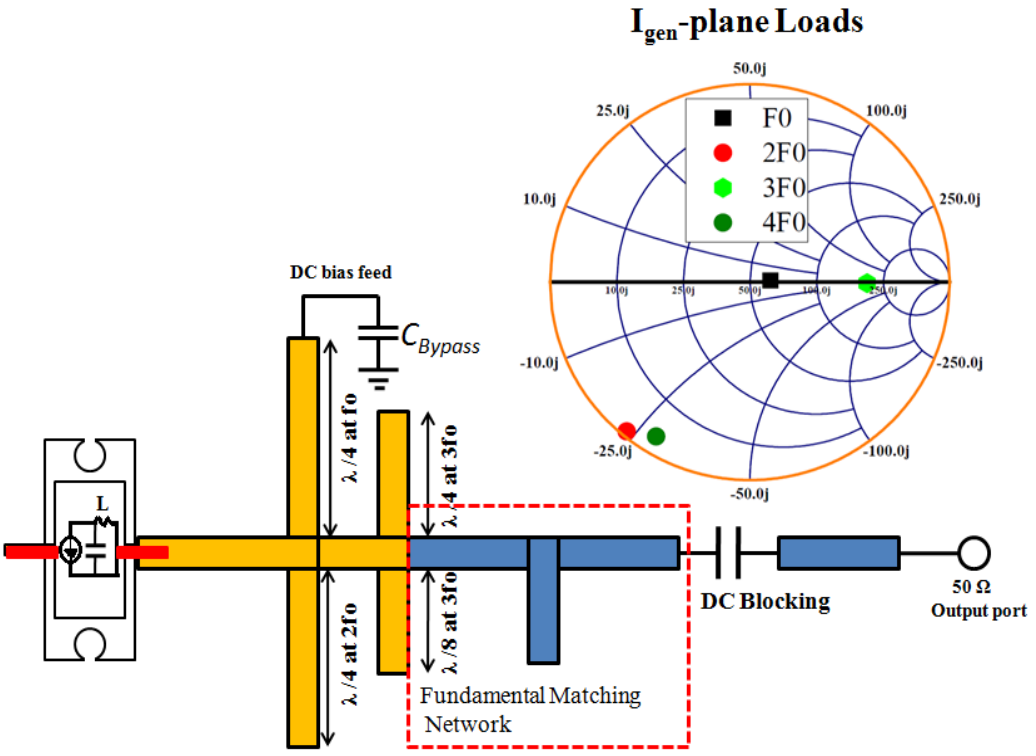


Figure 4.10: Fundamental loading now completes the three harmonic matching networks to approximately the impedances required.

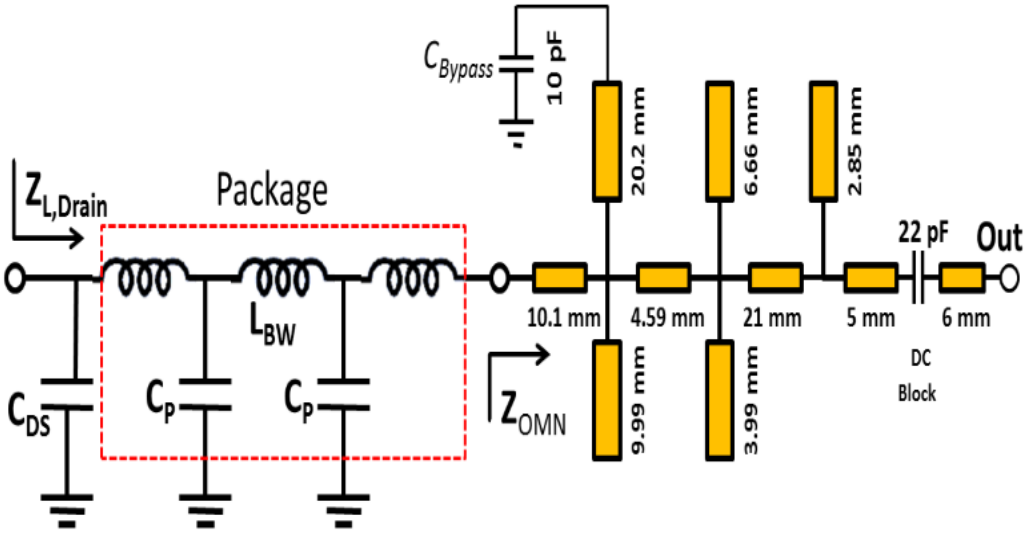


Figure 4.11: Optimized output matching network design at 2 GHz for Class-F PA.

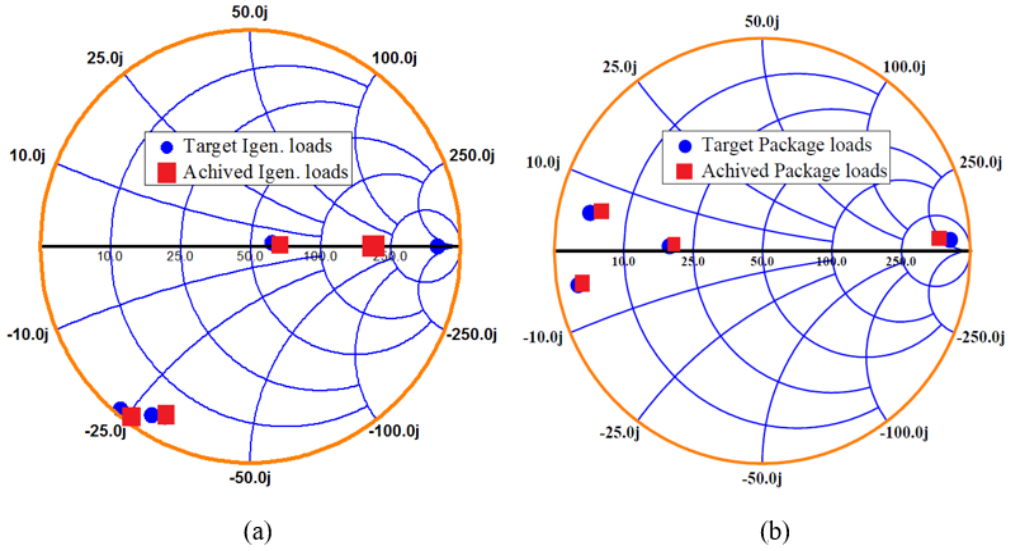


Figure 4.12: S-parameter simulation results displaying the impedances presented by the output network to the device package-plane and Igen. plane, as specified.

Figure 4.11 is showing the implemented OMN with their corresponding length and width of transmission lines. The fundamental and harmonics impedances are shown in Figure 4.12 (a) at the package plane, while the Figure 4.12 (b) is showing the impedance at the intrinsic drain plane, respectively. The

implemented OMN achieved the desired fundamental matching over the target frequency since the impedance is very close to the optimal points.

4.8 Input matching network

In this simulation experiment, we adapt the method of adding bias circuit at the short circuit microstrip, which will minimize the impact on the fundamental and harmonic impedances of matching network. The input matching circuit is shown in Figure 4.13. In input matching circuit, a 33 Ω series resistor with gate bias and a parallel RC circuit used to ensure in and out of band stability of PA. The input matching circuit provides a match at the fundamental frequency, and an open at the second harmonic. This matching network is then implemented with TLs, the same as the ones in the output network.

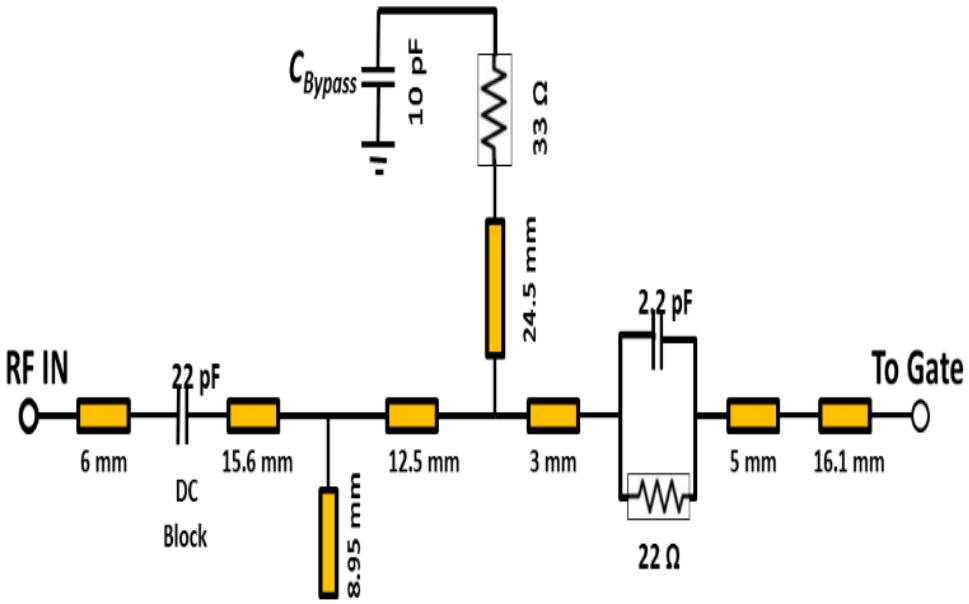


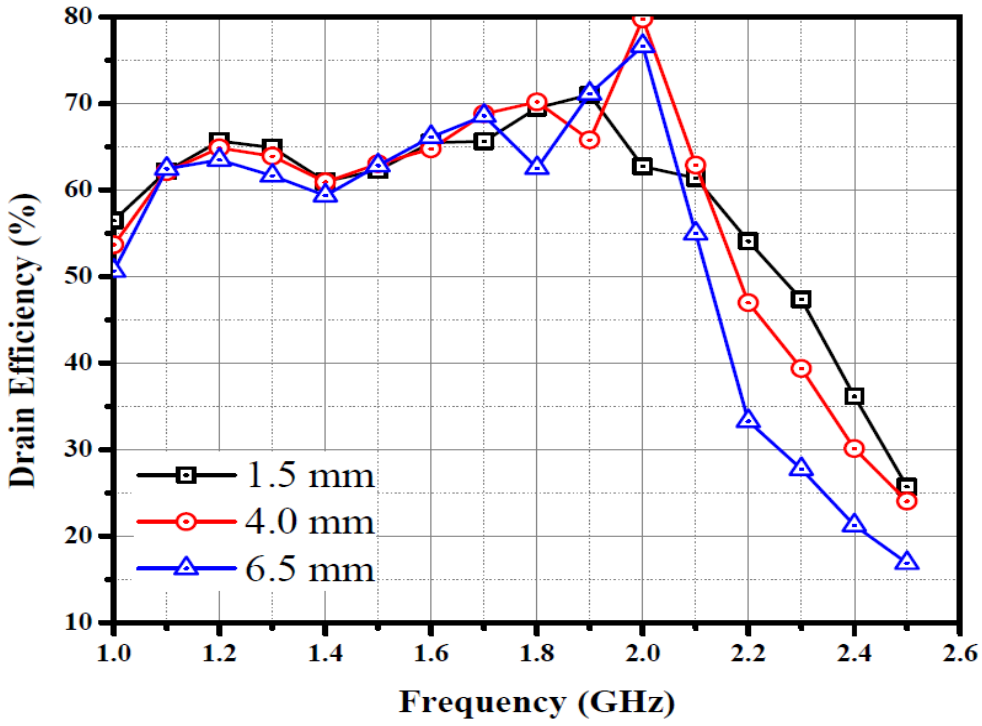
Figure 4.13: Final input matching based on microstrip at 2 GHz for Class-F PA.

4.9 Effect of harmonic termination on bandwidth

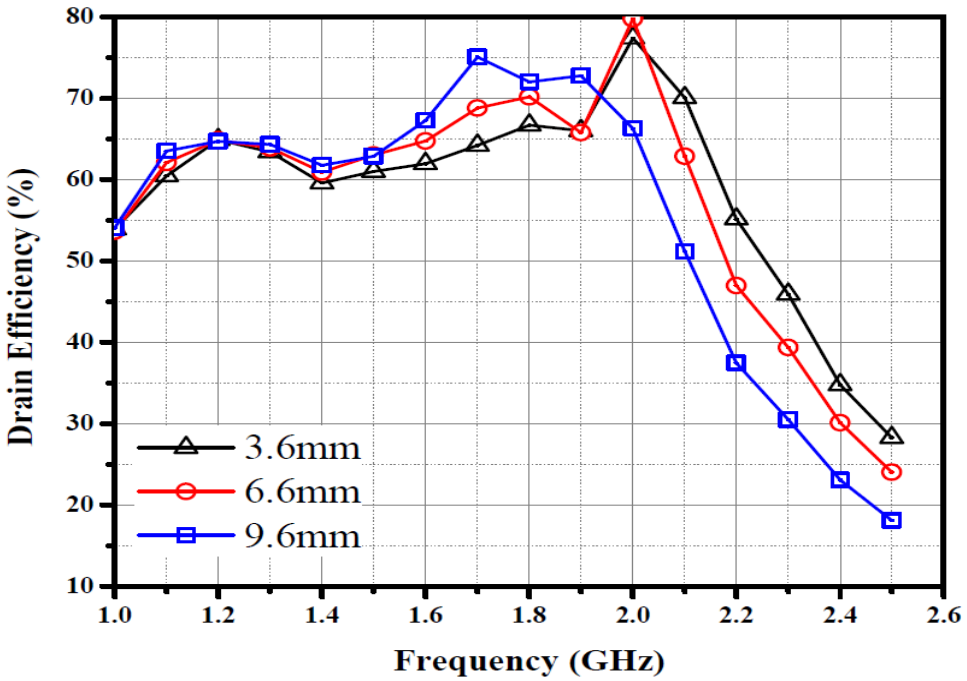
Based on the simulation results discussed in the previous section proposed PA performed superior performance at the design frequency. In order to achieve efficiency higher than 60% over the desired bandwidth, an optimization routine is run to fine-tune the fundamental and harmonic load impedances presented by the

OMN network. In particular, the effect of the second, third and fourth harmonics on the PA efficiency is investigated. This is carried out where the impedances are successively tuned until optimum broadband operation is achieved. The impedance tuning is done by allowing a minimal variation (±3 mm) in the physical lengths of the microstrip lines and stubs.

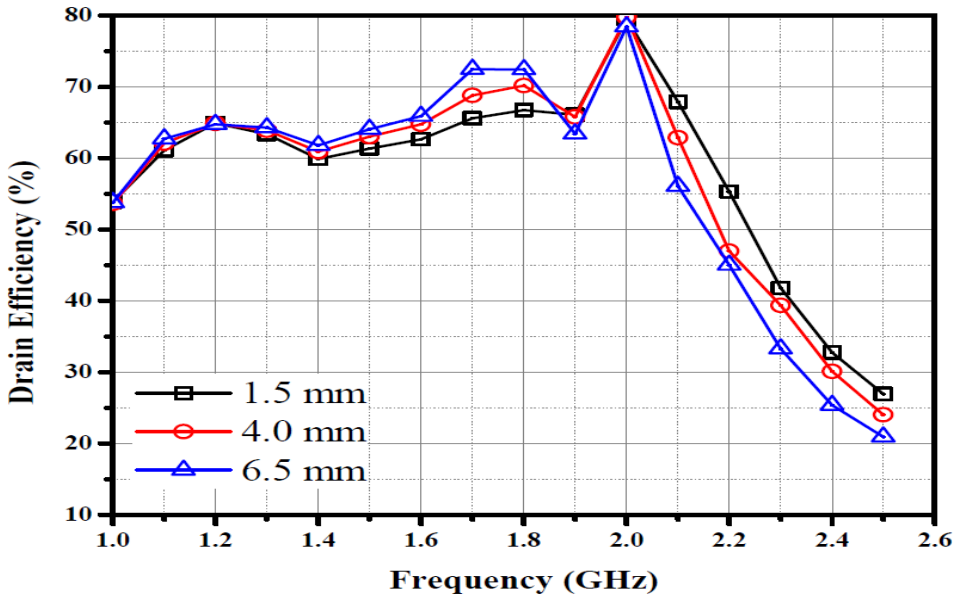
The second-, third- and fourth load-harmonic impedances are varied with the lengths of the open stubs above and below the optimal point. Simulated frequency responses of DE for different circuit configurations are recorded and shown in Figure 4.14. The configurations (a) based on second harmonics impedance variation from 1.5 to 6 mm and its corresponding drain efficiency is shown in Figure 4.14 (a). It is observed that the load impedance at the second harmonic also have significant effect on the efficiency throughout the band. Second harmonic load impedance was carefully tuned for optimum bandwidth performance.



(a)



(b)



(c)

Figure 4.14: Simulated DE for different circuit configurations for desired bandwidth, (a) 2nd harmonics impedance variation, (b) 3rd harmonics impedance variation, and (c) 4rth impedance variation.

The configurations (b) based on third harmonics impedance variation from 3.6 to 9.6 mm and its corresponding drain efficiency was recorded. It is observed that the load impedance at the second also has significant effect on the efficiency throughout the band. Second harmonics impedance was properly tuned for ultra-wide band option. Figure 4.14 (b) shows the drain efficiency for three different circuit configurations.

Finally, the effect of the fourth harmonic load impedance on bandwidth was also studied. The fourth harmonics load impedances are tuned by varying the lengths of the open stubs used for termination and the corresponding PA bandwidth is recorded. It can be seen from the Figure 4.15 (c), it has very less effect on bandwidth in comparsion to second and third harmonics.

In summary, it is observed that the load impedance at the second and third harmonics are crucial to obtain a wide bandwidth, as desired. On the contrary, the load impedance of the fourth harmonic has little effect on bandwidth, while it can be tuned to effectively increase the drain efficiency at the design frequency.

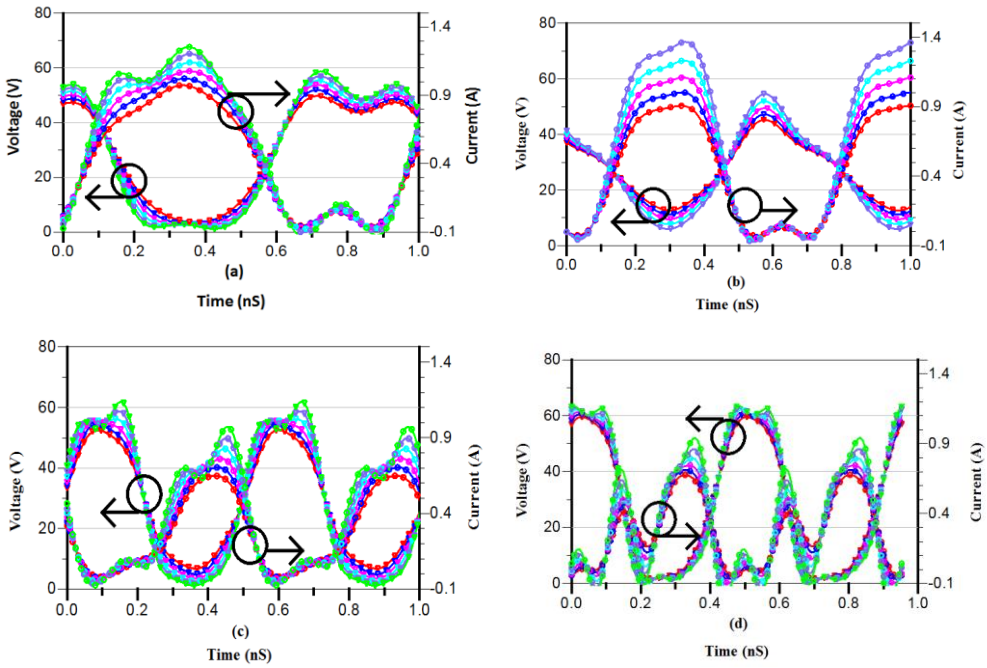


Figure 4.15: Drain current and voltage waveforms of the Class-F PA at different frequencies with the increasing input power (a) 1.1 GHz, (b) 1.5 GHz, (c) 1.95 GHz design frequency and (d) 2.1 GHz.

After the harmonics tuning, simulated drain voltage and current waveforms were extracted at the internal drain terminal by de-embedding package parasitics

using the device model discussed in section 4.5. Figure 4.15 shows the simulated drain voltage and current waveforms at 2 GHz. The overlap between the drain voltage and current waveforms is very less, causing lower power consumption by the GaN HEMT and enhancement in PAE within band of interest.

4.10 PA implementation

After the load harmonics tuning in final step, input and output matching networks based on transmission lines are combined together (Data is given in appendix B). Then, an electromagnetic simulation is performed using the large signal device model in the EM simulator. A post-optimization also performed for best PA performance. The final design values for the proposed PA are shown in Figure 4.16.

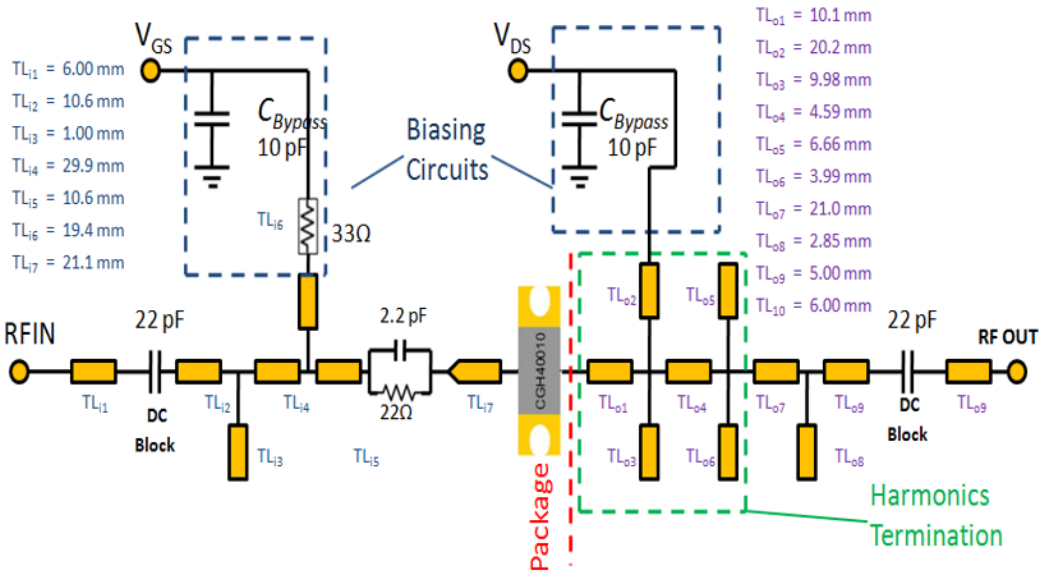


Figure 4.16: Final circuit schematic of the ultra-wide band Class-F PA.

The complete PA is fabricated by connecting the transistor between input and output matching networks, and a copper tape transmission lines on a 0.80 mm FR4 substrate with dielectric constant of 4.7 was used. The physical implementation of the Class-F PA is shown in Figure 4.17. The biasing networks is realized by a λ/4 transmission line and 10 pF bypass capacitor. A heat sink was inserted under the substrate to provide good thermal control. The footprint of the fabricated PA is 120×40 mm.

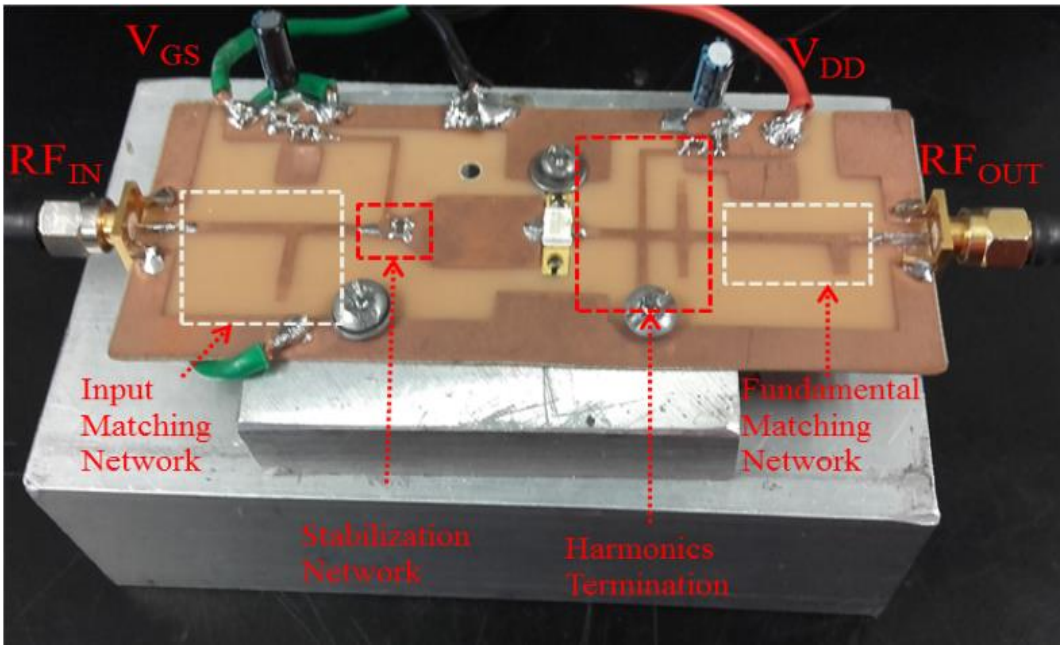


Figure 4.17: The photograph of realized prototype of broadband Class-F PA.

4.11 Experimental results

The prototype has been characterized in small- and large-signal regime in order to establish the performance of the proposed design. The measurement equipment includes the Agilent 8510C vector network analyzer (VNA) and the HP 8563E spectrum analyzer. A SOLT calibration procedure is used to calibrate the VNA [61]. Figure 4.18 shows the measured and simulated small-signal performance of the PA biased at V_{DS} = 28 V and I_{DS} = 200 mA. The measured small-signal gain curve closely tracks the simulated one between 1.2 to 2.0 GHz, while it is slightly lower at the edges of the targeted bandwidth. An approximately constant small-signal gain in excess of 12 dB is maintained over a 800 MHz bandwidth. However, a shift of the center frequency from 2 GHz to 1.95 GHz is detected. In fact, the S_{11} curve has a global minimum around 1.95 GHz. This can be ascribed to some fabrication errors, such as changes in the width and length of the transmission lines, occurred during in-house fabrication.

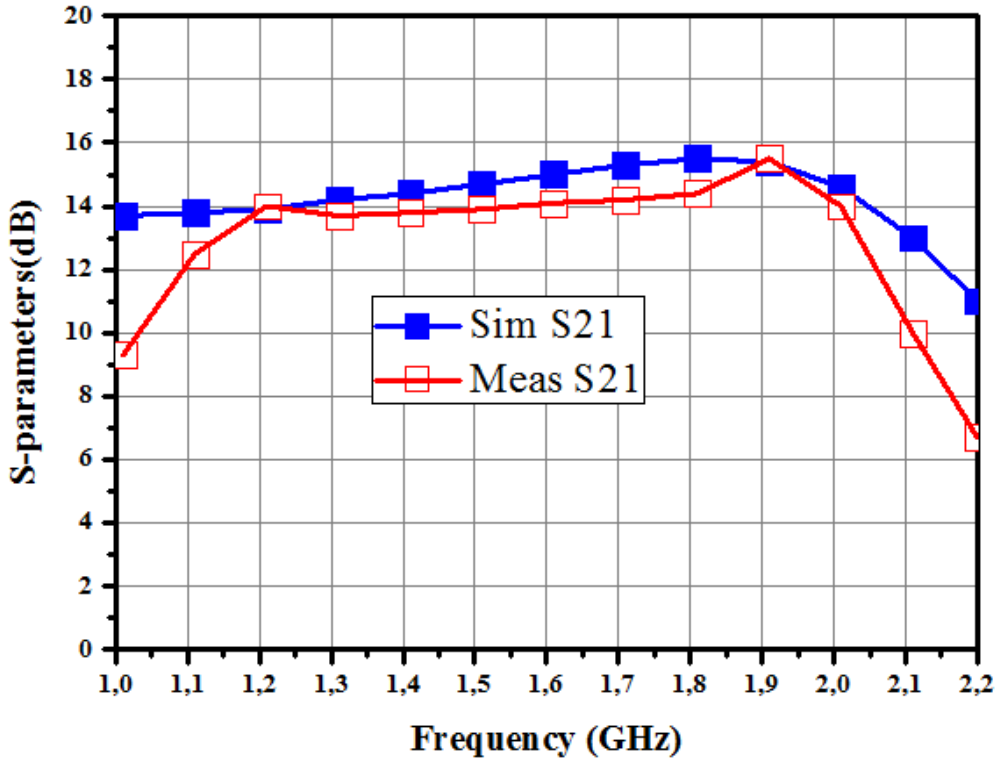


Figure 4.18: Simulated and measured small-signal gain versus frequency for the realized PA.

Figure 4.19 shows the measured and simulated output power, gain, drain efficiency, and PAE performances at 1.95 GHz. A peak drain efficiency of 73% is measured at 1.95 GHz, together with an output power of 40 dBm and a power gain of 13.4 dB. The same measurement is performed over the entire design frequency band, as reported in Figure 4.20. The efficiency (DE) curve has a peak at 1.95 GHz. The measured gain closely follows the simulated curve up to 2 GHz, where it maintains gain close to 15 dB. A slight difference stands out at the upper band edge, where the measured gain drops to 10 dB while the simulated one does not go below 12 dB. The output power curves are almost superimposed and range from 39.5 to 41 dBm. Finally, the measured efficiency ranges from 60 to 73% with an average value of around 65%. The measurement is in close agreement with the simulation, which reports drain efficiency of 63-77 %.

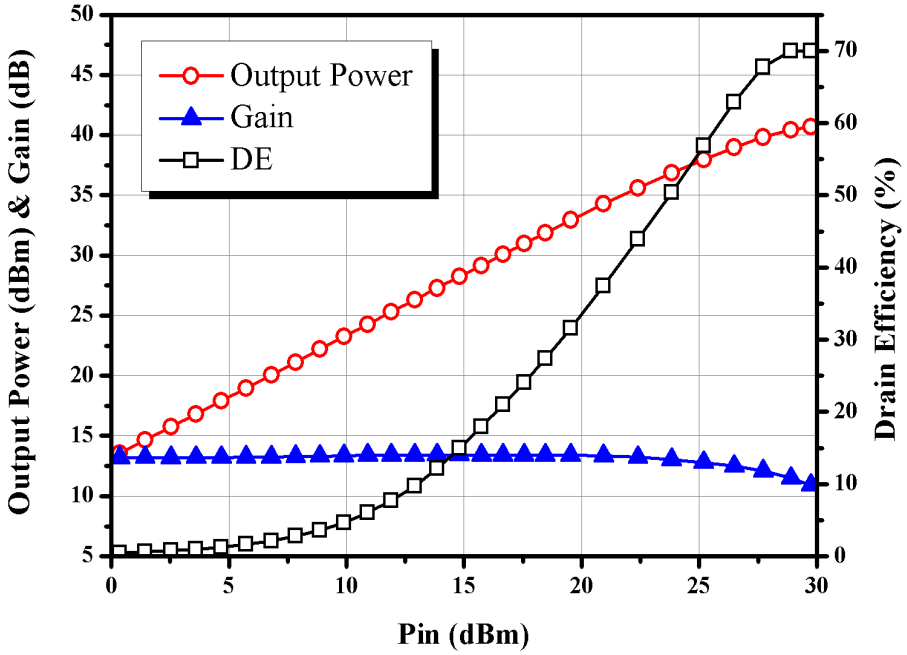


Figure 4.19: Measured drain efficiency, output power and gain vs. input of the proposed Class-F at 1.95GHz.

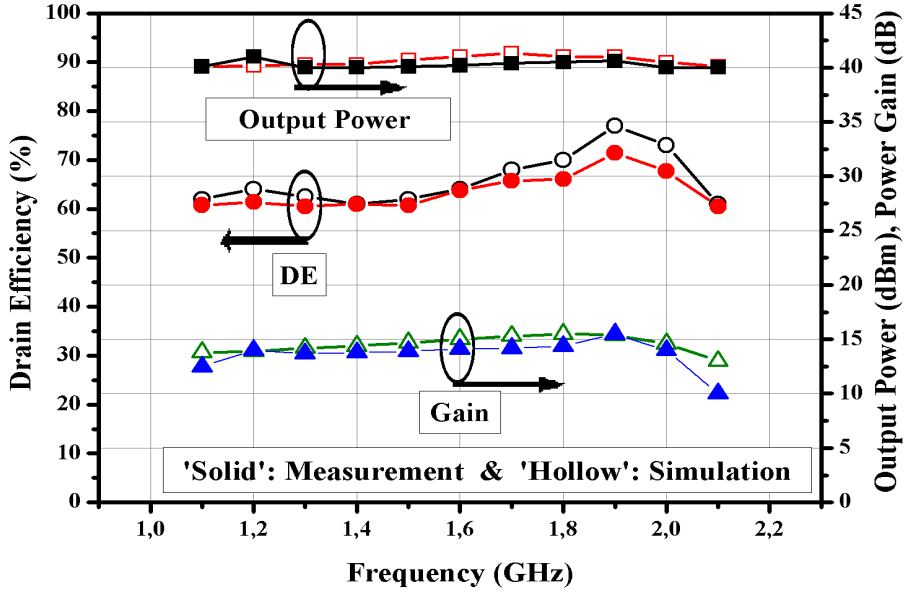


Figure 4.20: Simulated output power, power added efficiency and drain efficiency vs. frequency.

Table 4.5 compares the performance of the present design and of other published works on state-of-the-art Class-F PAs. The designed PA has an efficiency comparable to the other PAs while achieving a bandwidth of 62%, which is wider than other published results. Although the output power level is not the highest achieved, the power gain performance is particularly notable.

Table 4.5: Performance compression with state-of-the power amplifier.

S/N	Class Of Operation	Bandwidth		Power (W)	Gain (dB)	Effeciency (%)
		(GHz)	(%)			
[61]	Class-F	1.7-2.2	26%	8.7-13.4	>11.4	>55 PAE
[62]	Class-F-1	1.6-2.2	31%	13	>13	>60
[63]	Class-F	1.45-2.45	51%	11-16.8	>10	70-81
[64]	Class-F	2.15-2.65	21%	11.4- 15	>10	>63
[65]	Class-F	1.4-2.5	56.8%	11.2-7.4	>11	73-88.6
[66]	Class-F	1.35-2	39%	11-14	>10	65.8 - 76.3
[67]	Class-F	0.55-1.1	51%	8.5-13	>9	70-80
[68]	Class-F	1.9-2.9	42%	38	>10.8	>60
This work	Class-F	1.1-2.1	62%	9-11	>13	>60

4.12 Summary

This chapter presented design and implementation of a broadband Class-F power amplifier based on 10 W (CGH40010F) GaN HEMT from Cree Inc. packaged model. Load-pull and source-pull techniques were utilized to determine the optimal source and load impedances at fundamental and harmonic frequencies. The input and output matching networks were optimized using the Momentum simulator. To efficiently deal with the parasitics of the packaged device and perform harmonic control up to the fourth-order, low-pass matching network is designed and implemented as the output circuit. The fabricated broadband Class-F power amplifier can achieve maximum 60-77% of saturated drain efficiency, and 10 W output power throughout the desired band. The simulation and measurement results verify that the broadband Class-F amplifier is suitable for a high-efficiency PA over a frequency range for 1.1 to 2.1 GHz.

Chapter 5

Single- and Dual-Input Doherty PA

5.1 Introduction

In the last two chapters, the focus was on maximizing the peak efficiency and linearity of a single-ended PAs for wider bandwidth. Generally, the highest efficiency of a PA is obtained close to the saturated output power and good linearity in Class-A bias conditions or close to this bias point. However, as explained in chapter 2, the efficiency of a single-ended PA in the back-off region decreases significantly, when it is fed with high peak-to-average-power-ratio signals.

In advanced wireless communication systems, the involvement of high PAPR signals can push PA to work at a mean output power, which is well below the saturation region resulting in low levels of average efficiency. There are several techniques proposed to increase the average efficiency of the PA in the literature. However, it is reported in [10], that the Doherty PA is a promising and most effective solution. DPA working efficiency is almost constant for a targeted range of input levels or output power, typically at the 6 dB back-off [69-74], [76].

In this chapter, a single- and dual-input Doherty power amplifier for LTE application in the 3.5 GHz frequency band are presented and compared. Main goal of this study is to improve the performance of gallium–nitride (GaN) Doherty transmitters over wide bandwidth in the 3.5 GHz frequency band. For this purpose, the linearity-efficiency trade-off for the two proposed architectures is

discussed in detail. Simulated results demonstrate that the single- and dual-input Doherty power amplifier exhibited a peak drain efficiency (DE) of 72.4% and 77%, respectively. Both the circuits show saturated output power more than 42.9 dBm throughout the designed band. Saturated efficiency, gain and bandwidth of dual input DPA is higher than that of the single-input DPA. On the other side, dual-input Doherty power amplifier linearity is worse compared to the single-input DPA.

5.2 Doherty power amplifier theory

Until now, plenty of work has been presented on single-band DPAs [73-78]. However, this does not meet the requirements of multi-standard of modern future radio base-station for the mobile communication. Therefore, much effort has been made to extend the bandwidth of the DPA by using various different matching networks [75] or by exploiting wideband matching networks [2], [76-79]. Moreover, several exploration outcomes have shown that the acquired bandwidths are not yet broad enough to cover many LTE bands simultaneously and to short the time-to-market of new wireless standards. In addition to this, one more drawback is that, broadband DPAs not always have optimal operation for the operating bandwidth. Consequently, it leads to rapid performance degradation of a DPA, when it compared to the designed frequency performance. Before designing a DPA, basic building blocks of DPA and working principle reviewed. After that, a detailed design approach will be presented for single- and dual-input DPAs.

A simplified circuit diagram of a conventional DPA is shown in Figure 5.1. It comprises on two current sources, one for the main amplifier and other representing the auxiliary amplifier with a λ/4 impedance inverter line (Z_T). The load seen by the main and auxiliary current sources are represented by the Z_M and Z_A, respectively. Z_M and Z_A can be controlled by the current level of other current source. As the current of the auxiliary current source increased after a certain input, the impedance seen by the main amplifier (Z_M) starts to decrease. When both the current sources are producing the same amount of current ($I_M = I_C$), in this condition impedances seen by the amplifiers are equal ($Z_M = Z_C$).

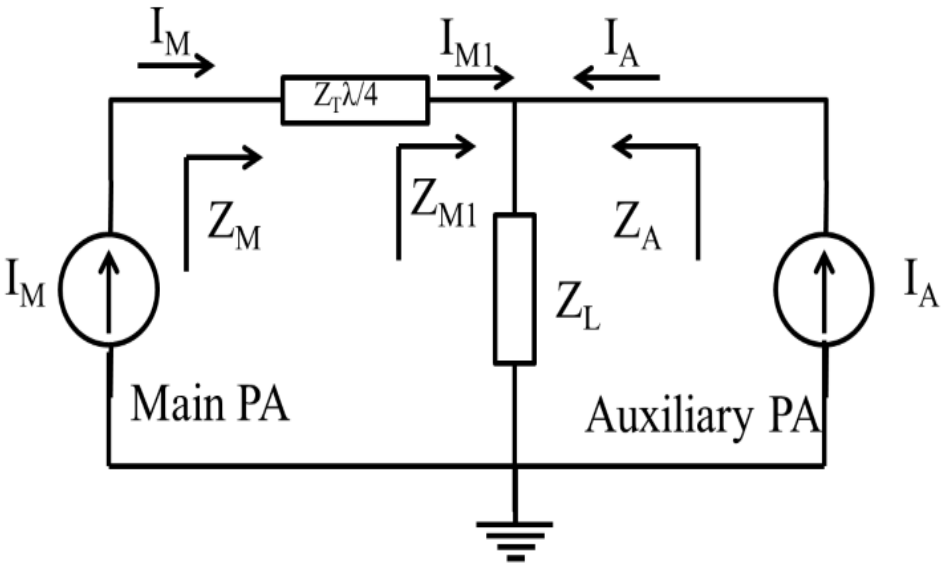


Figure 5.1: A simplified schematic of the conventional Doherty power amplifier.

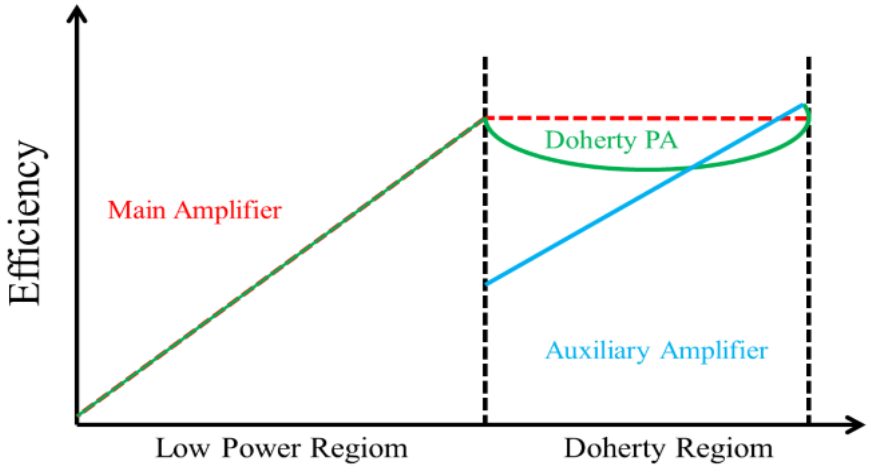


Figure 5.2: Efficiency behavior of main, auxiliary and Doherty amplifiers.

According to the Doherty amplifier working principle, it can divided into two different regions, low power and Doherty regions. In the low input power region, only the main amplifier is in on state. Therefore, there is no load modulation occurring at recombining node and only the main amplifier is responsible for the output current ($I_{OUT} = I_M$). However, when the input power reaches to certain value, auxiliary amplifier turned on and the main amplifier amplifier reaches its maximum efficiency. At the same time load impedance seen by the main start

decreasing by following the current ratio. At the saturation, Z_M and Z_A reaches Z_L to $Z_L/2$ and ∞ to Ropt, respectively. These are the load impedances at the maximum output power of both amplifiers at saturation. Figure 5.2 is showing the theoretical drain efficiency curves of carrier, auxiliary and Doherty power amplifier.

A basic block diagram of a single-input DPA is shown in Figure 5.3. It comprises on two PAs, a main amplifier and an auxiliary amplifier that are joined by input splitter, phase compensation line, a $\lambda/4$ impedance inverter, and recombining network. However, the single-input DPA using a power splitter suffers from power-dependent phase imbalance between the main and peaking stages resulting in suboptimal performance. An alternative way of resolving the power-dependent phase imbalance is to split the input of the main and peaking stages such that they are independent of each other. Unlike single-input DPAs, dual-input DPAs eliminate the analog input splitter, allowing independent control of the input signals to the main and auxiliary PA. In this way, the input power to both amplifiers can be efficiently distributed so that the power wasted in the peaking branch is minimized when the peaking PA is turned off. In addition to that, the phase relation between branches can be independently controlled at different frequencies thus enabling frequency re-configuration and wider bandwidth implementations. Because of this reason, the dual-input DPA is becoming more and more attractive, as a digital Doherty amplifier. It is an attractive transmitter architecture for current and future wideband communication systems [69]. A block diagram of a dual-input DPA is shown in Figure 5.4. It consists of two parallel amplifiers, a main amplifier and a peaking amplifier, and an impedance inverter network.

The work in this chapter focuses on the development of two new designs to overcome the limitations of conventional Doherty power amplifier. Especially, the focus was on maximizing the efficiency and the output power of single- and dual-input DPAs for wider bandwidth in the 3.5 GHz frequency band. We designed and simulated both the circuits in Keysight Advanced Designed System (ADS) based on 10 W GaN HEMT devices. A comprehensive comparison is also made between single- and dual-input DPA. In the simulated results, the dual-input DPA achieves a higher drain efficiency, gain and bandwidth compare to single-input DPA, but at the cost of linearity.

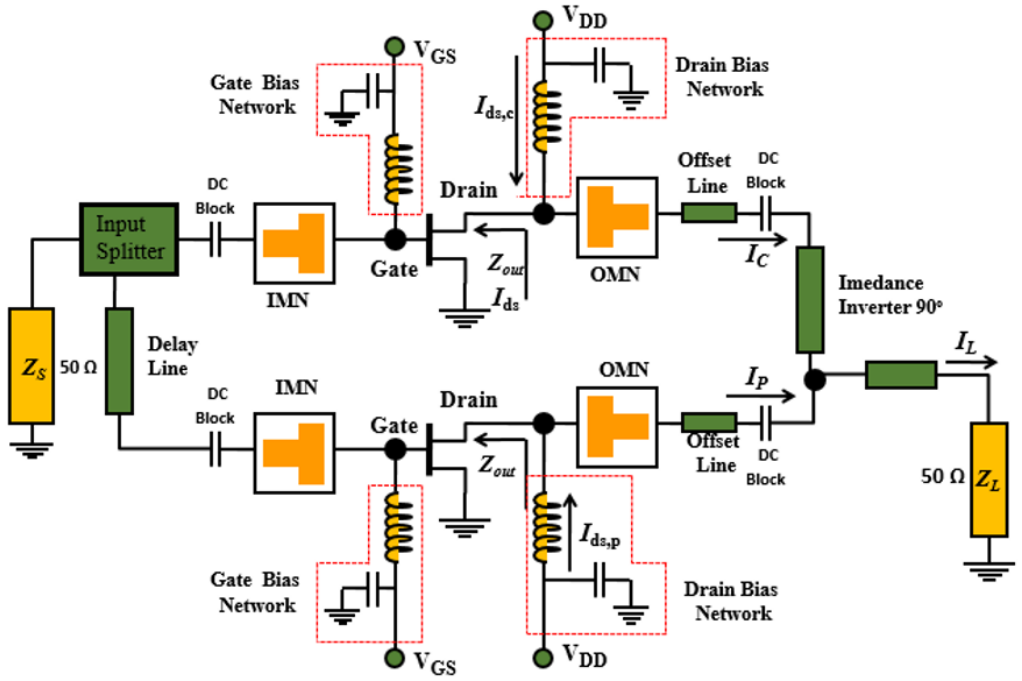


Figure 5.3: Circuit topology of single-input Doherty power amplifier.

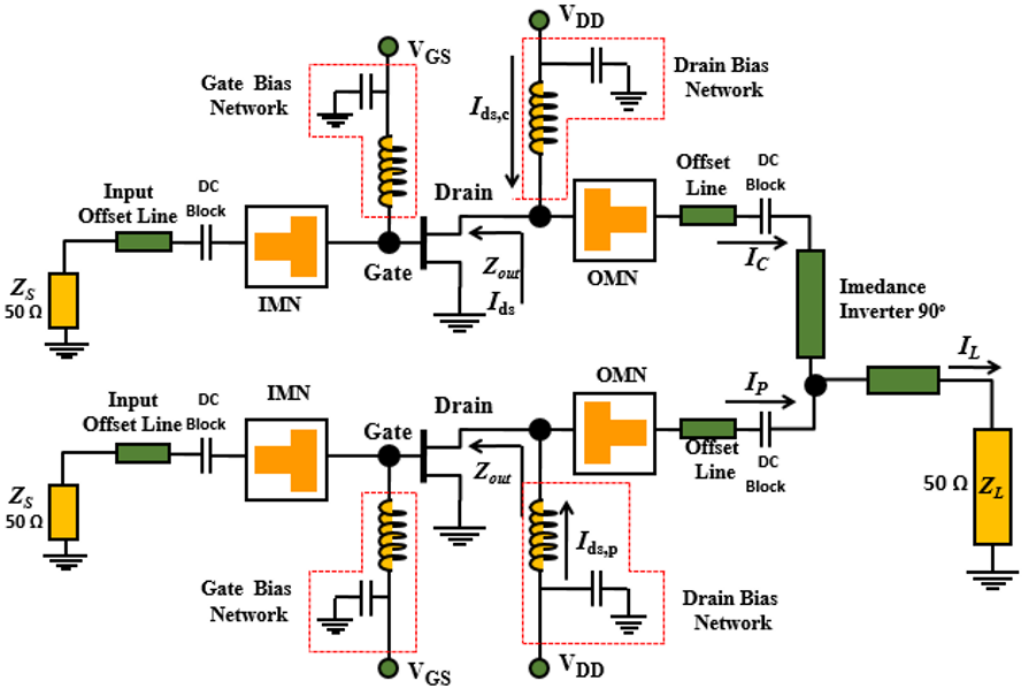


Figure 5.4: Circuit topology of dual-input Doherty power amplifier.

5.3 Circuit design methodology

In this section, the adopted design approach of a single- and dual-input DPA for wide bandwidth is presented. In the first step, basic design parameters such as design frequency, active devices, desired frequency band and optimum load impedance of the selected active device are determined. The optimum impedances comes from the load-pull data of the active devices under deep Class-AB bias conditions for carrier PA and in Class-C for peaking PA for each frequency in the required bandwidth. The optimum impedance is normally an average value of the load-pull results over the desired band.

In the second step, a wideband matching network from optimum impedance of selected device to load impedance is designed for carrier and peaking amplifiers. The designed OMN of carrier should be capable to provide the desired bandwidth and follow the impedance variation trend from low- to high-power mode. After that by using wideband OMN, the carrier PA is designed and optimized to provide at least 50% drain efficiency at 6 dB back-off output power throughout the band.

In the third step, a wideband input matching network for both power amplifiers, input splitter and output combiner network are designed. Then, the impedance inverter length and characteristic impedance is adjusted for best performance. The phase delay line is also inserted at the input side of peaking amplifier for perfect 90^{o} difference at the drain terminal of both the active devices.

In the final step, all the sub-circuits are combined into one circuit for the final optimization for best performance thought out the desired band. Before the implementation, EM simulations are also necessary for the reliability study and check the robustness of the design to ensure first-pass design.

5.4 Doherty PA designs example from 3.1 to 3.7 GHz

This section provides a practical design example for wideband DPA in the 3.5 GHz frequency band based on the design approach explained in the previous section. The selected frequency range is from 3.1 to 3.7 GHz. Designs of these power amplifiers started with a set of specifications and device selection. The two 10 W GaN HEMT transistor from Cree (CGH40010F) are selected for this particular DPA design and implementation. According to the datasheet of the selected device [59], the 10 W GaN HEMT transistor can work up to 6 GHz and

is also capable to provide a output power of 41 dBm for V_{DD} = 28 V at 3.5 GHz. After that, the selection of proper impedances in low and high power mode. The selected impedances at different node of the dual-DPA are presented in Figure 5.5. Special requirements of high efficiency in back-off output power, and wider bandwidth at higher frequency make DPA design very challenging.

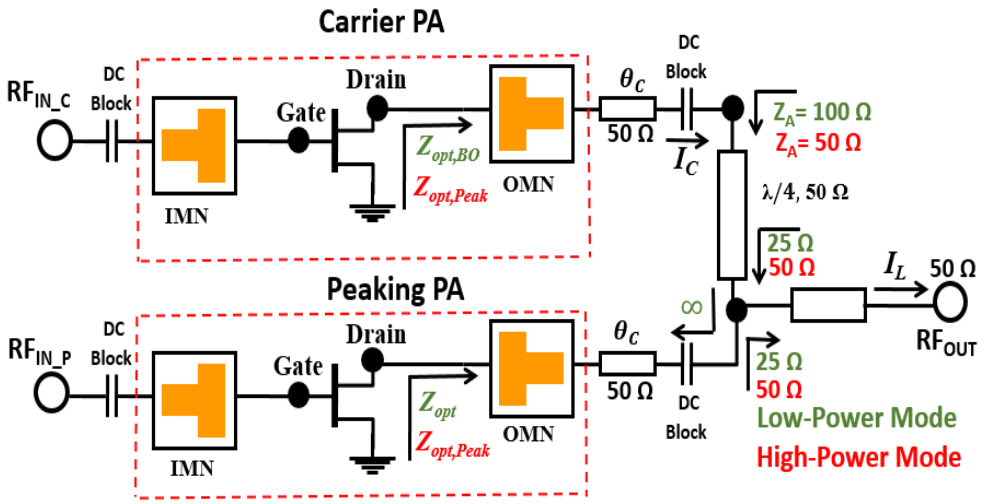


Figure 5.5: Block diagram of the proposed dual-input Doherty power amplifier.

5.4.1 Wideband carrier matching network

This section presents the design of wideband matching network for the carrier power amplifier. For optimum impedance extraction from the selected devices, load-pull simulations of the active devices under deep Class-AB bias conditions for each frequencies from 3.1 to 3.8 GHz with 100 MHz step are performed by using available load-pull simulation tools in ADS. All the load-pull simulations are on the condition of open harmonic loads. The extracted optimum impedances for the desired band are presented in Table 5.1 at saturation and the 6 dB back-off conditions. The range of optimal impedances for real component is from 10.1 to 19.5 Ω. The selected optimum impedance is 13.2+j*1.8 Ω, which is the average value of the load-pull results over the designed band.

The output-matching network (OMN) of the carrier PA should be capable to follow the impedance variation from low- to high-power mode (100-50 Ω at R_A point) throughout the desired bandwidth. The two-point matching technique provided in [85] presents a way for designing a matching network for changing

loads. For this PA design, low-pass T-matching configuration is used to realize the OMN for the carrier PA. Figure 5.6 shows the proposed low-order microstrip based OMN with their dimensions. The designed OMN is following the impedance variation trend from 100 to 50 Ω. The OMN simulated results at three-selected impedances (50 Ω, 75 Ω, and 100 Ω) are shown in Figure 5.7. The OMNs reflection losses are less than -10 dB and insertion losses are close to 0 dB. After the OMN design, the performance of carrier PA is optimized at 6 dB back-off, because at 6 dB back-off region peaking PA is in cold operating condition and it does not contribute to main output power. Only carrier PA is responsible of back-off drain efficiency and output power.

Table 5.1: Extracted optimum impedances for efficiency and output power from load-pull simulations in Class-AB bias conditions.

Frequency	**3.1 GHz**	**3.2 GHz**	**3.3 GHz**	**3.4 GHz**
Z_{OPT} at Sat. (Ω)	18.5+j1.5	16.5+j1.3	14.6+j1.3	12.9+j1.3
Z_{OPT} at 6 dB BO	19.5+j1.1	18.4+j1.0	17.8+j1.0	16.7+j0.9
Frequency	**3.5 GHz**	**3.6 GHz**	**3.7 GHz**	**3.8 GHz**
Z_{OPT} at Sat. (Ω)	11.8+j1.2	11.4+1.2	11.1+j1.2	10.1+j1.2
Z_{OPT} at 6 dB BO	15.4+j0.8	14.8.3+j0.8	12.4+j0.8	11.4+j0.8

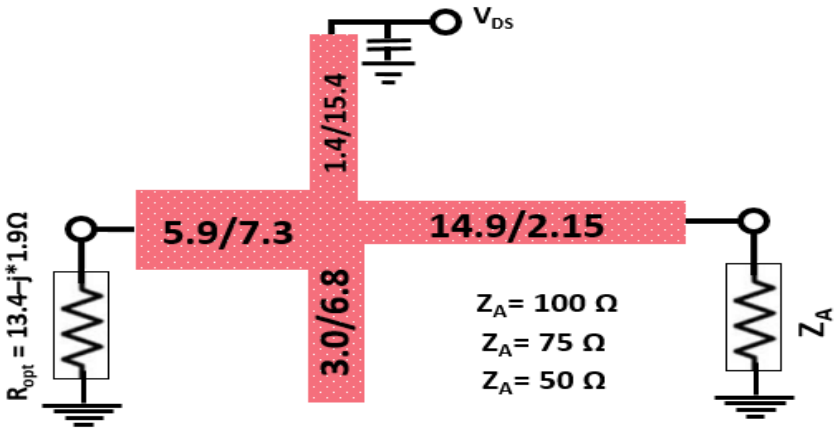


Figure 5.6: Synthesized output matching networks of peaking amplifier simulated on an Er = 2.33 microstrip substrate with a thickness of 0.79 mm. All dimensions are in millimeters.

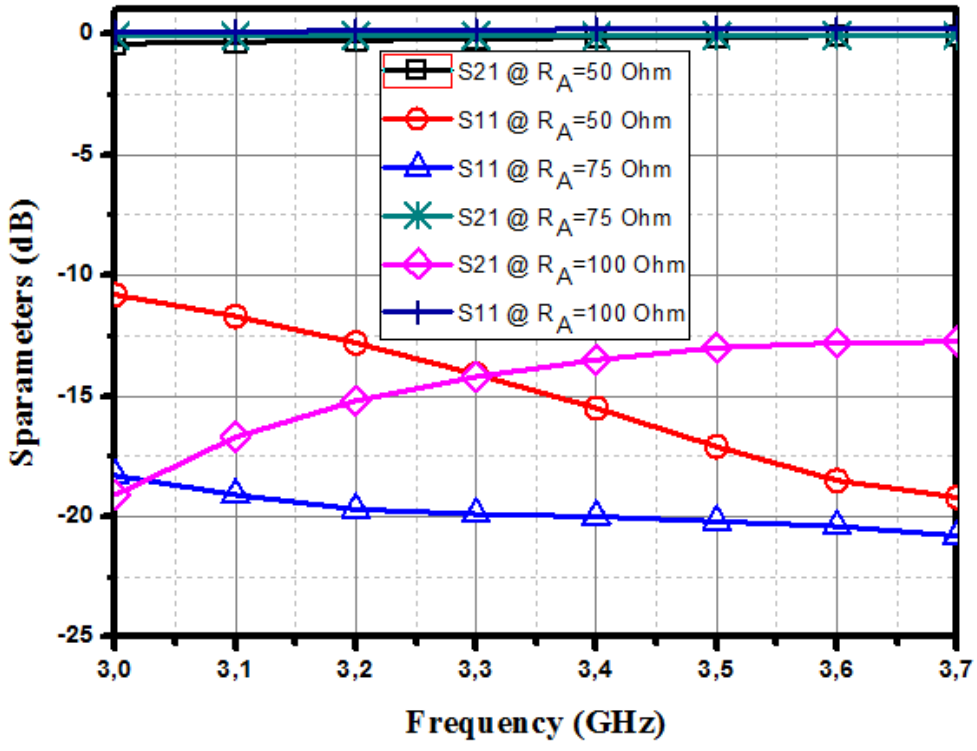


Figure 5.7: Return and insertion losses of the proposed OMN of carrier PA.

5.4.2 Wideband peaking matching network

This section presents the wideband matching network for the peaking PA. For peaking OMN design similar procedure is adopted. In the first step, the optimum impedances are calculated from the load-pull simulations of the active devices under deep Class-C bias conditions for each of the frequencies from 3.1 to 3.8 GHz with 100 MHz step. All the load-pull simulations are on the condition of open harmonic loads. The extracted optimum impedances for the desired band are presented in Table 5.2 at saturation. The range of optimal impedances is from 9.1 to 17.8 Ω. The selected optimum impedance is 12.9+j*1.25 Ω, which is the average value of the load-pull results over the designed band.

Table 5.2: Extracted optimum impedances for efficiency and output power from load-pull simulation in Class-C bias conditions.

Frequency	**3.1 GHz**	**3.2 GHz**	**3.3 GHz**	**3.4 GHz**
Z_{OPT} at Sat. (Ω)	9.9-j2.5	12.5-j2.1	13.6-j2.0	14.9-j1.8
Frequency	**3.5 GHz**	**3.6 GHz**	**3.7 GHz**	**3.8 GHz**
Z_{OPT} at Sat. (Ω)	17.4-j0.8	17.8-j0.4	8.6-j0.2	9.1-j0.0

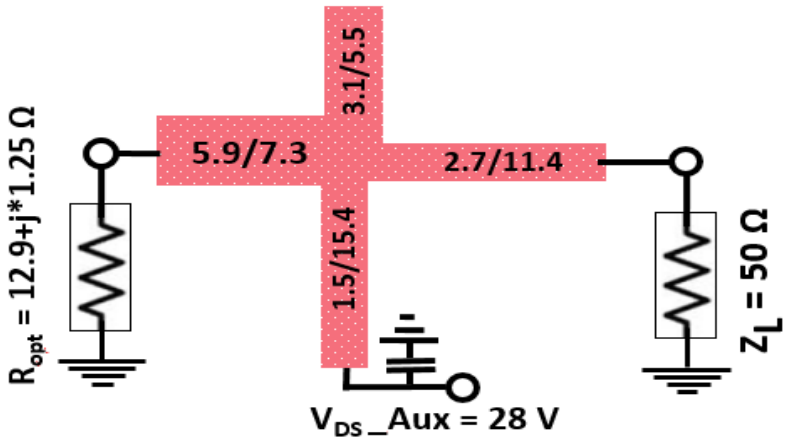


Figure 5.8: Synthesized output matching networks of peaking amplifier simulated on an Er = 2.33 microstrip substrate with a thickness of 0.79 mm. All dimensions are in millimeters.

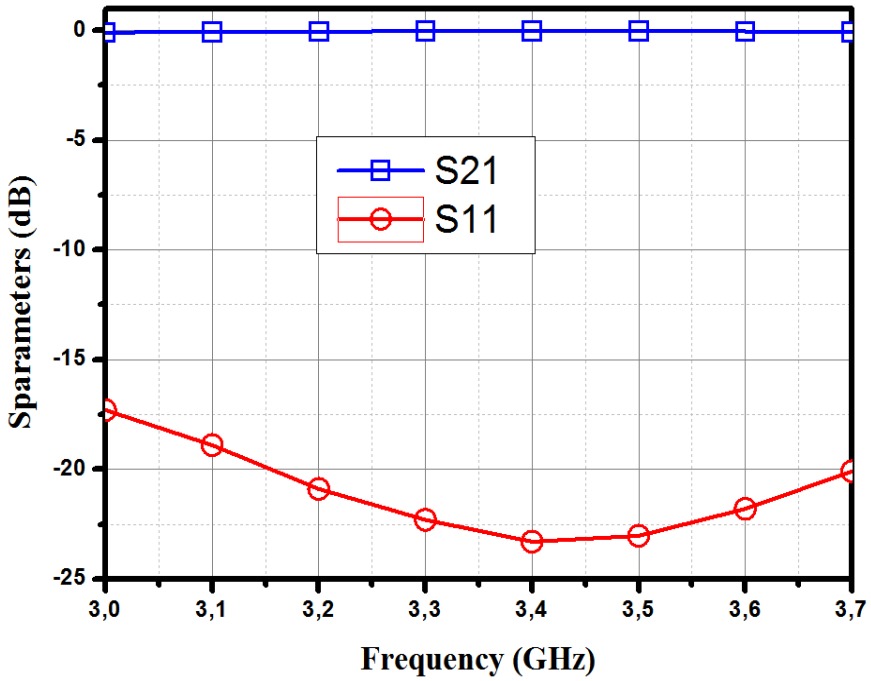


Figure 5.9: Return and insertion losses of the proposed OMN of peaking PA.

OMN design of peaking PA is relatively easy from carrier OMN, because there is no need to follow the impedance variation trend. The matching network has to convert reference impedance 50 Ω to optimum load impedance (R = 12.9 + j*1.25 Ω) for desired band. For carrier PAs low-pass T-configuration is exploited again for wide band output matching network, as it was used for carrier OMN. Figure 5.8 shows the peaking output matching network topology based on microstrip transmission lines with their crossholding dimensions. The OMNs reflection losses are less than -17 dB and insertion losses are close to 0 dB throughout the design band, as shown in Figure 5.9. After the OMN design, the performance of peaking PA is optimized at saturation.

5.4.3 Input matching network

The main goal of input matching network is to transform the optimum source impedance to system level impedance 50 Ω for maximum power transfer. Input matching network for both carrier and peaking amplifiers have same matching network. This particular IMN has to transform the input impedance from Zin = 6+j*6.5 Ω to 50 Ω. The input matching network has been designed using a *T*-configuration low pass matching lumped components then implemented with TLs, the same as the ones in the output network. The final layout of the proposed

designed network is shown in Figure 5.10. The result in Figure 5.11 of the final input matching network shows very good reflection and insertion losses throughout the band.

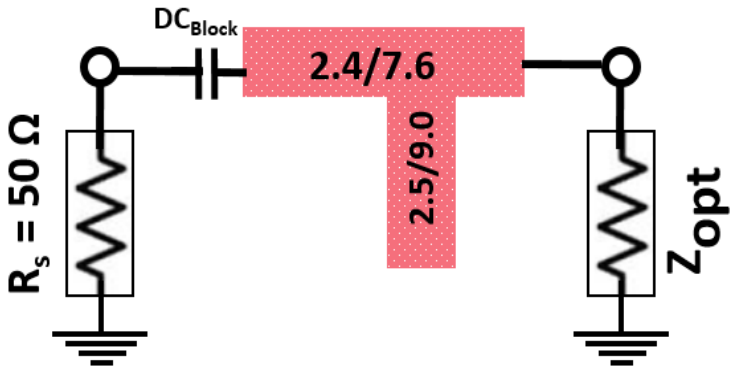


Figure 5.10: Layout of the input matching network of both PAs.

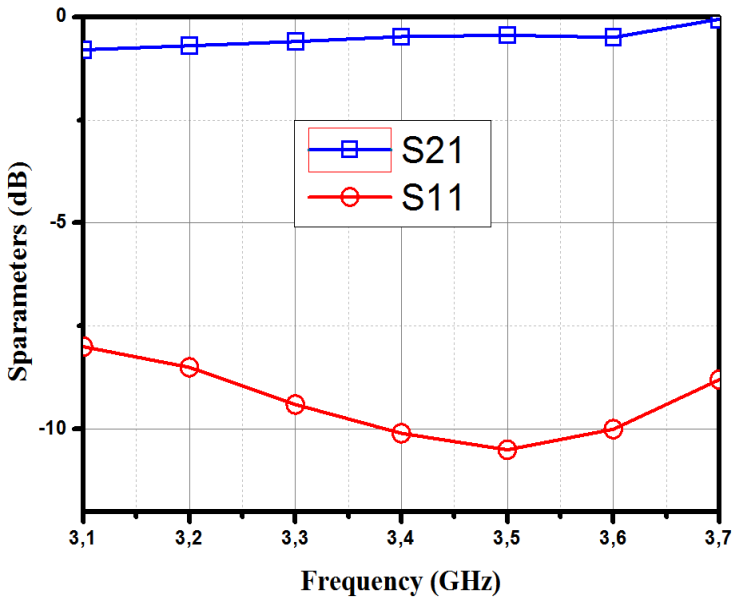


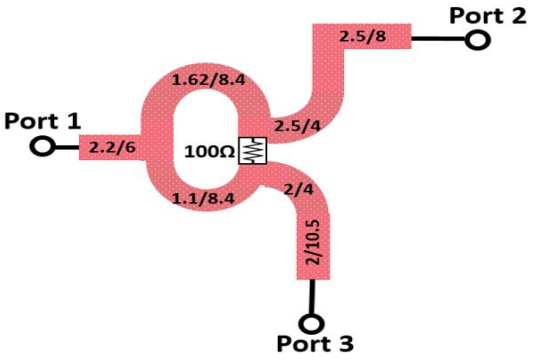
Figure 5.11: Return and insertion losses of the proposed IMN of both PAs.

Input matching network also includes the stability network as well. A 47 Ω series resistor and 82 pH inductor added in the gate bias to ensure low frequency

stability. Moreover, a parallel RC (R = 22 Ω and C = 4.7 pF) circuit in series to the transistor's gate is also used to ensure in and out of band stability of the power amplifier. Moreover, in the gate-bias network instead of using a conventional λ/4 line, a series resistor and inductor are used for reducing the gate current and absorb the noise. A set of bypass capacitors are also used [1 pF, 22 pF, 100 pf and 4.7 μF] to effectively terminate the envelope to short circuit.

5.3.5 Power dividing network

Uneven power divider is used at the input side of single-input PA. Power divider is designed for desired bandwidth. The conventional ring-structure topology is adopted due to its easy implementation and small size. The design goal is to determine the optimum values of characteristics impedances of λ/4 transmission lines of the power divider to minimize the insertion losses and keep adequate reflections, at all ports, for the defined bandwidth. The isolation between outputs ports of a power divider primarily depend upon the values of isolation resistors. A 100 Ω isolation resistor is used between port 2 and 3 for optimum isolation performance for wideband operation from 3.0 to 4.0 GHz. The Z_0 in the circuit represents the impedance terminating the input and output ports. Figure 2.12 shows the layout of the proposed power divider. The optimized characteristic impedances values of λ/4 transmission lines and input/output stubs are Z_C = 70.06 Ω, and Z_0 = 50 Ω, respectively. The simulated results of the power divider has return loss lower than -20 dB and insertion loss better than -3.2 dB for the frequency band 3.0-4.0 GHz. After the optimization, the width and length of transmission lines are calculated by using Line-calculator tool available in Keysight Advanced Design System (ADS). The phase difference between two output ports, insertion and reflection losses are shown in Figure 5.12.



(a)

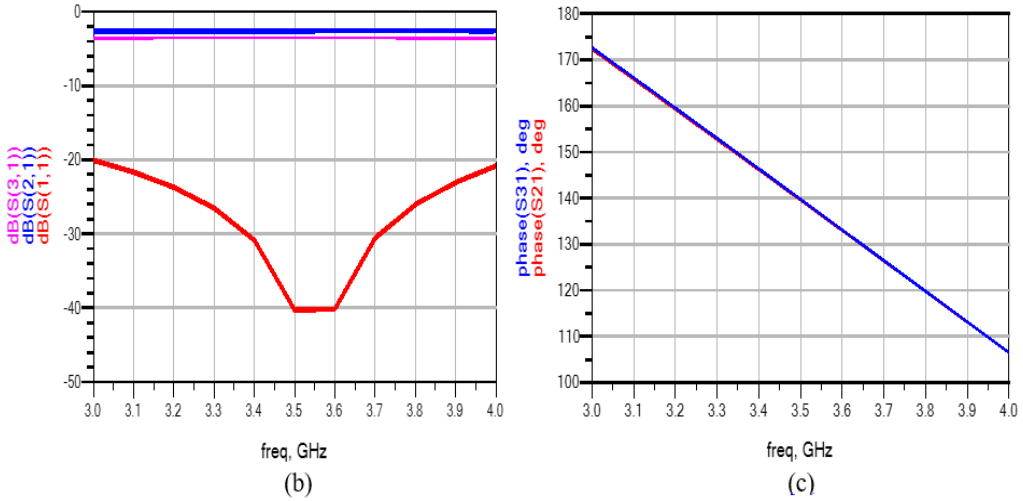


Figure 5.12: (a) Wilkinson power divider, (b) simulated insertion loss (S_{21}) and reflection loss (S_{11}), (b) phase difference between port 2 and 3.

In a broadband DPA design, the matching network is usually based on high-order topologies for addressing the high impedance transformation ratio in the designed band. High-order topologies are frequently build using filter circuit, which can presents reasonable band-pass and band-stop characteristics with high impedance ratio transformation as well. In our proposed design, the output-matching network is designed using low order topologies. The λ/4 impedance inverter converts the recombination node impedance to (25 Ω to 100 Ω) load matching impedance. A quarter-wave transmission line is used and optimized for best bandwidth performance. The optimized impedances values of λ/4 transmission lines is $Z_0 = 48$ Ω.

The 90^o transmission lines is used at the input of peaking amplifier for introducing perfect 90 degree phase difference at the drain of both active devices. It was also assured that the phase difference at the recombination node as close to zero, or as minimum as possible throughout the desired band for good load modulation. The output-combining network of the 3.5 GHz Doherty power amplifier was designed using transmission lines. Figure 5.13 (b) shows the simulated phase difference, which is approximately zero. Finally, the output impedance transformer is also designed by using a quarter-wavelength transformer. Impedance at the recombination node is approximately 25 Ω and the system impedance is 50 Ω. As a result, an impedance transformer is required to convert this impedance. A quarter-wavelength transformer is used to convert the

recombination node impedance (R_{com}) to system level impedance (50 Ω). The calculated characteristics impedance of the λ/4 (Z_T) is given below

$$Z_T = \sqrt{50\Omega \cdot 25\Omega} = 35.4\Omega$$

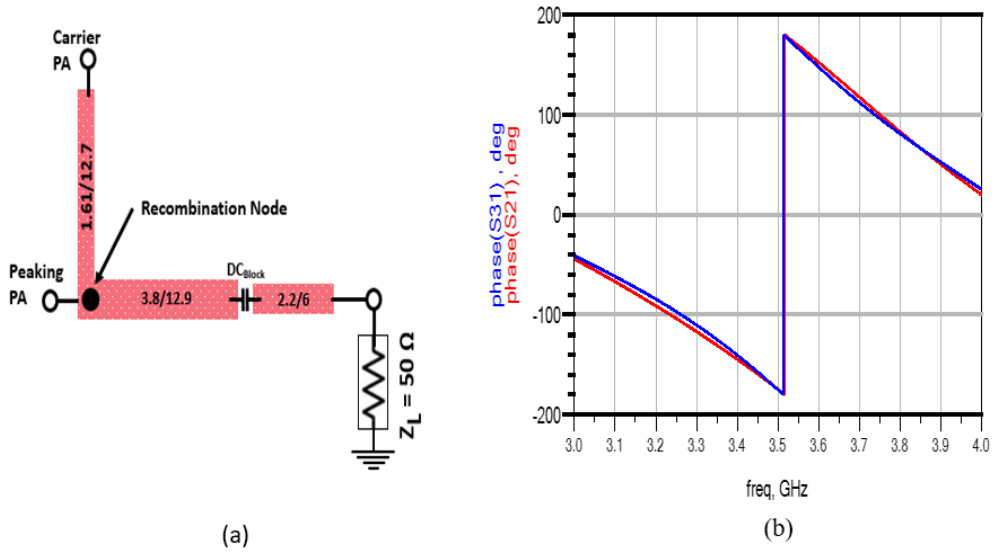
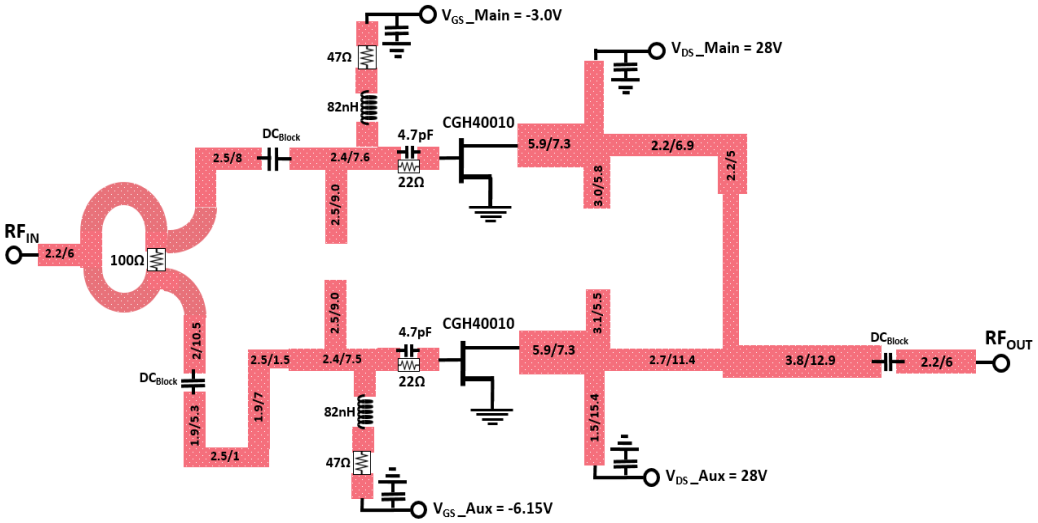


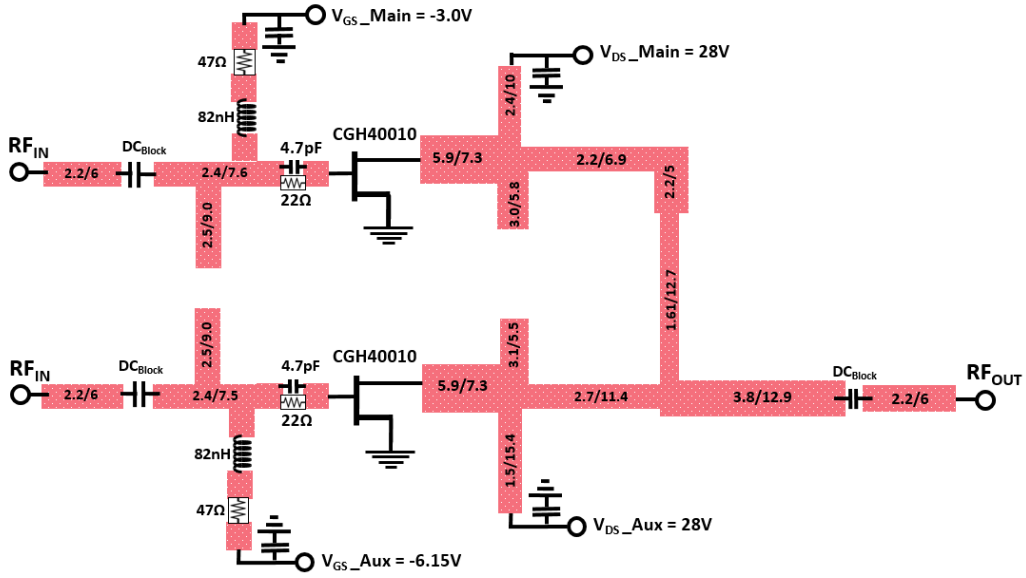
Figure 5.13: (a) Output combining network, and (b) simulated phase at the recombination node.

5.5 Final design

Eventually, all the sub-circuits are combined into the main circuit and final optimization for best large-signal performance. The chosen laminate is Duriod 5850 with thickness of 0.79 mm and relative dielectric constant of 2.33. The synthesized biasing and matching networks are implemented using transmission lines (detail circuit diagrams in ADS are given in appendix C). The key difference between the two proposed circuits is the power divider. In the last step of simulation and for verification purpose, an electromagnetic simulation has been performed for the distributed networks and the complete DPA. The details layout of the proposed DPAs are given in Figurer 5.14.



(a)



(b)

Figure 5.14: Final layouts of the proposed (a) single-input DPA and (b) dual-input DPA.

5.6 Small-signal gain

This section will presents the simulated and measured performance of the proposed Doherty power amplifiers in terms of small-signal gain, drain efficiency, gain, output power, and bandwidth. Figure 5.15 shows the simulated small-signal performance of the DPA biased at V_{DS} = 28 V and I_{DS} = 68 mA. It is important to note that the measured small-signal gain is due to the main power amplifier, while peaking power amplifier is in the off-state in this bias point. As it can be seen from Figure 5.18, an approximately constant small-signal gain in excess of 9.2 dB is maintained over a 700 MHz bandwidth.

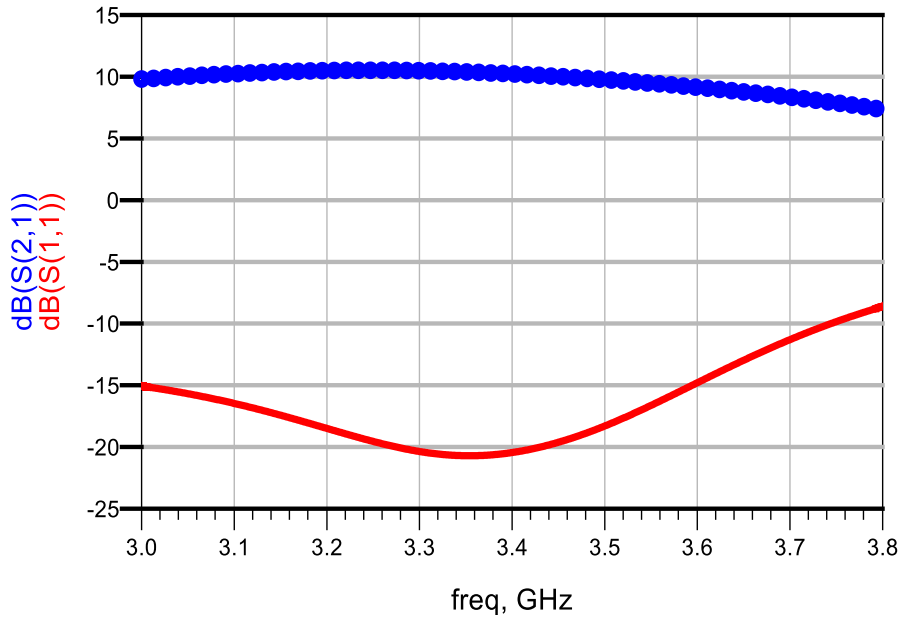
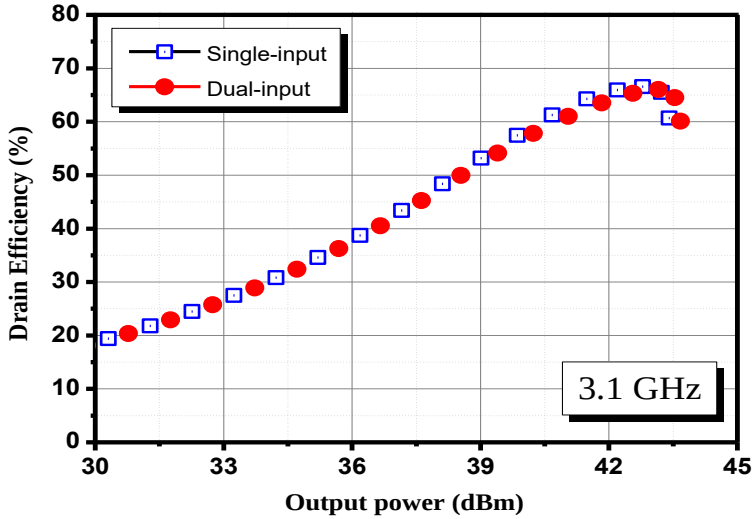


Figure 5.15: Simulated S_{21} (blue line with square mark) small-signal gain of the proposed DPA and input return loss S_{11}.

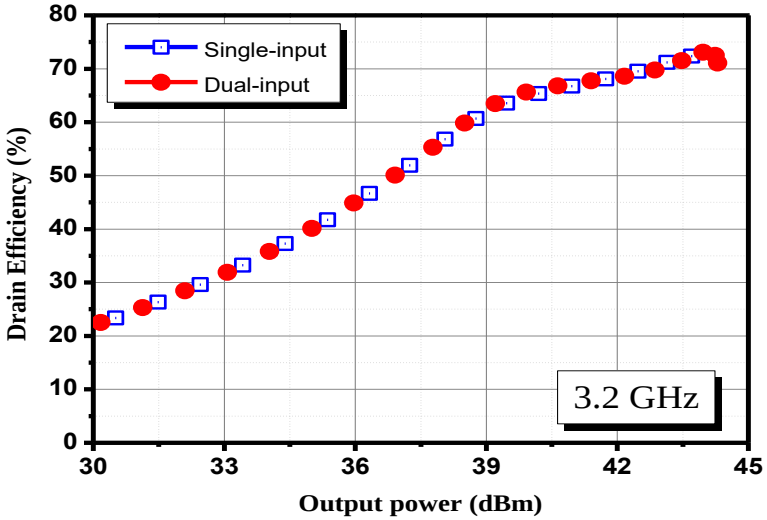
5.7 Single-tone power sweep

Single-tone large-signal characterizations are carried out in order to establish the proposed DPA performance at different input power level. The simulated results of DPA over the designed bandwidth with 100 MHz spacing are recorded, when it is biased at V_{DS} = 28 V and I_{DS} = 68 mA. In single-tone power sweep simulated drain efficiency with respect to output power at each frequency are plotted in Figure 5.16 (a) to (f). The input power is swept from 20 to 37 dBm. Simulated results demonstrate that the single-input Doherty power amplifier

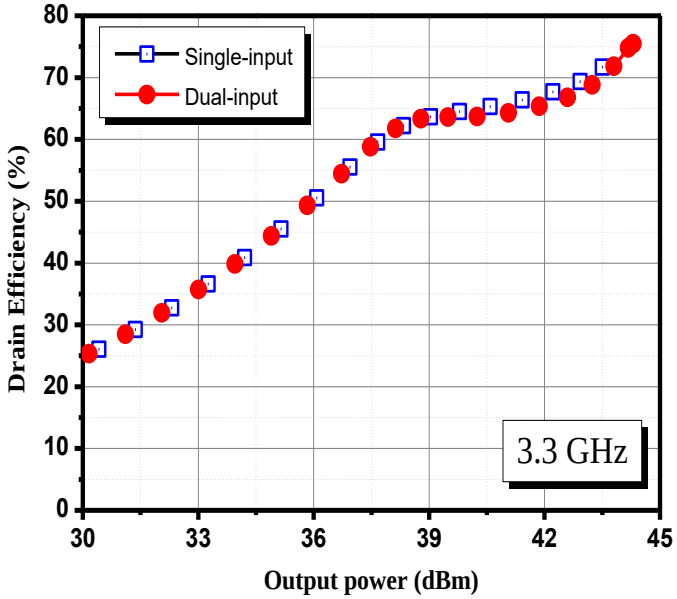
exhibited a peak drain efficiency (DE) of higher than 63% and at 6 dB back-off efficiency higher than 44% for the frequency range of 3.1 to 3.7 GHz. The dual-input Doherty power amplifier exhibited a drain efficiency (DE) higher than 60% and at 6 dB back-off efficiency higher than 40% for the frequency range of 3.0 to 3.7 GHz.



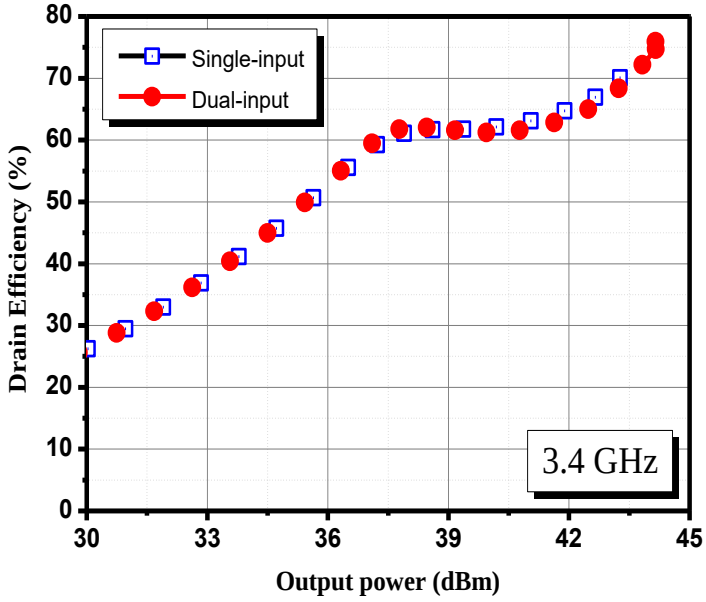
(a)



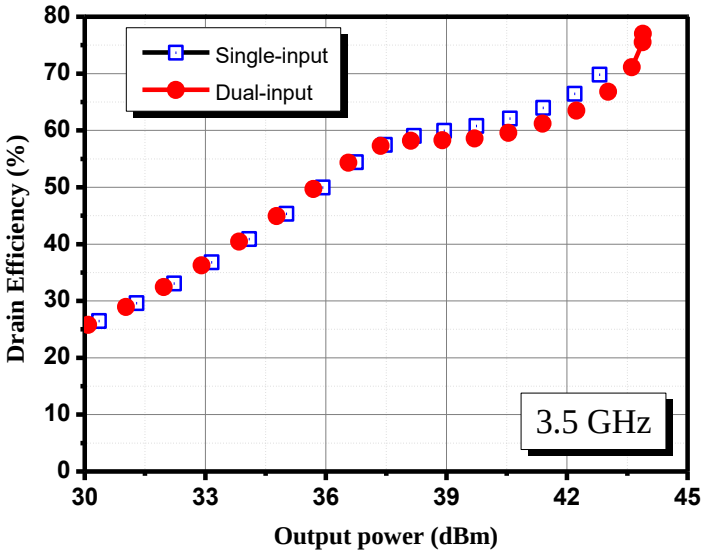
(b)


Single-input
Dual-input
3.3 GHz
Drain Efficiency (%)
Output power (dBm)
0
10
20
30
40
50
60
70
80
30
33
36
39
42
45

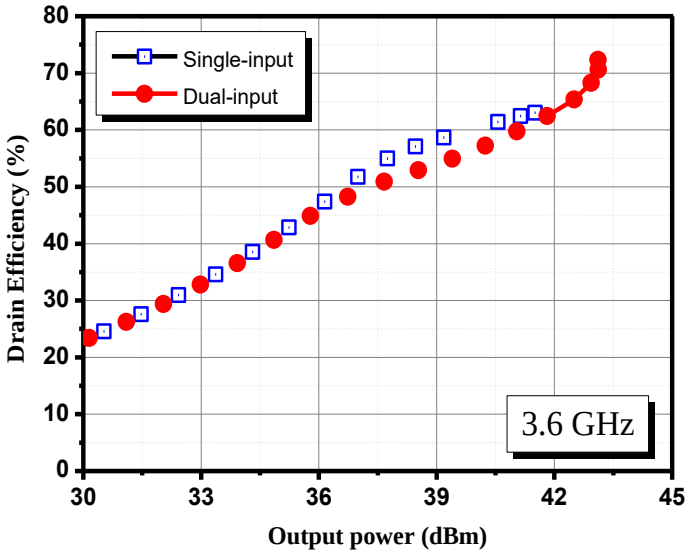
(c)


Single-input
Dual-input
3.4 GHz
Drain Efficiency (%)
Output power (dBm)
0
10
20
30
40
50
60
70
80
30
33
36
39
42
45

(d)



(e)

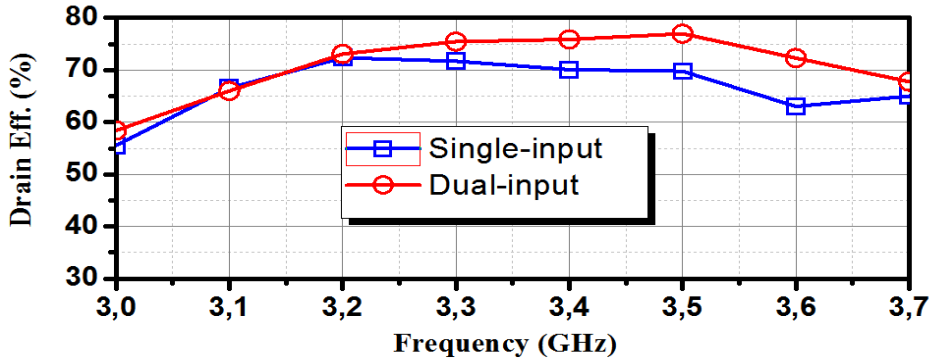


(f)

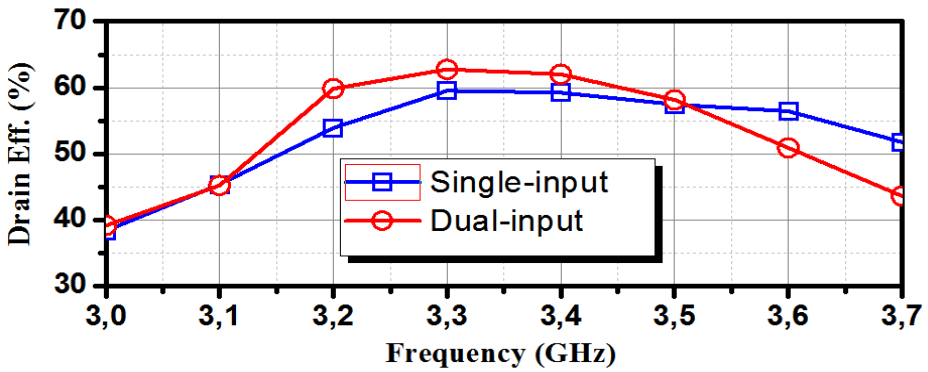
Figure 5.16: Simulated drain efficiency vs. output power for designed bandwidth at the V_{DS} = 28 V and I_{DS} = 68 mA.

Finally, to know the bandwidth response of designed DPA, single-tone testing has been performed from 3.0 to 3.7 GHz with spacing of 100 MHz. The simulated

parameters such as output power, gain at the 6 dB back-off, gain at saturation and output power are plotted in Figure 5.16, from 3.0 to 3.7 GHz. The simulated data show, a peak gain of 12 dB is revealed at 3.3 GHz with an output power of 44 dBm and 10 dB of gain at the 6 dB back-off for dual-input DPA. Moreover, PA maintain a saturated output power higher than 43 dBm and gain peak gain higher than 10 dB over the whole frequency band, as depicted in Figure 5.17. Single-input DPA showed comparatively lower performance in terms of drain efficiency, gain and saturated output power. In addition to this, the dual-input DPA provides more degree of freedom to overcoming the limitations of power-dependent phase imbalance and phase compensation at the input of the peaking amplifier; however, it requires additional input circuitry for complex input signal and it is not easy to be characterize too. Table 5.3 compares the performance of the present designs and of other published works on state-of-the-art DPAs in the 3.5 GHz frequency band. The simulated performance of the proposed PAs have better efficiency comparable to the other PAs while achieving a wider bandwidth.



(a)



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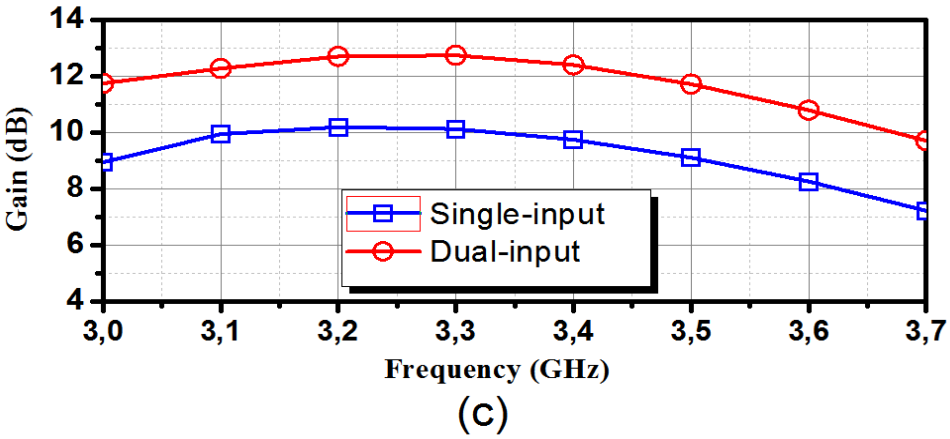

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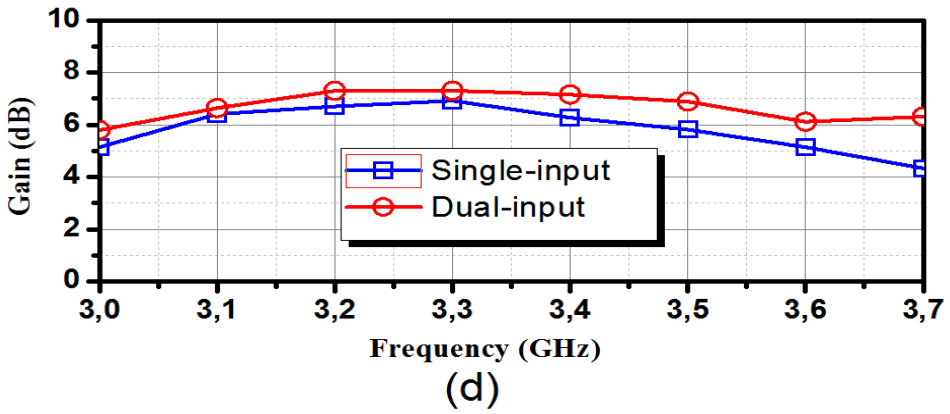

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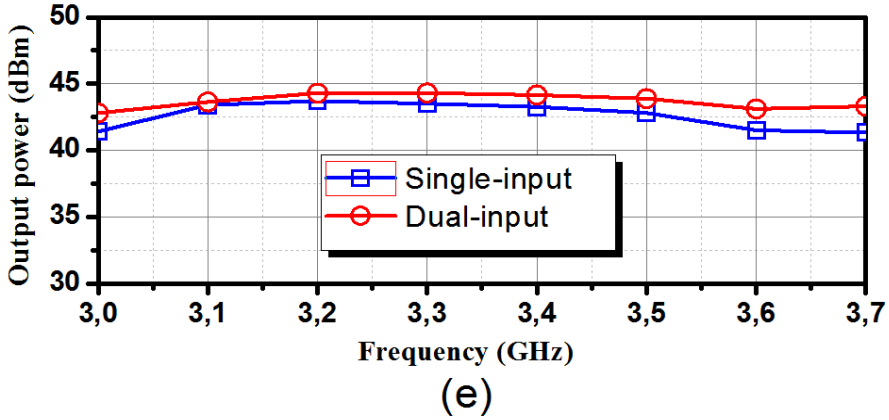


(e)

Figure 5.17: Simulated output power, drain efficiency, and gain versus frequency for the both PAs under optimum input power conditions.

5.8 Comparison with other publication

Finally, a comparison between the recently published broadband DPAs in the 3.5 GHz frequency band and state-of-the-art proposed DPA is made, as shown in Table 5.3. The designed PA has high back-off and saturated drain efficiency comparable to the other PAs. The power utilization factor is also very good. The simulated results stated that, the implemented DPA has higher fractional bandwidth compare to the other published results.

Table 5.3: Performance compression of the proposed DPAs with state-of-the Doherty power amplifier in the 3.5 GHz frequency band.

Ref.	**Freq. (GHz)**	**P_{sat} (dBm)**	**DE @ Sat (%)**	**DE @ 6 dB OPBO (%)**	**Gain (dB)**
[81]	3-3.6	43-44	55-66	38-56	8-11
[82]	3.53	46.3	60	44	11.2
[83]	3.4–3.5	46	67	40	N/A
[84]	3.3-3.6	48.5-49.5	40.9-55.1	50-58	14.4-14.9
[85]	3.4–3.6	49.2	60-61	48–52	12.3
T.W(1)	**3.1-3.5**	**42.9-43.7**	**63-72.4**	**44-60**	**9.1-10.2**
T.W(2)	**3.0-3.7**	**43-44.4**	**60-77**	**40-62**	**10-12.8**

5.9 Summary

In summary, two new designs of Doherty power amplifiers are presented for LTE application in the 3.5 GHz frequency band. A comprehensive comparison was made between single- and dual-input DPA. Before the implementation, extensive simulations were performed in ADS using accurate device model and component's model to achieve best back-off and saturated drain efficiency for the desired bandwidth. In the simulated results, the dual-input DPA achieves higher performance compared to single-input DPA, but at the cost of linearity. The simulation results verify that DPAs are suitable candidate for a LTE downlink communication signal over the frequency range from 3.1-3.6 GHz.

Chapter 6

Ultra-Wideband Doherty Power Amplifier

6.1 Introduction

In the previous chapter, the focus was on maintaining constant efficiency up to the 6 dB back-off for LTE 3.5 GHz band. However, the operational bandwidth of the proposed DPA is only 600 MHz. In this chapter, the key factors that contribute to the limited bandwidth of the DPA are described. A novel design methodology for the ultra-wide band DPA is presented. The proposed DPA can be experimentally exploited for base-station application over the frequency range of 1.15-2.4 GHz. The main goal of this design is to achieve a drain efficiency more than 40% at the 6 dB back-off for the whole frequency band. A prototype of proposed DPA is implemented using a hybrid technology for design validation. The realized DPA is characterized with CW and modulated input signals for the desired frequency band.

6.2 Bandwidth limitation factors of conventional DPA

Up to now, a lot of work has been presented on single-band DPAs [86]-[100]. However, this does not meet the requirements of multiple standards of a modern future radio base-station, as discussed in section 1.2 chapter 1. Therefore, much effort has been made to extend the bandwidth of the DPA by using various matching networks [101] or by exploiting wideband matching networks [97],

[102-107]. Moreover, many investigational outcomes have shown that the acquired bandwidths are not yet broad enough to cover many bands simultaneously and to reduce the time-to-market of new wireless standards. In addition to this, one more drawback is that, broadband DPA dose not always have the optimal performances throughout the design band. Consequently, it helps to lead rapid performance degradation of a DPA, when compared to the designed frequency performance. In the following sub-sections, some of the important bandwidth limitation factors of a conventional DPA are described.

6.2.1 Influence of the impedance inverter

The basic building blocks of a conventional Doherty power amplifier are presented in Figure 6.1. The DPA comprises of two power amplifiers, input splitting and a λ/4 impedance inverter for prefect load modulation. It is presented in [94] that a λ/4 transmission line impedance inverter has been often identified as the bottleneck for the bandwidth extension of a conventional DPA design and implementation, due to its inherent limited bandwidth operation.

6.2.2 High impedance transformation ratio

Another bandwidth limitation factor in a conventional Doherty amplifier configuration is the large impedance transformation ratio required at the R_A point (depicted in Figure 6.1). Generally, the impedance at R_A point changes from Z_0 to $Z_0/2$ (100 to 50 Ω). Even, if we assume impedance inverter can work for any frequency, still it is not easy to transfer this large impedance variation throughout broadband matching network. There are some commonly available filter topologies such as stepped transmission-line (TL) impedance, multistage band-pass matching network transformers and two kinds of multistage filter networks to realize the broadband matching networks [110]. These generalized broadband matching networks simply cannot overcome the bandwidth extension limitation of the conventional DPA.

6.2.3 Quasi-open-circuit requirements

In low power DPA operation, the peaking power amplifier is in the off-state up to the 6 dB back-off level. It is described in [94] that the Z_p impedance of peaking PA should be infinite, Z_p is the impedance when looking back to the transistor from the output side of the transistor in off state, as shown in Figure 6.1. Normally on the Smith chart Z_p would be close to the boundary of the unit circle

and the phase of the Z_p should be inside the ± 45 limit to satisfy the quasi-open-circuit conditions for minimum leaking current through the peaking transistor. Presences of any physical component except matching network in the OMN of the peaking PA leads to positive phase dispersion in Z_P because of phase dispersion. Furthermore, it limit the bandwidth of the standard DPA. Therefore, any physical component except OMN should not be present in between the load modulation point and peaking power amplifier.

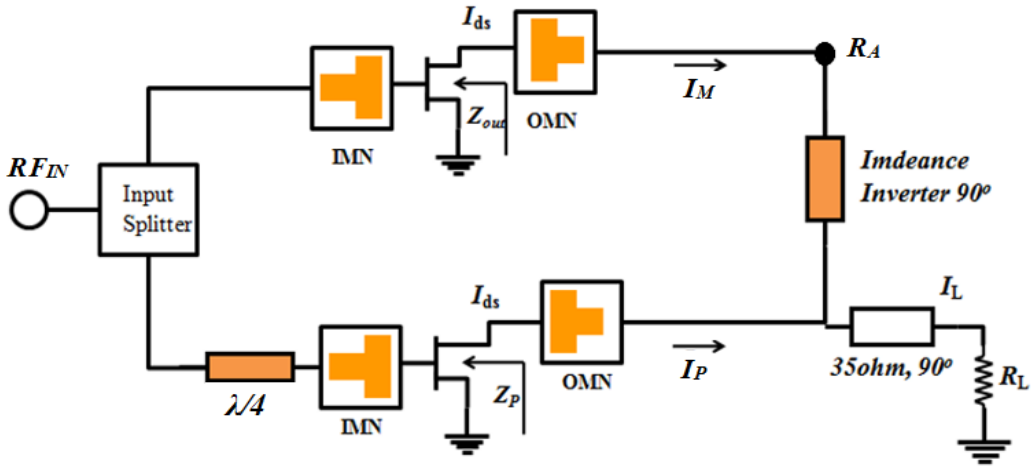


Figure 6.1: Basic building blocks of conventional Doherty power amplifier.

In order to overcome all of these limitations, many dual-band and wideband DPAs are proposed in the literature, which are a superior contender due to the flexibility of choosing the operating bands. Some recently published work on dual-band operation are in [107-109]. However, they present architectural overviews without any comprehensive or general design methodology. In the following section, a detailed design approach for the ultra-wideband DPA design is presented.

6.3 A novel Doherty power amplifier

In order to overcome the bandwidth limitation of conventional DPA, in the new proposed DPA all the three bandwidth limitation factors described in previous section are addressed for bandwidth extension. The post-matching architecture is exploited instead of the conventional architecture to eliminate the need of impedance inverter form the circuit. The detail of post-matching architecture is given in [110]. For this particular architecture, it is possible to utilize the high-order matching network topologies for bandwidth extension. A

DPA based on this architecture has reported 40% fractional bandwidth [110]. The post-matching networks topology reduce impedance transformation between the optimum impedance node and load modulation point node. Impedances at the load modulation point can be found out by using the following equations

For carrier,

$$Z_{Carrier} = Z_{load} \times \frac{I_{out}}{I_{carrier}} = Z_{load} \times \frac{I_{carrier} + I_{peaking}}{I_{Carrier}} \quad (6.1)$$

For peaking,

$$Z_{peaking} = Z_{load} \times \frac{I_{out}}{I_{carrier}} = Z_{load} \times \frac{I_{carrier} + I_{peaking}}{I_{Carrier}} \quad (6.2)$$

In above equations, I_{out} is the output current from the post-matching network, $I_{carrier}$ is the carrier amplifier current and $I_{peaking}$ is the peaking PA current in peaking branch. Same as to the standard DPA, the carrier PA active device is biased in deep Class-AB operation and peaking PA active device biased in Class-C operation. For a symmetrical DPA operation, peaking current is zero at the back-off level and the peaking current equal to carrier amplifier current at saturation.

For carrier,

$$Z_{Carrier} = \begin{cases} 2Z_L & @\ Saturation \\ Z_L & @\ OBO \end{cases} \quad (6.3)$$

For peaking,

$$Z_{Peaking} = \begin{cases} 2Z_L & @\ Saturation \\ \infty & @\ OBO \end{cases} \quad (6.4)$$

In the saturation region, both active devices must produce equal amount of power for perfect load modulation, similar to a convectional DPA. Moreover, both the impedance inverters of the carrier and peaking PA should provide the required impedance transformation and perfect matching for optimum performance. For ideal operation at the 6 dB back-off point, suitable impedance that can push

carrier PA into the saturate is required. For this condition, optimum impedance of a carrier PA is decided to be at 3 dB lower than the saturation point. The design procedure is given in next section in detail.

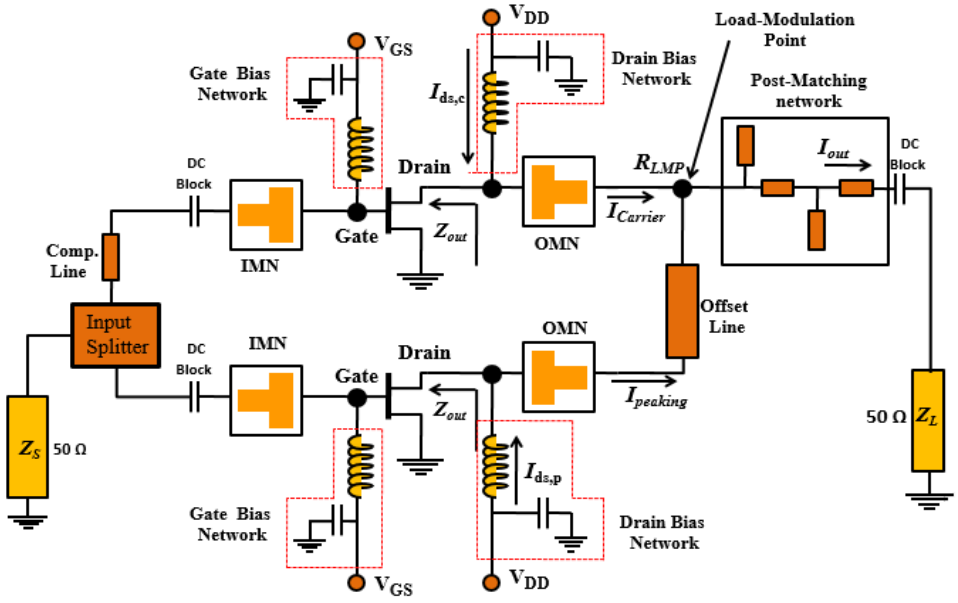


Figure 6.2: Circuit topology of proposed Doherty power amplifier.

Moreover, in order to reduce the impedance transformation ratio between load modulation point (LMP) and the optimum impedance of the active device, another step is considered in design, which leads to the higher operational bandwidth. In this run, LPM impedance (R_{LMP}) is selected to be equal to the optimum load impedance of the carrier device, which can be found from the load-pull data.

Finally, in order to have a quasi-open-circuit condition for minimizing the leaking current through the peaking transistor during low input power operation, an off-set line in the output of peaking PA is used. For a perfect open circuit requirement for wide bandwidth, a compensation line at the input of carrier PA for phase adjustment is also used. In this part, the selection of impedance and length of the off-set line is a key to adjust the quasi-open-circuit conditions for the desired bandwidth. The length of the offset line could be from minimum from 60^o to 110^o, dependency on the bandwidth and performance requirements of the DPA. The impedance of the off-set line depends on the selected impedance of LMP and extracted optimum impedance of the peaking PA. Normally, it is twice the load modulation point impedance, its value depends upon the bandwidth and performance requirements. Moreover, this design technique also allows a great

degree of freedom for optimization of each section separately for best performance, which is not possible in a conventional DPA due to strict requirements of the impedance transformer and large impedance variation.

A diagram of the proposed Doherty power amplifier is shown in Figure 6.2. The proposed DPA consists of two power amplifiers main and peaking. A post-matching network is used for a wideband impedance matching for both PA, from the 50 Ω reference impedance to LPM impedance. A power divider is used for power splitting at the input. The same wideband input matching network for both PA is designed for input matching. Since there is no need of a quarter-wavelength impedance inverter in this proposed circuit, as a result, wide bandwidth design is possible.

6.3.1 Advantages of the proposed design methodology

In order to give a clear picture, the key differences between the conventional design methodology and the proposed design methodology for Doherty amplifier are highlighted in Table 6.1. The main advantage of this design approach is that it is possible to design extended bandwidth DPA by using the same number of active devices and to control the DPA bandwidth form 30% to 66%. There is no more need of using an impedance inverter in this topology. Beside this, there are other advantages as well. For instance, as can be seen from the Table 6.1, the R_{opt} is equal to R_{LMP}, due to the zero impedance transformation ratio; it is simple to design an OMN.

Table 6.1: Compression of conventional and proposed design methodology.

S/N	Conventional PA	Proposed PA
Z_T	R_{opt}	$R_{opt,avg}$
R_L at back-off	R_A (100 Ω)	$R_{LMP} = R_{opt}$
R_L at saturation	$R_A/2$ (50 Ω)	$R_{LMP} = 2R_{opt}$
Impedance inverter	Required	Not required
Active devices	Asymmetrical	Symmetrical
Drain bias	Symmetrical	Symmetrical
Complexity	Low	Medium
Bandwidth	Low	Very high

Moreover, the proposed methodology is based on symmetrical devices and equal drain bias is required for both PAs. Therefore, the advantage of using symmetrical devices over the asymmetrical devices is a higher output power. The disadvantage compared to conventional approach is due to the additional post-matching network circuitry.

6.4 Circuit design methodology

Based on the concept proposed in previous section, a basic design methodology for DPA bandwidth extension is described here in detail. The key steps are given below.

Step 1: The basic design parameters such as center frequency and optimum load impedance of the selected active device are determined. The optimum impedances come from the load-pull data of the active devices under deep Class-AB bias conditions for each frequency in the required bandwidth. The optimum impedance is normally an average value of the load-pull results over the designed band.

Step 2: The load modulation point impedance (R_{LMD}) is set equal to the average value of the optimum impedance (Ropt,avg). This leads to lower impedance transformation ratio between average optimum impedance and LMP impedance, even zero impedance transformation ratio is required in case of real component. For the lower impedance ratio is easy to design a wideband impedance inverting network. The low-order impedance network should be capable for impedance transformation.

Step 3: After that, a single-ended Class-AB carrier PA is designed with input reference impedance of 50 Ω and output reference impedance set equal to load modulation point impedance (R_{LMP}), estimated from the load-pull data at 3 dB back-off point. The designed carrier PA should be capable to provide more than 40% drain efficiency at 3 dB back-off output power throughout the designed band. The performance of carrier PA is optimized at 3 dB back-off, because at the 6 dB back-off region peaking PA is in off-state and it does not contribute to main output power. Only carrier PA is responsible for the 6 dB back-off drain efficiency and output power.

Step 4: Then, optimum impedances for peaking efficiency for peaking amplifier in Class-C bias conditions are extracted from load-pull simulation for each frequency in the required bandwidth. The average value of the load-pull results is taken over the designed band. An impedance inverter for peaking PA is designed based on low-order network for wideband form optimum impedance to $2R_{LMP}$.

Step 5: An offset-line with characteristic impedance of $2R_{LMP}$ is selected, if DPA is operating for 40% fractional bandwidth and 1.5 R_{LMP} for a higher bandwidth operation. Offset-line is required between the LMP and peaking inverter, in order to reduce the influence of output impedances of the peaking branch on the carrier matching. The selection of length and impedance of the offset line is adjusted for quasi-open-circuit conditions for desired bandwidth. A compensation line is also inserted at the input side of carrier amplifier for phase compensation shift occurred due to offset line.

Step 6: A post-matching network is designed based on a high-order network from R_{LMP} to 50 Ω load impedance. In addition to this, a power divider is also design for the required bandwidth.

Step 7: In the final step, all the sub-circuits are combined into the main circuit and the final optimization is performed for the best performance throughout the desired band. Before the implementation, electromagnetic (EM) simulations are also necessary for the reliability study and also to check the robustness of the design to ensure first-pass design.

In order to verify the proposed design methodology, two DPAs are designed in Keysight Advanced Design System (ADS) based on 10 W (CGH40010F) and 6 W (CGH40006P) Cree GaN HEMT devices. Both the designed DPAs showed expected bandwidth response. In the next section, the proposed design procedure is validated by the design and implementation of high efficiency DPA operating from 1.15 to 2.35 GHz.

6.5 Doherty PA design example from 1.15 to 2.35 GHz

This section provides a practical design example for ultra-wideband DPA based on the proposed design theory. The selected frequency range is from 1.15 to 2.3 GHz. The design of a power amplifier starts with a set of specification and the

selection of an appropriate device. Specially, the requirements of high linearity, efficiency, and wide bandwidth simultaneously make the DPA design more challenging. Two 10 W GaN HEMT transistors from Cree (CGH40010F) are selected for this particular DPA design and implementation. According to the datasheet of the elected device [25], the 10 W GaN HEMT transistor can work up to 6 GHz and is also capable of providing a output power of 41 dBm for V_{DD} = 28 V at 2.0 GHz.

6.5.1 Power dividing network

Before DPA design, two Wilkinson power dividers (WPD) are designed and implemented for desired bandwidth, one of them is published in "A miniaturized Wilkinson power divider for ultra-wide band operation" [111]. The other one is a conventional ring-structure power divider, adopted due to its easy implementation and small size. The design goal is to determine the optimum values of characteristic impedances of λ/4 transmission lines of the power divider to minimize the insertion losses and keep adequate reflections at all ports for the defined bandwidth. The isolation between output ports of a power divider primarily depend upon the values of isolation resistors. A 100 Ω isolation resistor is used between port 2 and 3 for an optimum isolation performance for the ultra-wideband operation from 1.1 to 3.0 GHz. The Z_0 in the circuit represents the impedance terminating the input and output ports. Figure 6.3 shows the simplified topology and photograph of the implemented power divider.

The optimized impedances values of λ/4 transmission lines and input/output stubs are Z_C = 70.06 Ω, and Z_0 = 48 Ω, respectively. The simulated results of the design power divider shows return loss lower than -14 dB and an insertion loss better than -3.2 dB for the frequency band 1.15-2.4 GHz. After the optimization, the width and length of transmission lines are calculated by using Line-calculator tool available in ADS. A Duriod 5850 printed circuit board (PCB) with a relative permittivity of 2.33 and 0.79 mm thick substrate is used to validate the design. The photograph of the realized splitter circuit is shown in Figure 6.4, which equally splits the input power into two output ports 2 and 3. The overall physical dimensions of the realized power divider are 15×15 mm^2. Finally, the scattering parameters are measured using a four port Vector Network Analyzer (VNA), calibrated using Ecal Kit [94].

The measured and simulated forward loss of the designed and fabricated power splitter is shown in Figure 6.4. The measured values of the forward loss for

both output ports (S_{21} and S_{31}) are within -3.3 dB for the desired bandwidth of Doherty PA operation. The measured value of insertion loss S_{21} and S_{31} are -3.1 dB at the design frequency of 2 GHz, this shows very good agreement with simulated insertion loss. The measured reflection loss (S_{11}) is lower than -23 dB at the design frequency and lower than -12 dB for the frequency range of 1.1-2.7 GHz, as can be seen from Figure 6.5.

The measured values of isolation (S_{32}) are better than 20 dB at 2 GHz and reflection loss at the output ports below than -10 dB for the entire band. Figure 6.6 shows the measured phase difference between both output parts, which is within ±0.5 degrees. This indicates a good in-phase performance throughout the band. A small difference in measured and simulation results is due to the substrate dielectric material losses, and a variation in length and width of the transmission lines during fabrication.

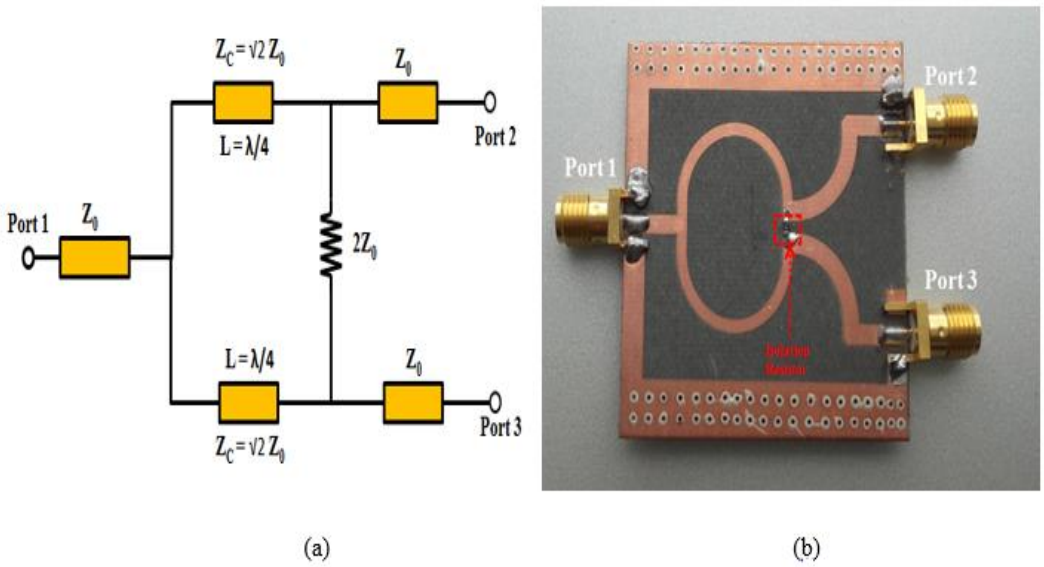


Figure 6.3: Wilkinson power divider (a) transmission line circuit and (b) photograph of the realized circuit.

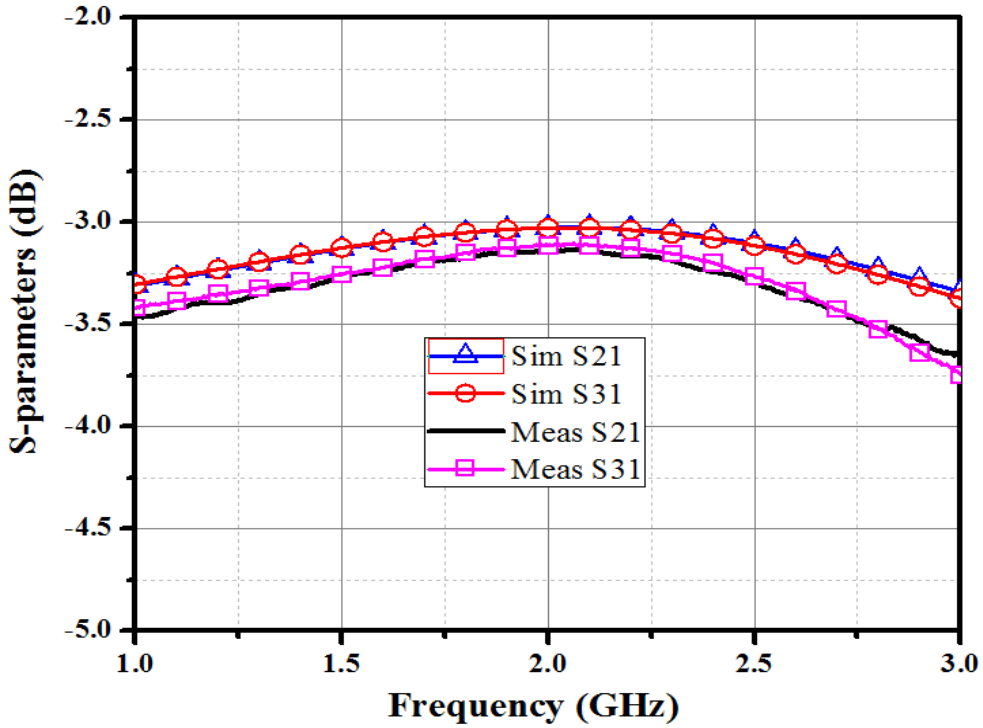


Figure 6.4: Measured and simulated insertion loss (S_{21}) of the ring structured Wilkinson power divider.

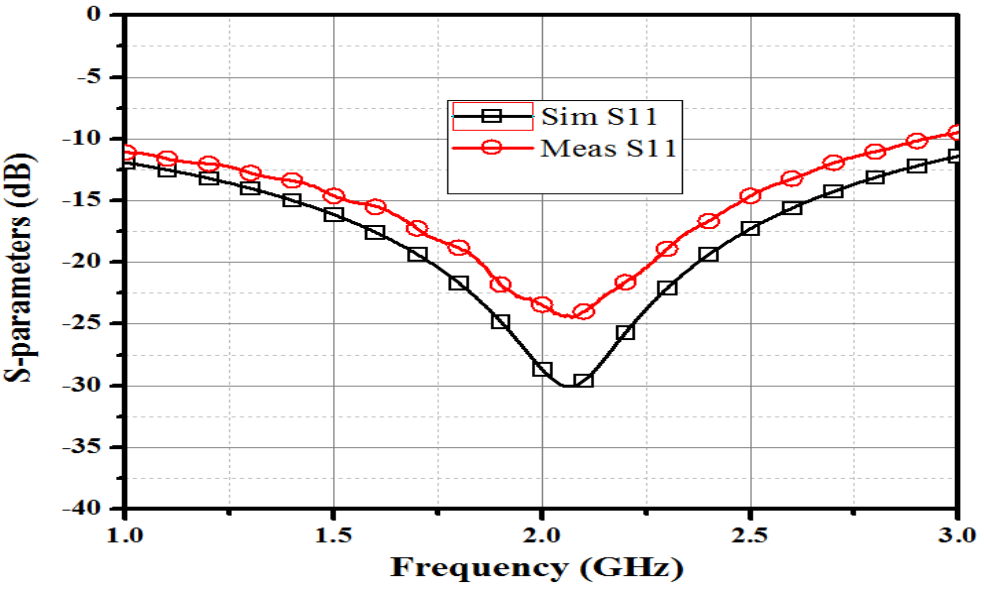


Figure 6.5: Measured and simulated reflection loss (S_{11}) of the ring structured Wilkinson power divider.

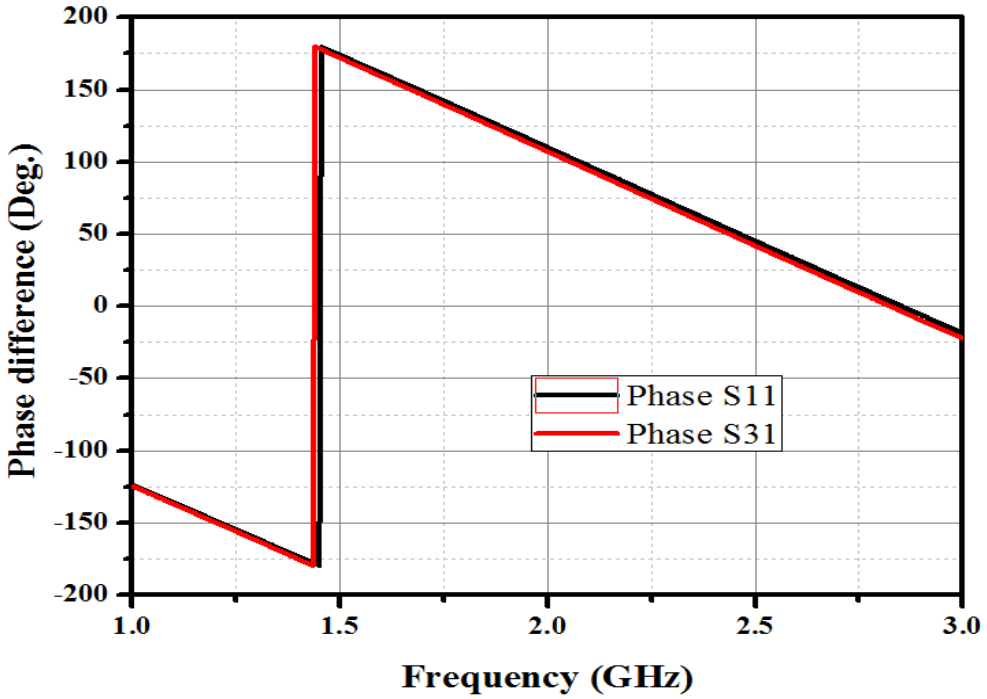


Figure 6.6: Measured phase difference in port 2 and 3 of the ring structured Wilkinson power divider.

6.5.2 Carrier and peaking impedance inverters

For the proposed DPA design, low-pass configuration isselected to realize the impedance inverters, both the peaking and carrier PA. A 70% fractional bandwidth from 1.15 to 2.35 GHz is set as the main target. In order to find the optimum impedance load and source-pull simulation was performed from 1.2 to 2.6 GHz for PAE and output power. Simulated load-pull optimum impedance for the whole band at saturation and 3 dB back-off point is shown in Table 6.2. The range of optimal impedances are from 15.3 to 23.4 Ω. Thus, average value are calculated from the optimum impedance, which is Ropt = 20 Ω. After that, the impedance value of the LMP is set equal to the average optimum impedance.

$$R_{LMP} = R_{OPT}$$

Table 6.2: Load-pull simulation for optimum efficiency and power at the 3 dB back-off, when biased with V_{GS} = -3.0 V.

Frequency	**1.2 GHz**	**1.3 GHz**	**1.4 GHz**	**1.5GHz**	**1.6 GHz**
Z_{OPT} (Ω) Saturation	23.4+j22.2	18.8+j19.2	18.8+j19.2	18.9+19.2	18.8+j19.2
Z_{OPT} (Ω) 3dB OBO	20.1+j37.7	20.3+j37.7	20.3+j37.7	20.3+j37.7	20.3+j37.7
Frequency	**1.7 GHz**	**1.8 GHz**	**1.9 GHz**	**2.0 GHz**	**2.1 GHz**
Z_{OPT} (Ω) Saturation	14.7+16.9	14.7+j16.9	14.7+j16.9	15.3+j11.9	14.7+j16.9
Z_{OPT} (Ω) 3dB OBO	20.3+j37.7	15.4+j31.1	17.8+j34.2	17.8+j35.2	13.1+j28.4
Frequency	**2.2 GHz**	**2.3 GHz**	**2.4 GHz**	**2.5 GHz**	**2.6 GHz**
Z_{OPT} (Ω) Saturation	15.3+j11.9	15.3+j11.9	15.3+j11.9	15.3+j11.9	15.3+j11.9
Z_{OPT} (Ω) 3dB OBO	28.8+j36.6	28.8+j36.6	28.8+j36.6	28.8+j36.6	28.8+j36.6

An impedance inverter network can be designed analytically or graphically using Smith chart utility available in ADS. The selection of the particular technology depends on the system requirements, for example the frequency of operation, bandwidth, size and the realization resolution. In wireless communication systems L- and S-band matching networks, normally consist of lumped and distributed elements. The particular requirements of the matching network depend on the operational mode of power amplifier. Moreover, the bandwidth requirements of the inverter depend upon the system requirements. This particular amplifier has 1100 MHz bandwidth and hence the impedance inverter networks should provide the respective bandwidth [102]. The value of the impedance transformation ratio is zero consequently, it is easy to design an

inverter. The low-order impedance inverter is designed for the proposed DPA, as shown in Figure 6.7 using the method [109].

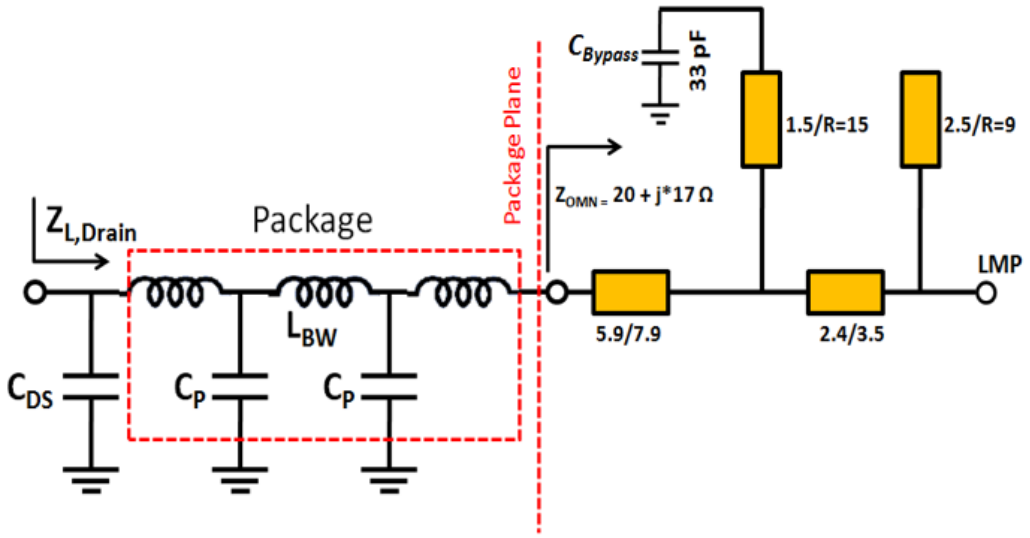


Figure 6.7: Carrier impedance inverter and drain biasing network.

Table 6.3: Load-pull simulation for optimum efficiency and power at saturation, when biased with V_{GS} = -6.15 V.

Frequency	**1.2 GHz**	**1.3 GHz**	**1.4 GHz**	**1.5 GHz**	**1.6 GHz**
Z_{OPT} (Ω) Saturation	25.3+j46.3	20.2+j37.7	20.2+j37.7	17.8+34.1	15.4+j31.1
Frequency	1.7GHz	1.8GHz	1.9GHz	2.0GHz	2.1GHz
Z_{OPT} (Ω) Saturation	17.2+24.9	17.2+24.9	17.2+24.9	13.9+j22.2	13.9+j22.2
Frequency	2.2GHz	2.3GHz	2.4GHz	2.5GHz	2.6GHz
Z_{OPT} (Ω) Saturation	15.3+j11.9	10.1+j19.9	10.1+j19.9	14.5+j16.9	14.5+j16.9

For the impedance inverter of peaking PA, a low-pass configuration is exploited. Once again, in order to find the optimum impedances load and source-pull simulation was performed from 1.2 to 2.6 GHz in Class-C bias conditions for optimum PAE and output power. Simulated load-pull optimum impedances for the whole band at saturation are shown in Table 6.3. The range of the real component of optimal impedances is from 10.1 to 25.3 Ω. Thus, the average value is $R_{opt,p}$ = 16 Ω. For the peaking PA, the LMP impedance is set to $2R_{LPM}$ and then impedance inverter is designed for peaking PA from 16 Ω to 40 Ω impedance. For peaking PA impedance inverter, same design procedure is used as for the carrier impedance inverter. The final diagram of impedance inverter is shown in Figure 6.8.

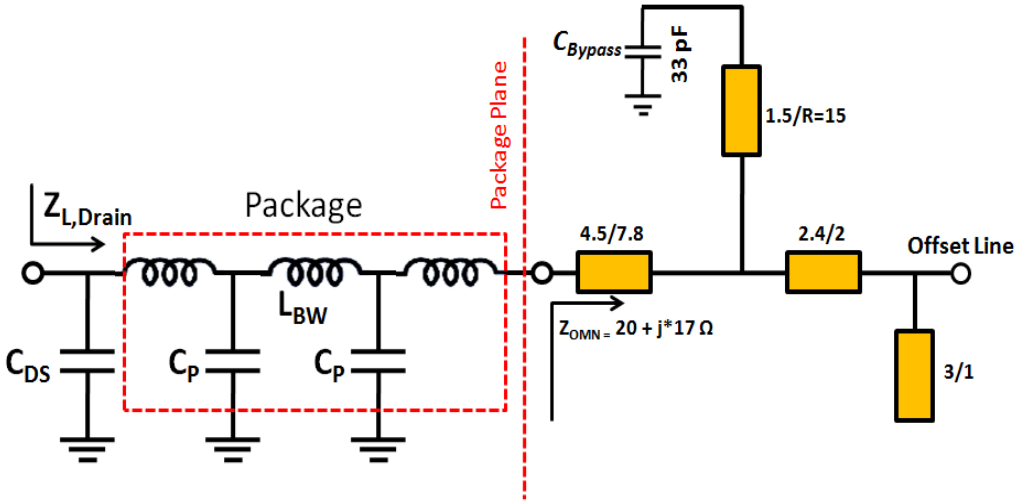


Figure 6.8: Peaking impedance inverter and drain biasing network.

6.5.4 Input matching network

The main purpose of an input matching network is to transform the optimum source impedance to system level impedance 50 Ω for the maximum power transfer from the source to the gate of a transistor. Input matching network can also be used to boost the overall gain of the power amplifier. In recent studies [92], it is also presented that the input matching network can enhance efficiency and output power of Class-F PAs. Input matching networks of carrier and peaking amplifiers have similar architecture. Input matching network also includes the stability network as well. A 47 Ω series resistor and 82 pH inductor is added in the gate bias to ensure low frequency stability. Moreover, a parallel RC (R = 22 Ω

and C = 4.7 pF) circuit to the series of transistor's gate is also used to ensure in and out-of-band stability of the power amplifier.

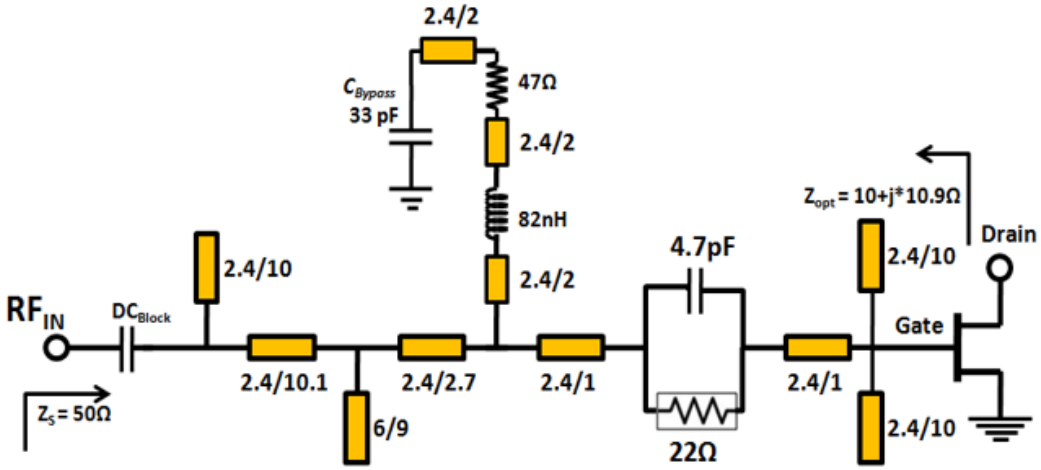


Figure 6.9: Input matching network topology.

After adding the stability circuit in the input matching network, the optimum input impedance of a transistor is determined again from a source-pull simulation. A complex conjugate of the small-signal impedance is taken from the simulated input reflection data S_{11}. The next step is to design the input matching network to transform the input of Zin = 10+j*10 Ω to 50 Ω. The input matching network has been designed using a π- input matching low pass matching. The schematic and the small-signal response of the designed network are shown in Figure 6.9. This matching network is then implemented with TLs, the same as that in the output network. The input matching network showed reasonable reflection and insertion losses throughout the band.

Moreover, in the gate-biasing network instead of using a conventional λ/4 line, a series resistor and inductor are used in the gate biasing network for reducing the gate current and absorbing the noise from the power supply. In the gate and drain bias networks of both PAs, a set of bypass capacitors are used [1, 22, 100 pf and 4.7 μF].

6.5.5 Post-matching network

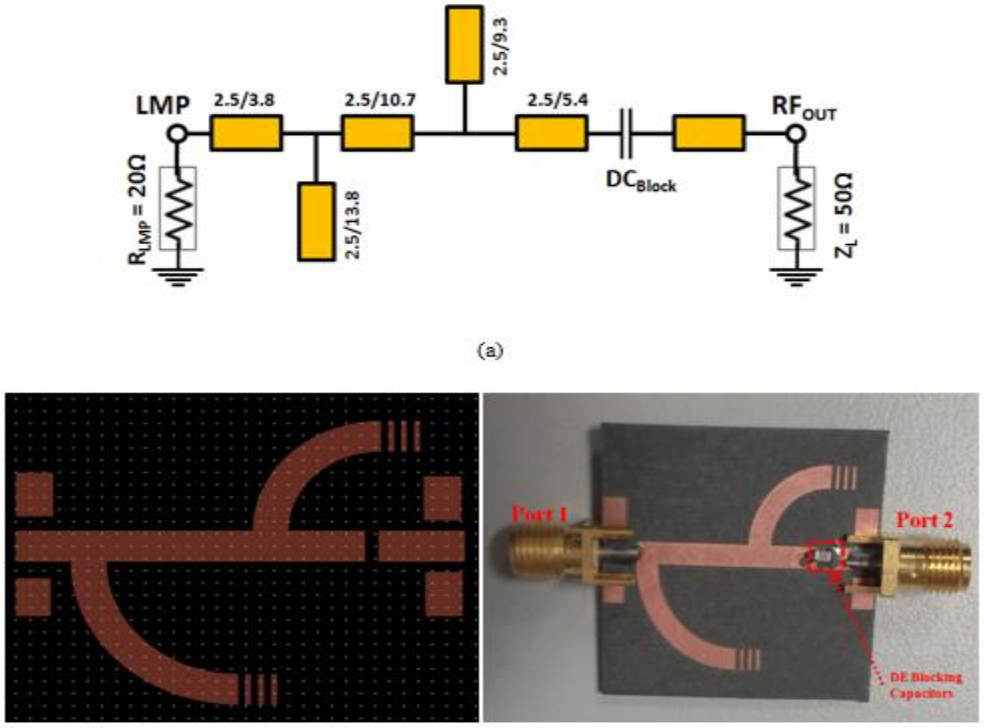


Figure 6.10: (a) Circuit topology, (a) EM simulation and (b) photo of realized post-matching network.

In a broadband DPA design, the matching network is usually based on high-order filter topologies for addressing the high impedance transformation ratio in the designed band. Higher order filter topologies for matching networks in the PAs are frequently built using filter circuit, which can present reasonable band-pass and band-stop characteristics with high impedance ratio transformation as well. In our design, post-matching network is also designed using higher-order topologies. The post-matching network converts reference impedance 50 Ω to 20 Ω load matching impedance. It is designed at central frequency and for ultra-wide bandwidth from 1.1 to 2.6 GHz frequency range. The Figure 6.10 (a) shows the used output matching network topology for the proposed PA. In the adopted topology for post-matching circuit design, four-ordered lumped component based matching network is used for the required bandwidth.

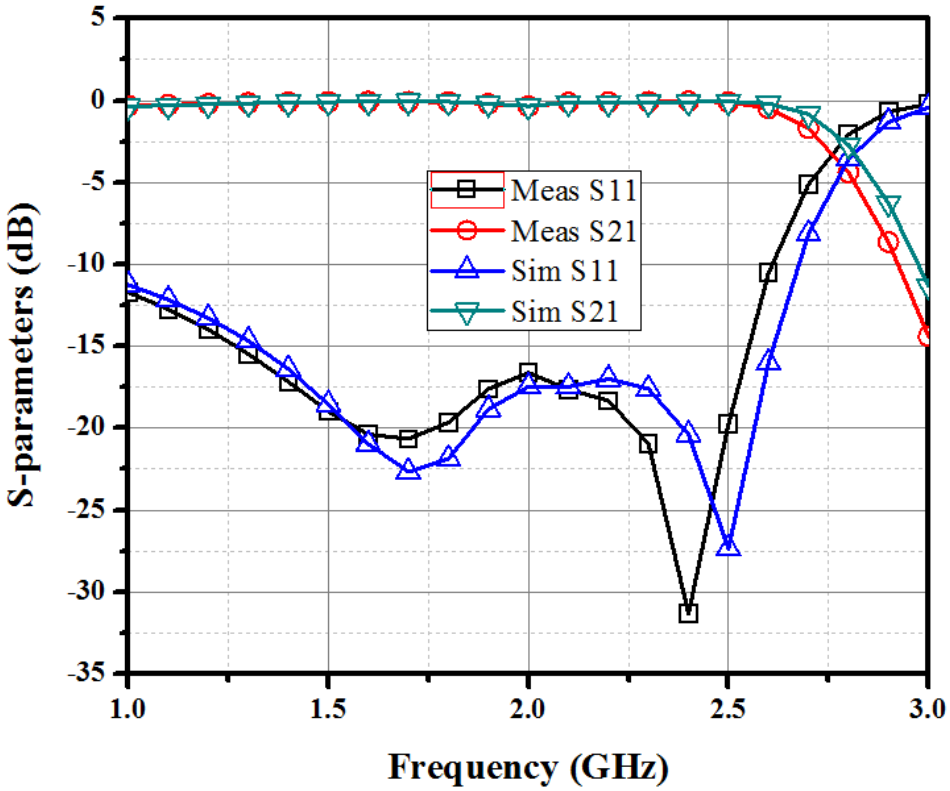


Figure 6.11: Measured and simulated transmission coefficient S_{21} and input reflection coefficient S_{11}.

Finally, before realizing the PMN, the length of each TL section is fine-tuned for a minimum reflection and insertion loss through the band. Figure 6.10 (b) shows the layout in ADS and implementation of PMN with their corresponding length and width of transmission lines. The EM simulation of the proposed post-matching network shows very good reflection and insertion losses throughout the designed band. The measured and simulated forward loss of the designed and fabricated PMN is shown in Figure 6.11. The measured value of the forward loss are within -0.1 dB for the desired bandwidth of Doherty operation. The measured value of reflection loss S_{11} is less than -15 dB at the design frequency of 2 GHz.

5.5.6 Offset-line and compensating-line

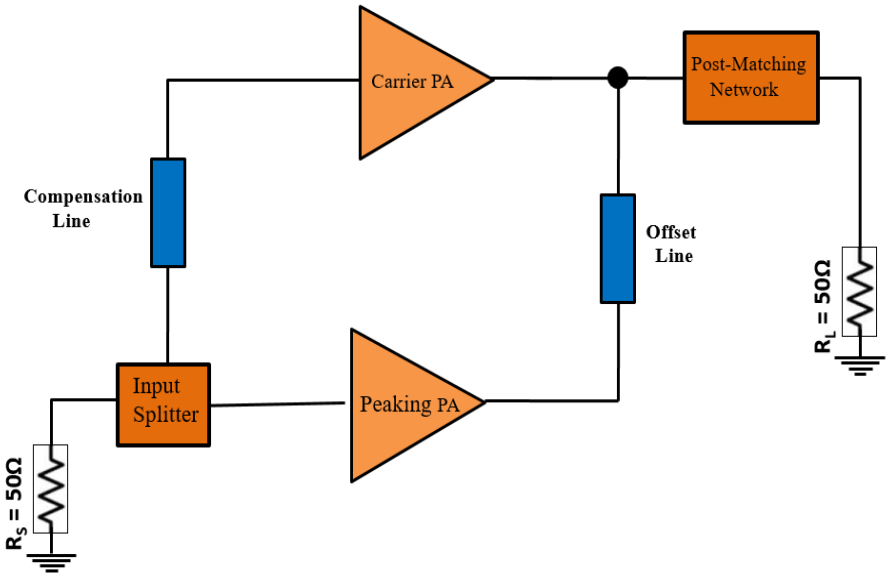


Figure 6.12: Basic building blocks of proposed Doherty power amplifier.

In a conventional DPA, it is very common to use offset-line in combination with output matching network to compensate the output parasitics of the active device. In this proposed designed, we used only one off-set line at the output of the peaking amplifier in combination with the peaking inverter network, shown in Figure 6.12. Moreover, a phase compensation at the input of the carrier amplifier is also used for the adjustment of 90^{o} degree phase difference between carrier and peaking PAs drain terminals in order to have the appropriate load modulation.

The offset-line and OMN can be implemented using distributed, lumped elements or may be a combination of both elements. The significance of the offset-line was first presented by [74], and after that several other researchers utilized offset-line in their work [109], [112]-[114]. We used offset-line for two basic purposes, first to have perfect load modulation at the LMP throughout the band. Secondly, preventing any leakage current from the peaking PA during off-state, when it is driven with low input power.

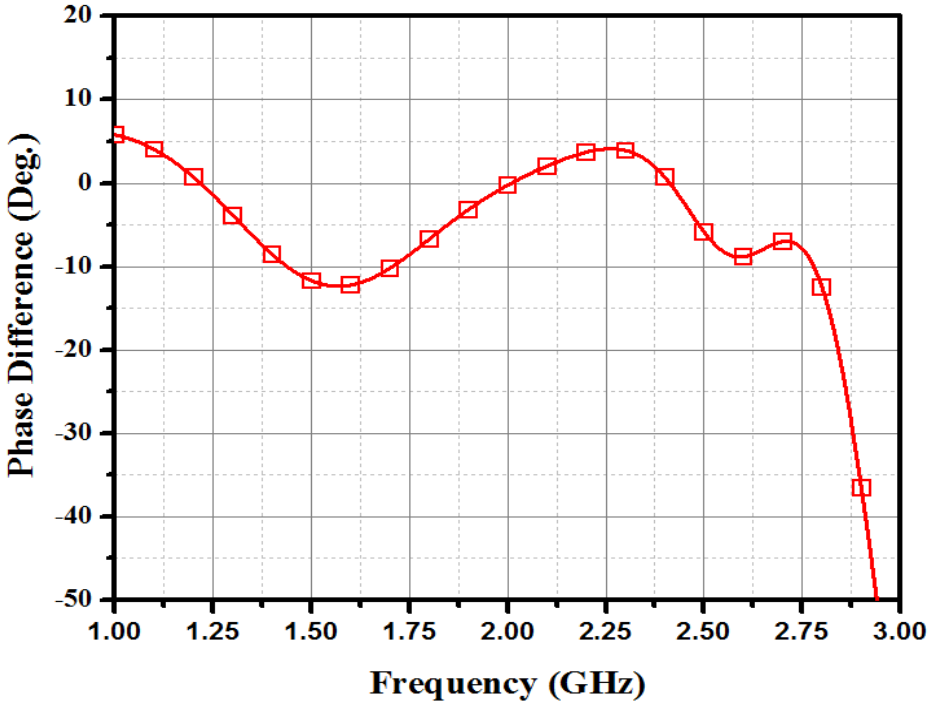
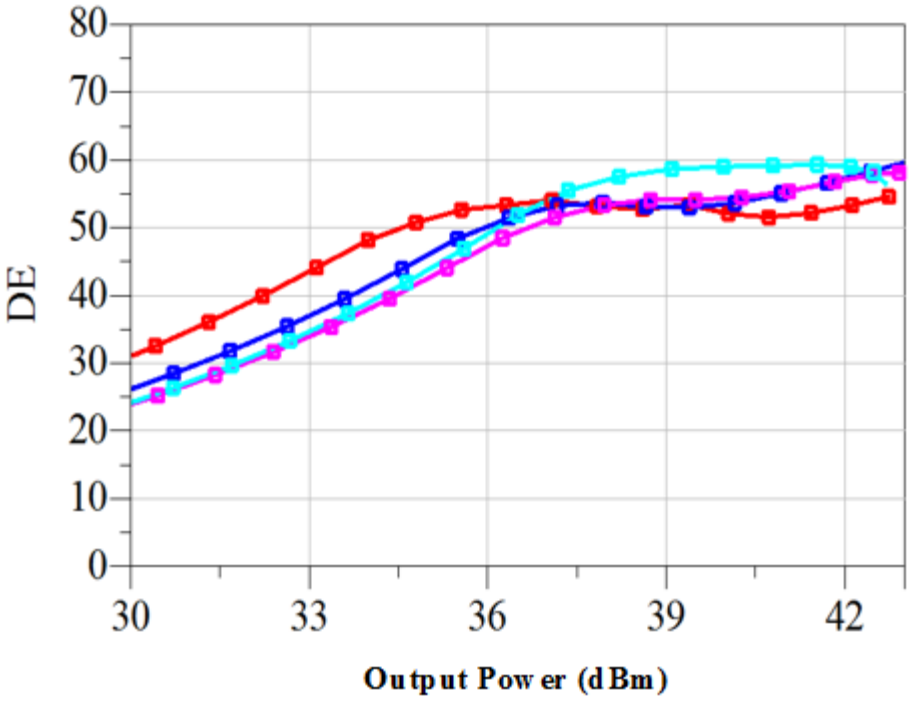
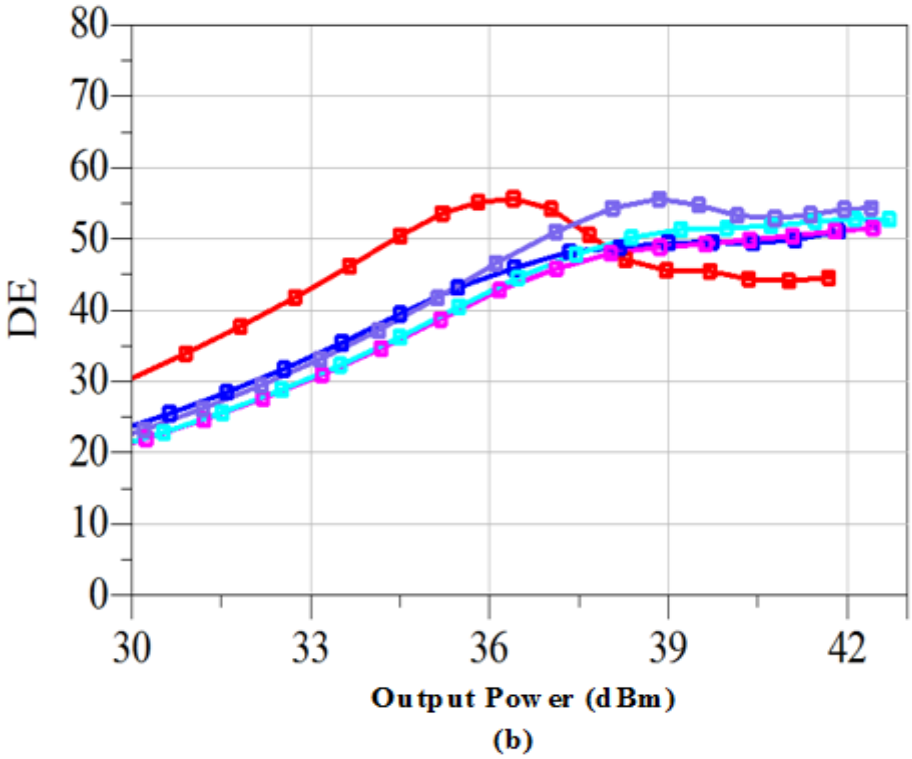


Figure 6.13: Phase difference in degree at load modulation point after the final optimization of offset-line and compensation-line.

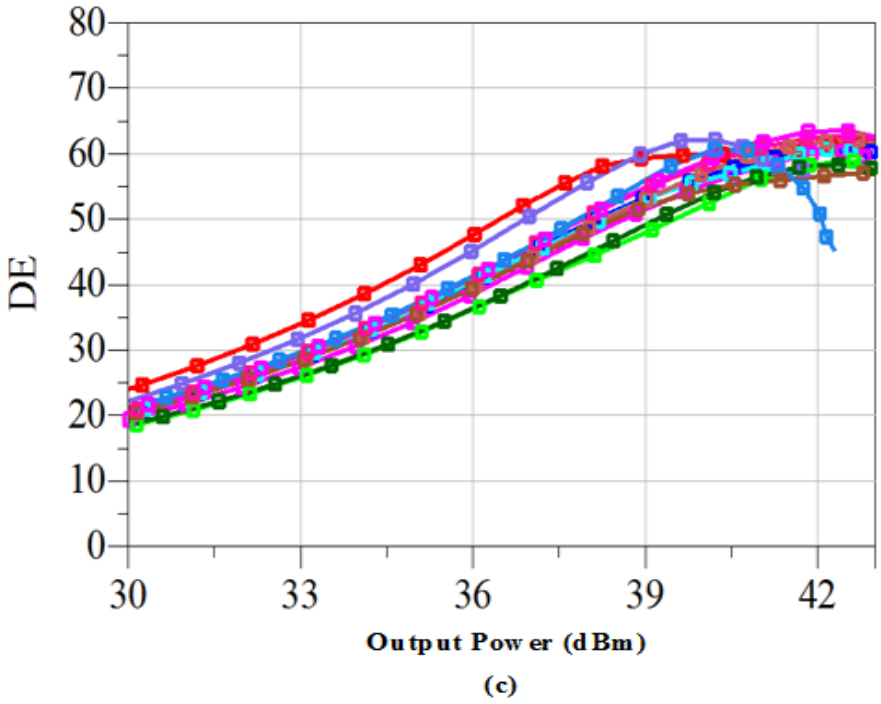
In order to know the behavior of the DPA, extensive simulation is performed with different offset-line length and characteristics impedance. The corresponding efficiency curves are plotted at four different points, as can be seen from Figure 6.14. Different combination of the offset- and compensation-lines show different bandwidth of the Doherty amplifier. The DPA performance in terms of back-off efficiency, output power and bandwidth response was recorded. It was noticed that with λ/6 offset-line length and 50 Ω characteristics impedance, DPA has a very high back-off efficiency; however, its working bandwidth was only 40%. On the contrary, DPA with a λ/4 line (characteristics impedance of 40 Ω), it showed wider bandwidth response but with slightly lower back-off efficiency. At 6 dB back-off, it is greater than 40%. Table 6.4 is showing DPA performance with the variation of offset/compensation-lines length and width. Figure 6.13 presents the phase difference in degree at load modulation point after the final optimization of offset-line and compensation-line. The phase difference is zero at design frequency (2 GHz). Overall, it is within the range of +8 to -12 degree throughout the targeted band. It is proposed that DPA bandwidth can be controlled by tuning the offset- line for required bandwidth and performance by using this particular circuit architecture.


80
70
60
50
40
30
20
10
0
DE
30
33
36
39
42
Output Power (dBm)

(a)


80
70
60
50
40
30
20
10
0
DE
30
33
36
39
42
Output Power (dBm)

(b)



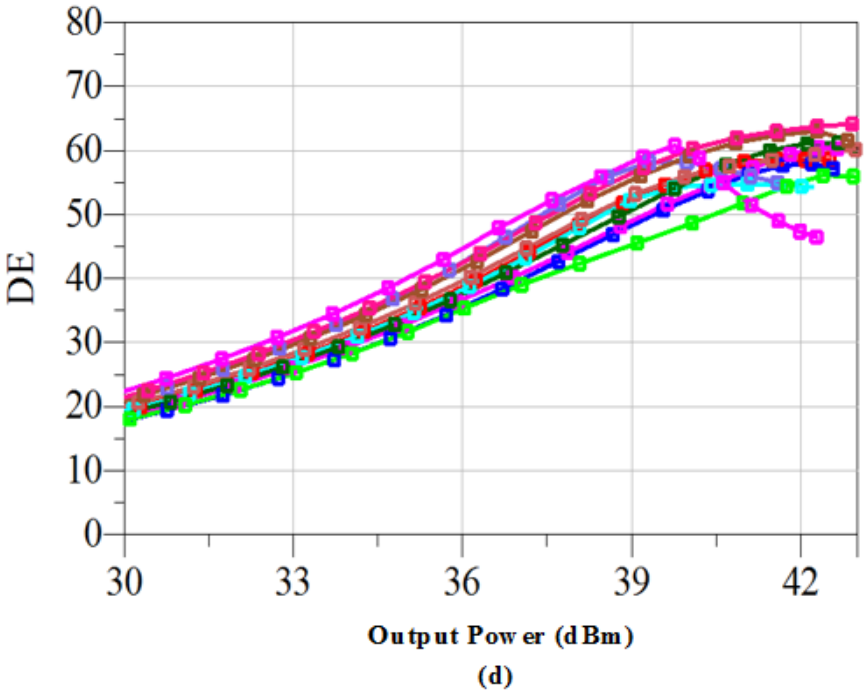


Figure 6.14: Drain efficiency at different offset line combination.

Table 6.4: DPA bandwidth with the variation of offset/compensation-lines length and width.

Length of Comp. line (Degree)	Length of Offset line (Degree)	Impedance (Ω)	Bandwidth (GHz)	Efficiency (%)
60	60	44	1.3-1.6	50%
75	75	44	1.2-1.6	44%
90	80	44	1.15-2.35	42%
105	105	44	1.2-2.2	39%

6.6 Final design

On the final schematic of PA, various small-signal and large-signal simulations have been performed to optimize the input and output return losses, small-signal gain, bandwidth and drain back-off efficiency at 6 dB. A microwave substrate in the design environment of ADS was chosen with laminate Duriod of thickness 0.79 mm with a relative dielectric constant of 2.33. The synthesized biasing and matching networks were implemented using transmission lines (Detail circuit diagrams in ADS are given in Appendix D). At 2 GHz, on this Duriod 5850 substrate, a quarter-wavelength translates to approximately 26 mm length and width 2.4 mm impedance microstrip line.

In the last step of simulation and for verification purpose, an electromagnetic simulation has been performed for distributed network and complete DPA. The details of the DPA schematic and layout are given in Appendix D. A good agreement in circuit and electromagnetic simulations has been observed for the whole design band. Final dimension of the transmission lines of the proposed PA are presented in appendix D. The final step in DPA design is to realize the prototype circuit using the specified material and components.

The fabricated amplifier is based on hybrid technology. Lumped components and devices have been carefully soldered on printed circuit board (PCB) in order to minimize the fabrication errors. The physical implementation of the DPA is

shown in Figure 6.15. A heat sink was inserted under the substrate to provide good thermal control. The footprint of the fabricated PA is 120×80 mm.

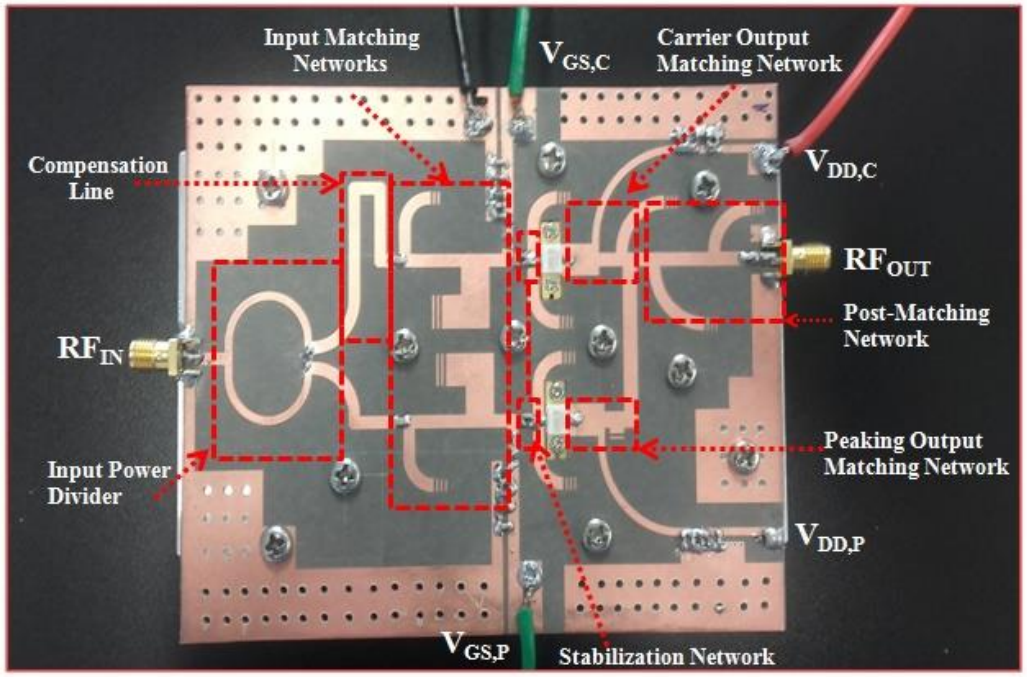


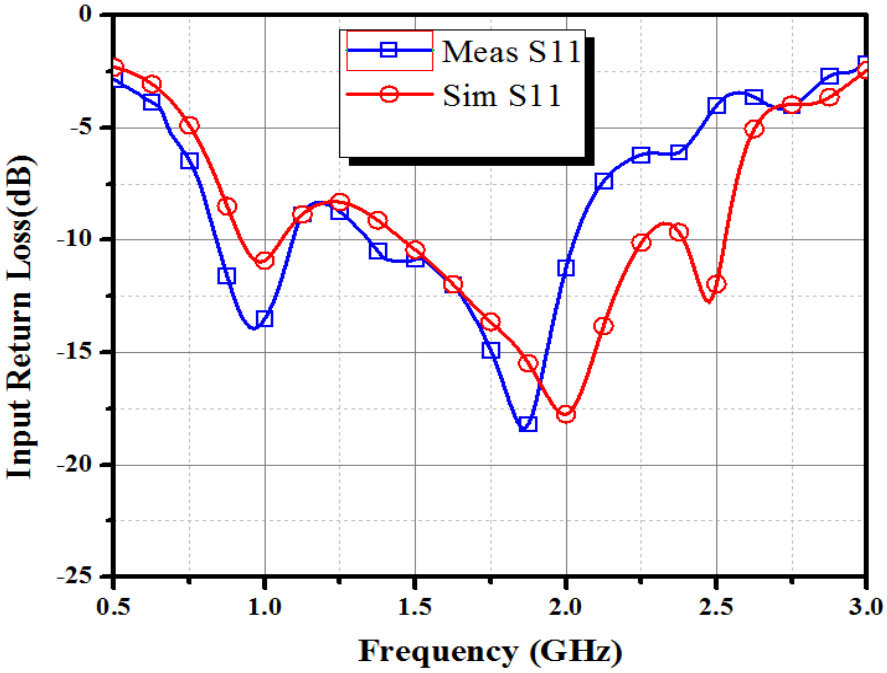
Figure 6.15: Photo of realized Doherty power amplifier.

6.7 Performance evaluation

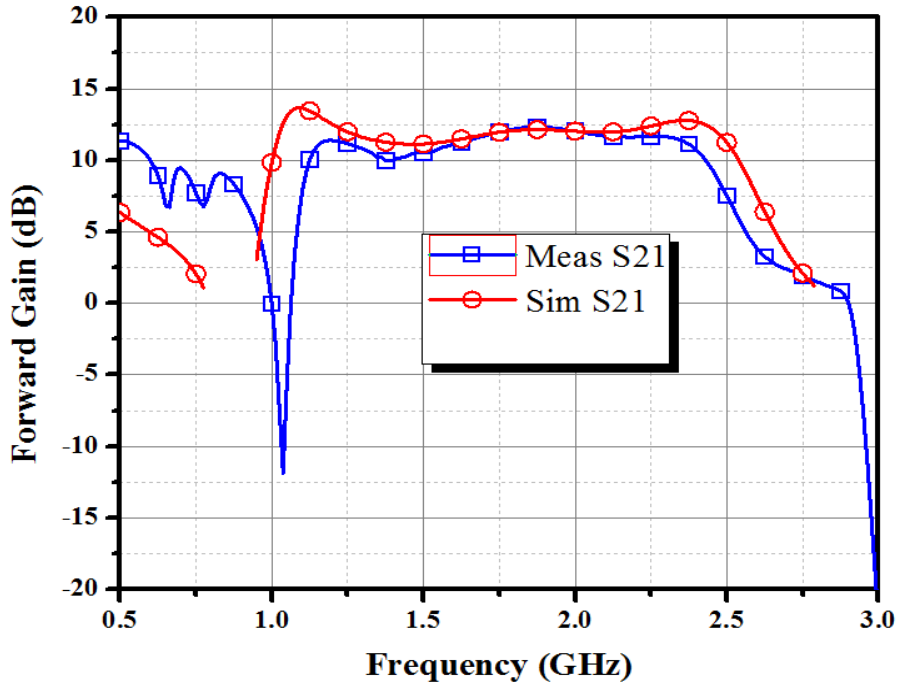
This section will present the simulated and measured performance of the proposed Doherty power amplifier, in terms of small-signal gain, drain efficiency, gain, output power, bandwidth and ACPRs.

6.7.1 Small-signal testing

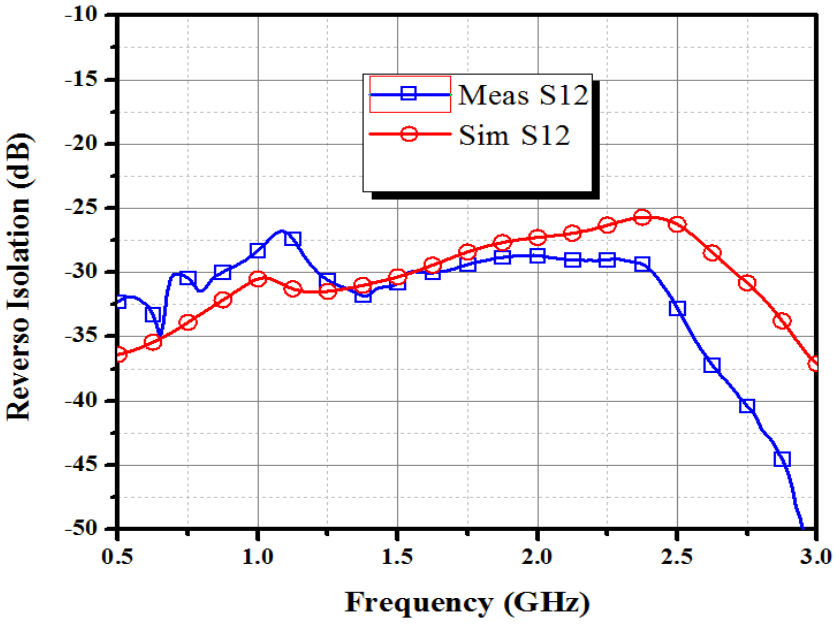
The prototype has been characterized in a small-signal regime in order to find the small signal gain and input return loss of the proposed DPA design. The measurement setup includes the four ports Agilent vector network analyzer (VNA), power supply, four ports electronic calibration kit, and the HP 8563E spectrum analyzer. An electronic calibration procedure is used to calibrate the VNA.


Meas S11
Sim S11
Input Return Loss(dB)
Frequency (GHz)
0
-5
-10
-15
-20
-25
0.5
1.0
1.5
2.0
2.5
3.0

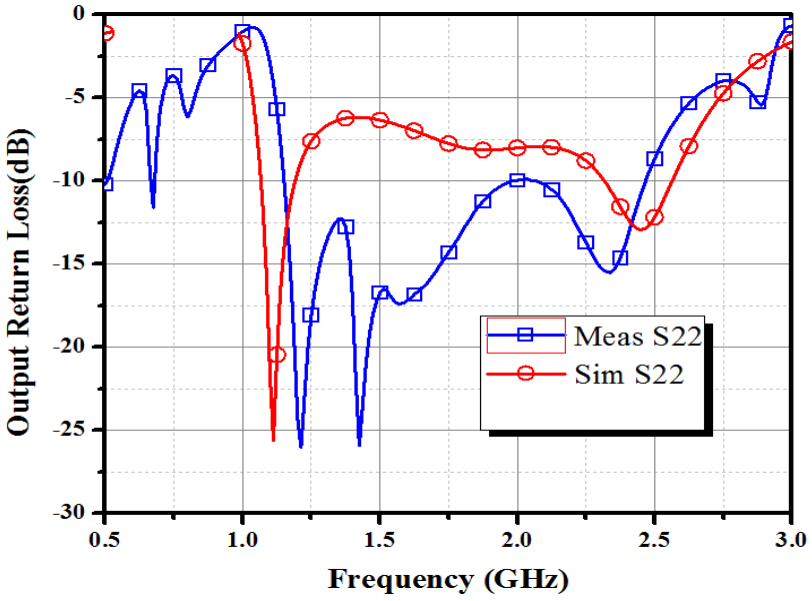
(a)


Meas S21
Sim S21
Forward Gain (dB)
Frequency (GHz)
20
15
10
5
0
-5
-10
-15
-20
0.5
1.0
1.5
2.0
2.5
3.0

(b)



(c)



(d)

Figure 6.16: Measured and simulated small-signal gain of the proposed DPA (a) input return loss, (b) forward gain, (c) reverse isolation, and (d) output return loss.

Figure 6.16 shows the measured and simulated small-signal performance of the DPA biased at V_{DS} = 28 V and I_{DS} = 50 mA. It is important to mention that the measured small-signal gain is presented because the main power amplifier, and peaking power amplifier is in off state at this biased condition. As it can be seen from Figure 6.16, an approximately constant small-signal gain in excess of 10 dB is maintained over 1.1 GHz bandwidth. The measured small-signal gain curve closely tracks the simulated one between 1.3 to 2.3 GHz, while it is slightly lower at the edges of the targeted bandwidth. A small bandwidth loss can be attributed to the fabrication errors during the implementation of DPA such as changes of the width and length of the transmission line, and inaccuracies in the model of the active components.

6.7.3 Single-tone power sweep

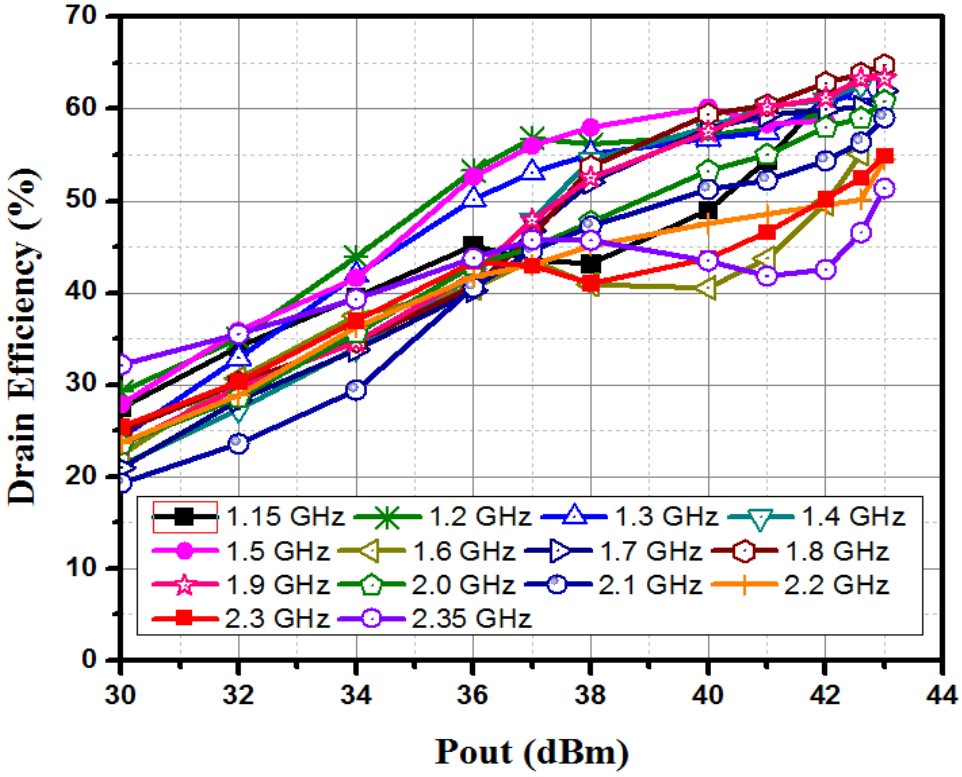


Figure 6.17: The measured drain efficiency vs. output power for designed bandwidth at the V_{DS} = 28 V and I_{DS} = 50 mA.

Single-tone large-signal characterizations are also carried out in order to establish the proposed DPA performance for the whole frequency band from 1.15

to 2.35 GHz as a function of the input power level. Before the single-tone large-signal measurements, the test bench was fully calibrated carefully. The measured results of DPA over the designed bandwidth with 100 MHz spacing are recorded, when it is biased at V_{DS} = 28 V and I_{DS} = 50 mA. In single-tone power sweep drain efficiency is measured as function of output power at each frequency, and efficiency curves are plotted in Figure 6.17. The corresponding input power are swept from 20 dBm to 36 dBm in 1 dB increments. The measured drain efficiency is greater than the 40% at 6 dB back-off (Pout = 37 dBm) for the designed bandwidth. Moreover, saturated drain efficiency is from 52 to 65% for the whole bandwidth. A linear transconductance gain is approximately 10.1-11.5 dB as shown in Figure 6.18 and the maximum output power is from 41.8 to 43 dBm.

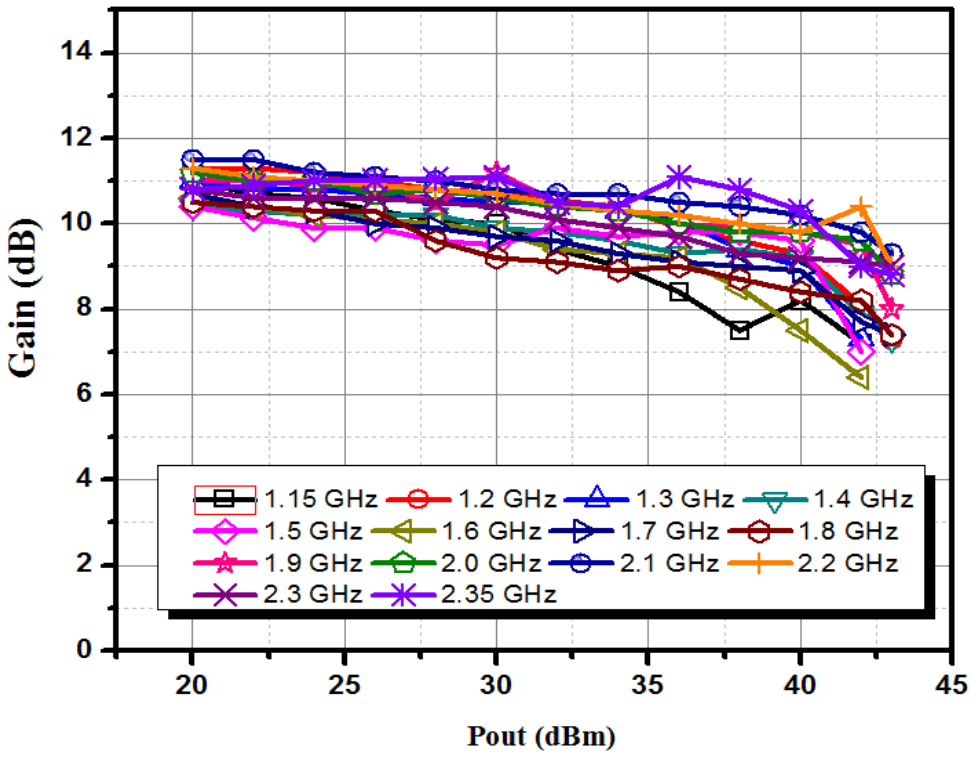


Figure 6.18: The measured gain vs. output power for designed bandwidth at the V_{DS} = 28 V and I_{DS} = 50 mA.

To evaluate the bandwidth response of designed DPA, single-tone testing has been performed from 1.15 to 2.35 GHz with a spacing of 100 MHz. The measured parameters such as output power, peak gain, gain at 6 dB back-off, and gain at saturation output power are plotted in Figure 6.19, ranges from 1.15 to 2.35 GHz. The measured data showed a peak gain of 11.6 dB at 2.1 GHz with an output

power of 43 dBm and a 6 dB back-off gain of 10 dB. Moreover, PA maintains a saturated output power higher than 41.7 dBm and gain peak gain higher than 10.2 dB over the whole frequency band, as depicted in Figure 6.19.

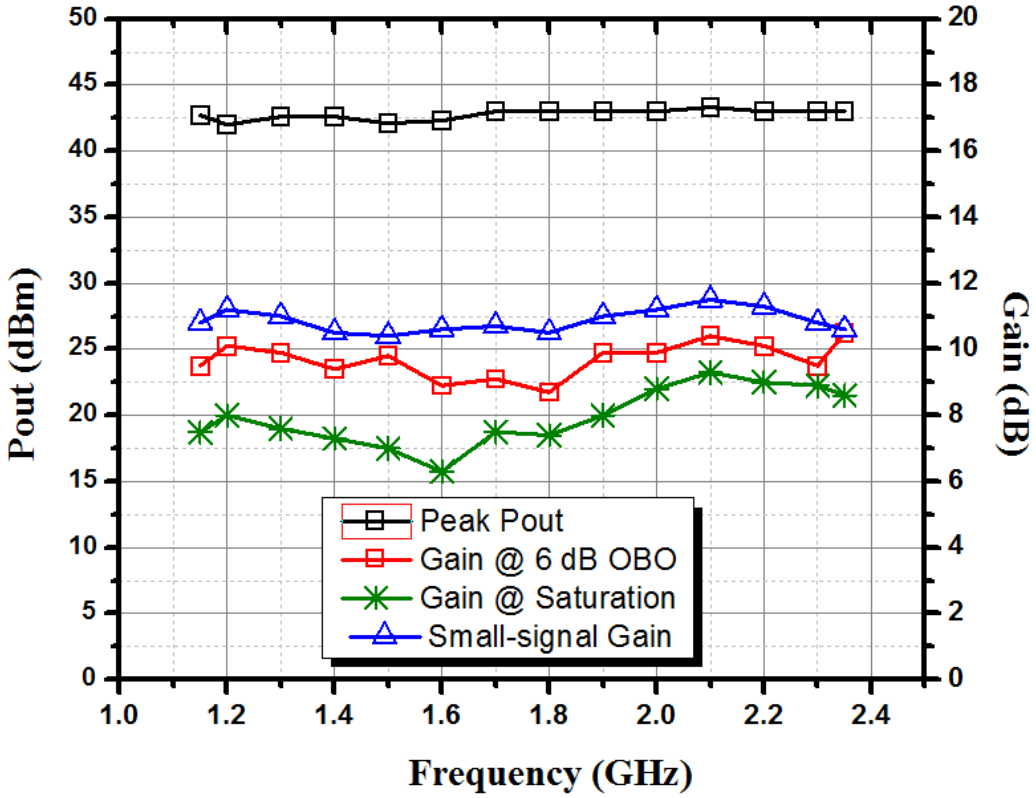


Figure 6.19: The measured gain at three different levels and output power versus frequency at the V_{DS} = 28 V and I_{DS} = 50 mA.

Since the proposed DPA is a potential candidate for an LTE application, its performance in terms of efficiency at 6 dB back-off are also recorded. To this purpose frequency are swept from 1.15 to 2.35 GHz and DPA's efficiency was measured. As can be seen from the Figure 6.20, the DPA showed excellent performance: a peak drain efficiency of 65% is measured at 1.8 GHz, and the drain efficiency varies from 52 to 65% at saturation. Moreover, it also maintains the 6 dB back-off efficiency higher than 40%.

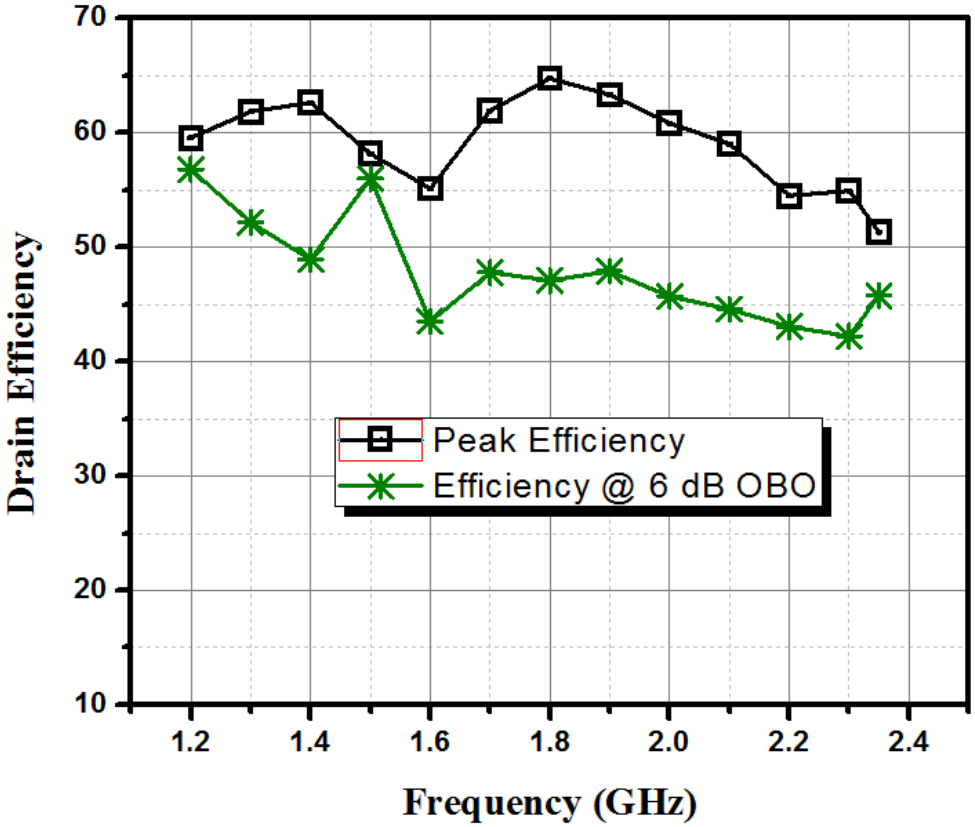


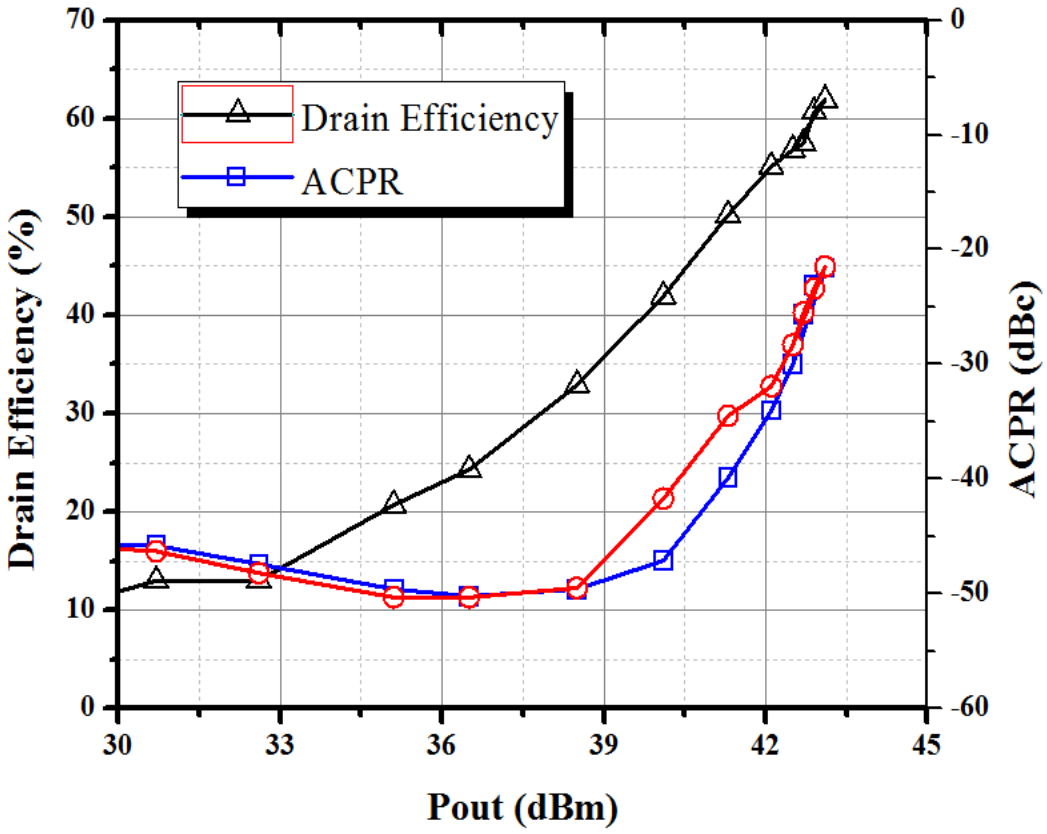
Figure 6.20: The measured peak drain efficiency and efficiency at 6 dB back-off vs. frequency at the V_{DS} = 28 V and I_{DS} = 50 mA.

6.7.3 Modulated signal characterization

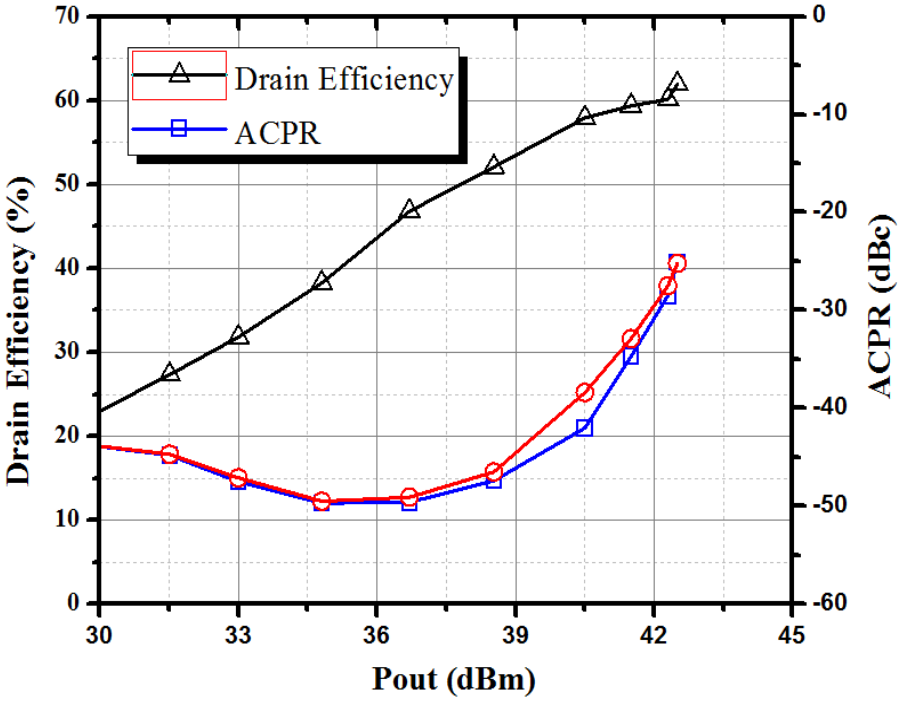
The performance of the power amplifier with a real communication signal has been measured over the proposed frequency band. A fully calibrated frequency domain measurement setup is used to measure the Adjacent Channel Power Ratio (ACPRs) of the implemented power amplifier. The same measurement setup is used to measure the Adjacent Channel Power Ratio (ACPR) described in Section 3.8 with an input signal of 5 MHz WCDMA signal with a PAPR of 6.5 dB. Measurement setup consists of power supplies, spectrum analyser, attenuator, driver amplifier and signal generator.

Figure 6.21 shows the measured drain efficiency and ACPRs of the implemented DPA at four different frequencies 1.3 GHz, 1.7 GHz, 2 GHz, and 2.3 GHz, when DPA is excited with a 5 MHz WCDMA input signal, which has a

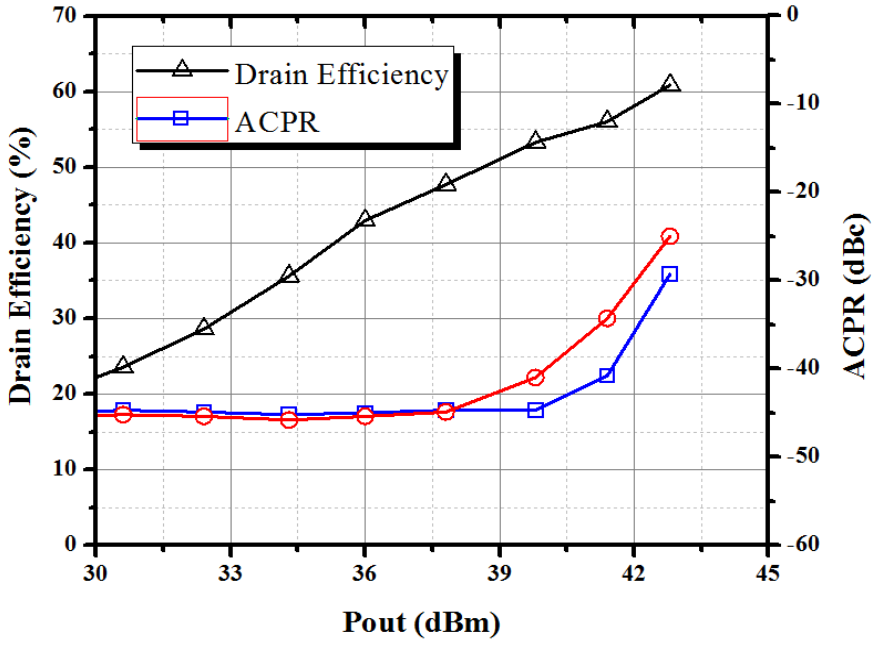
PAPR of 6.5 dB. At an output power of approximately 42 dBm close to saturation, upper ACPR of –33 dBc, and lower ACPR –35 dBc were measured at 1.3 GHz. The DPA almost shows the same trend of ACPRs at 1.7 GHz, 2.0 GHz, and 2.3 GHz. The measurements show a rapid increase in the ACPRs at an output power of more than 42 dBm. The DPAs ACPRs are also measured for the whole bandwidth using same input signal. As it can be observed in Figure 6.22, the values of lower- and upper-sideband ACPRs for the complete band are higher than 27 dB for an output power of 42 dBm, close to the saturation point.



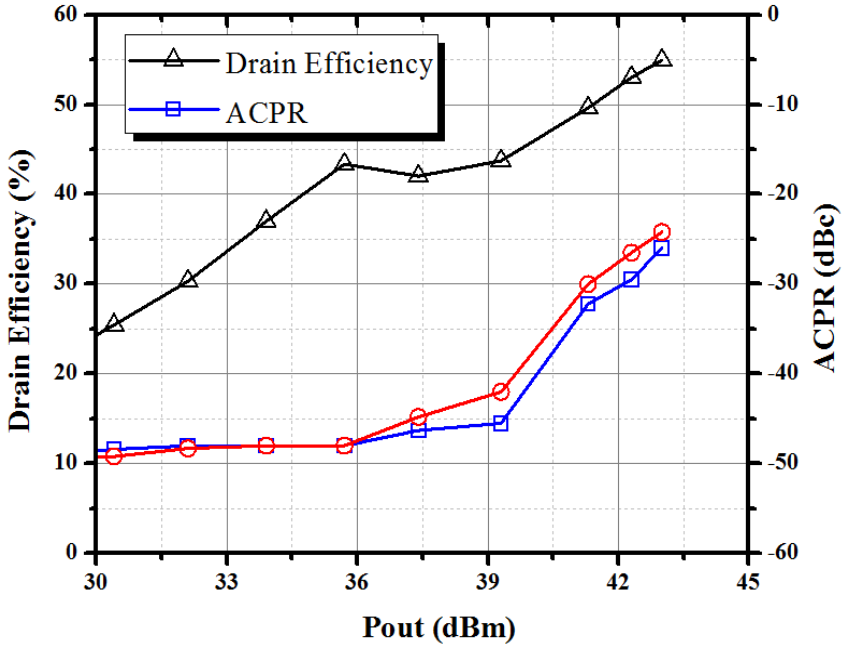
(a)


Drain Efficiency
ACPR
Drain Efficiency (%)
ACPR (dBc)
Pout (dBm)
70
60
50
40
30
20
10
0
0
-10
-20
-30
-40
-50
-60
30
33
36
39
42
45

(b)


Drain Efficiency
ACPR
Drain Efficiency (%)
ACPR (dBc)
Pout (dBm)
70
60
50
40
30
20
10
0
0
-10
-20
-30
-40
-50
-60
30
33
36
39
42
45

(c)



(d)

Figure 6.21: Measured drain efficiency, upper ACPR and lower ACPR, when DPA is excited with a 5 MHz WCDMA input signal, which has PAPR 6.5 dB at four different frequencies (a) 1.3 GHz, (b)1.7 GHz, (c), 2 GHz, and (d) 2.3 GHz.

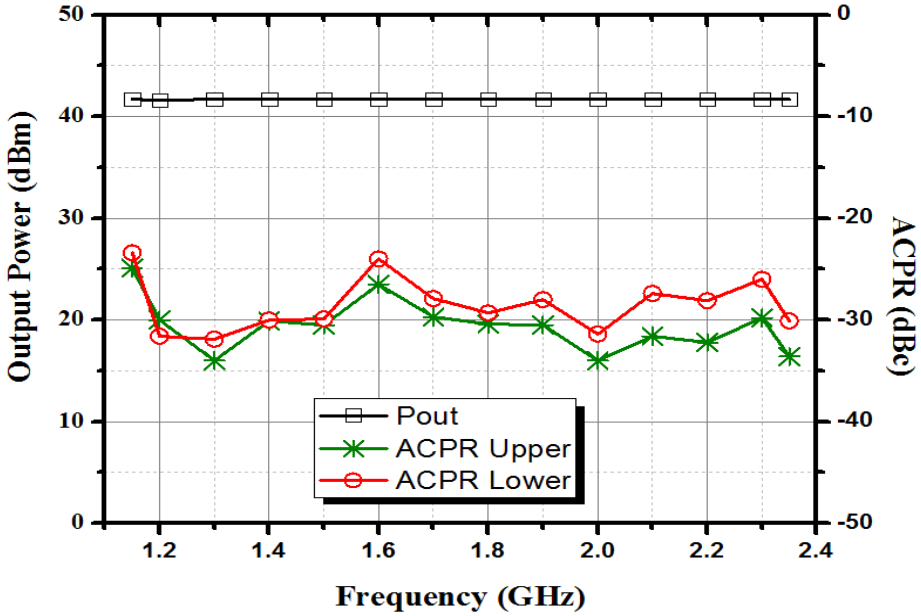


Figure 6.22: The measured ACPRs Vs. frequency at 1.6 dBm output, when DPA is based at the V_{DS} = 28 V and I_{DS} = 50 mA.

6.8 Comparison with other published results

Finally, a comparison between the recently published broadband DPAs and state-of-the-art proposed DPA is made, as shown in Table 6.5. The designed PA has a gain, output power, and back-off drain efficiency comparable to the other PAs. The simulated and measured results show that the implemented DPA has a higher fractional bandwidth as compared to the other published results.

Table 6.5: Performance compression of the proposed DPA with state-of-the Doherty power amplifier.

Ref.	**Freq. (GHz)**	**Fractional BW (%)**	**P_{sat} (dBm)**	**DE @ Sat (%)**	**DE @ 6 OPBO (%)**	**Gain (dB)**
[81] 2012	3-3.6	18	43-44	55-66	38-56	8-11
[105] 2012	2.2-3.0	31	40-42	50-67	40-48	6-8.5
[115] 2013	0.7-1.0	35	48.5-50.8	62-75	53-68	>15.3
[84] 2016	3.3-3.6	9	48.5-49.5	40.9-55.1	50-58	14.4-14.9
[117] 2014	2.1	15	41.5-42	65-68	50-58	--
[119] 2012	1.8-2.6	35	43.7-43.9	53-60	44-46	13-19
[116] 2016	1.65-2.4	40	43.5-46.1	60.1-76.2	46-57	11.5-12.1
[118] 2015	1.7-2.8	49	44-44.5	57-51	50-55	11-13
[110] 2015	1.7-2.6	42	42.1-42.3	50-55	41-55	10.2-11.6
[120] 2013	1.5-2.4	46	42	52-67	49-60	7-12
T.W	**1.15-2.35**	**68**	**41.8-43.2**	**50-68**	**40-56**	**10.3-11.6**

6.9 Summary

In this chapter, a novel design mythology for the DPA bandwidth extension is presented. Based on the proposed design methodology, a 20 W Doherty power amplifier circuit is designed and implemented using two 10 W GaN HEMT devices from Cree Inc for a multi-standard communication signal. Before the implementation, extensive simulations were performed in ADS using an accurate device model and component model to achieve the required back-off efficiency for the designed bandwidth. The simulation and measurement results verify that the DPA is a suitable candidate for an LTE downlink communication signal over the frequency range from 1.15 to 2.35 GHz.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

The data demand for wireless communications continues to grow day by day, satisfying the data demand is very challenging. As described in the introduction chapter, use of complex spectrally efficient modulation schemes imposes new and more challenging demands on PA designer. The power amplifier should be more energy efficient and linear over wide range of operating frequencies for advanced wireless application.

The research work started with the study of PA design techniques, different calibration techniques for Vector Network Analyzer (VNA), and power characterization of the PA. The research presented in third and fourth chapters of this thesis has set out to find proper solution for linearity and efficiency enhancement over wide bandwidth for wireless application by utilizing the Class-AB and Class-F PA concepts, respectively. In Class-AB PA, focus of the study was on the single-stage efficient and linear power amplifier, because the efficiency and linearity enhancement can have a significant impact on the overall efficiency and linearity of the wireless communication. A 5 W Class-AB power amplifier circuit was design and implemented using a 6 W active device for LTE communication band. The simulation and measurement results verify that the Class-AB amplifier is suitable for a high-efficiency linear PA over a frequency range for 1.9-2.5 GHz. These results indicate potential application of the Class-AB architecture for envelop tracking systems. In the Class-F PA, bandwidth

limitation factor was considered, and a broadband PA based on 10 W CGH40010F GaN HEMT was designed and implemented. The fabricated broadband Class-F PA achieved maximum 60-77% of saturated drain efficiency, and 10W output power throughout the band (1.1-2.1 GHz). The simulated and measured results verify that the broadband Class-F amplifier is suitable for a high-efficiency system over a frequency range from 1.1 to 2.1 GHz.

The DPA is the workhorse in wireless transmitters thanks to its high energy efficiency and low complexity. However, narrowband performance often makes it difficult to satisfy the multi-standard communication signal requirements. The research presented in the last two chapters of this thesis has begun to find solutions to the requirements of enhancing the back-off efficiency with wider bandwidth for LTE wireless communications systems. For this purpose, a single- and dual-input Doherty power amplifier for LTE application in the 3.5 GHz frequency band were presented. A comprehensive comparison was made between single- and dual-input DPA. In the simulated results, the dual-input DPA achieves a higher performance compared to the single-input DPA. However, it shows linearity not as good as the single-input DPA. Both PAs are suitable for LTE application.

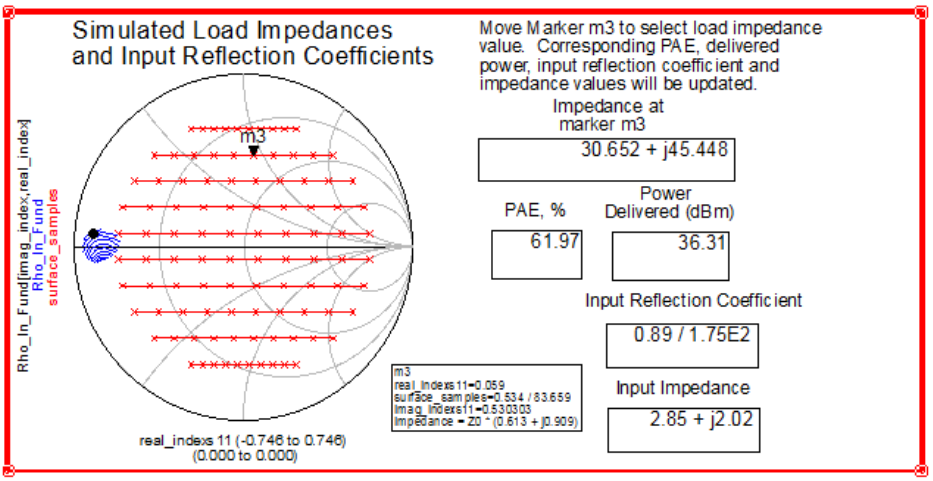
In this dissertation as the final step, in order to understand the bandwidth limitation factors, a conventional DPA design was reviewed by using standard design approach with the aim to extend DPA bandwidth as wide as possible. This study investigates the theoretical and practical bandwidth limitations of conventional DPA. It was concluded that the most of the reasons that limit the DPA bandwidth are related to its inherent properties, such as output matching network implementation and impedance inverter presence. Therefore, a novel design methodology for ultra-wide band Doherty power amplifier was presented. Experimental validation of the design methodology shows that bandwidth larger than 68% measured from two 10 W GaN HEMTs, targeting microwave application. The excellent performance and large bandwidths reported in this study shows that the DPA no longer needs to be considered as a necessarily narrowband amplifier. Due to this reason, the DPA might be the power amplifier of choice also in future wireless systems. In summary, all the amplifiers described in this study were suitable for wideband operation and their performances are satisfying the basics of the required standard of operation.

7.2 Future work

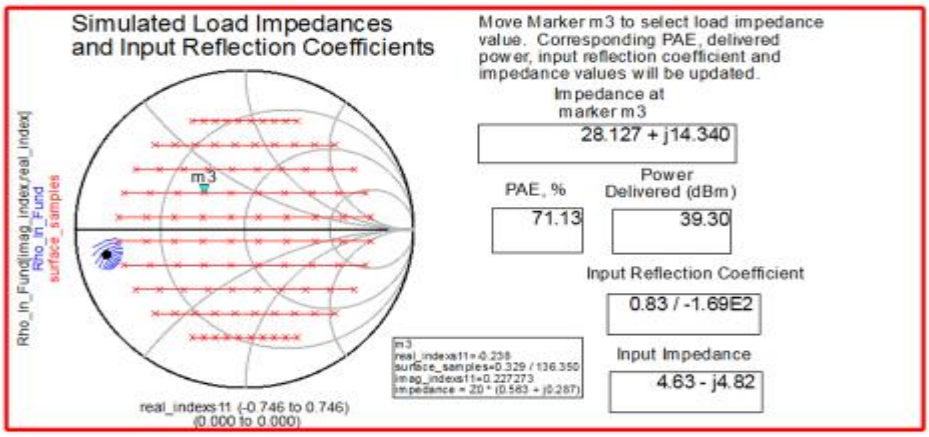
The bandwidth enhancing design methodology proposed in this study were implemented only on low and medium power levels (5-20 W) devices. Therefore, the applicability of the proposed design technique on high power microwave devices should be investigated. In particular, the bandwidth extension design technique was only applied on 6 W and 10 W transistors in the modified DPA circuits, might not be applicable at higher powers level due to large impedance variation in optimum impedance at drain terminal and device parasitics. Therefore, it should be utilized for high power active devices, which are more suitable for base-station application.

This work has not concluded the bandwidth extension more than 7 dB back-off. For commercially application, it could be a very good idea to extended the DPA back-off extension from 7 dB to 10 dB at the same time maintain wider bandwidth. Moreover, the ultra-wideband Doherty PA was implemented by using hybrid technology only. It is just a starting point to verify design methodology. From the commercial point of view, wireless communication industry would rather prefer a fully integrated wide-band Doherty power amplifier based on MMIC technology for base-station applications. The presented technique could be useful for bandwidth extension of a DPA based on MMIC technology.

Appendix A



(a)



(b)

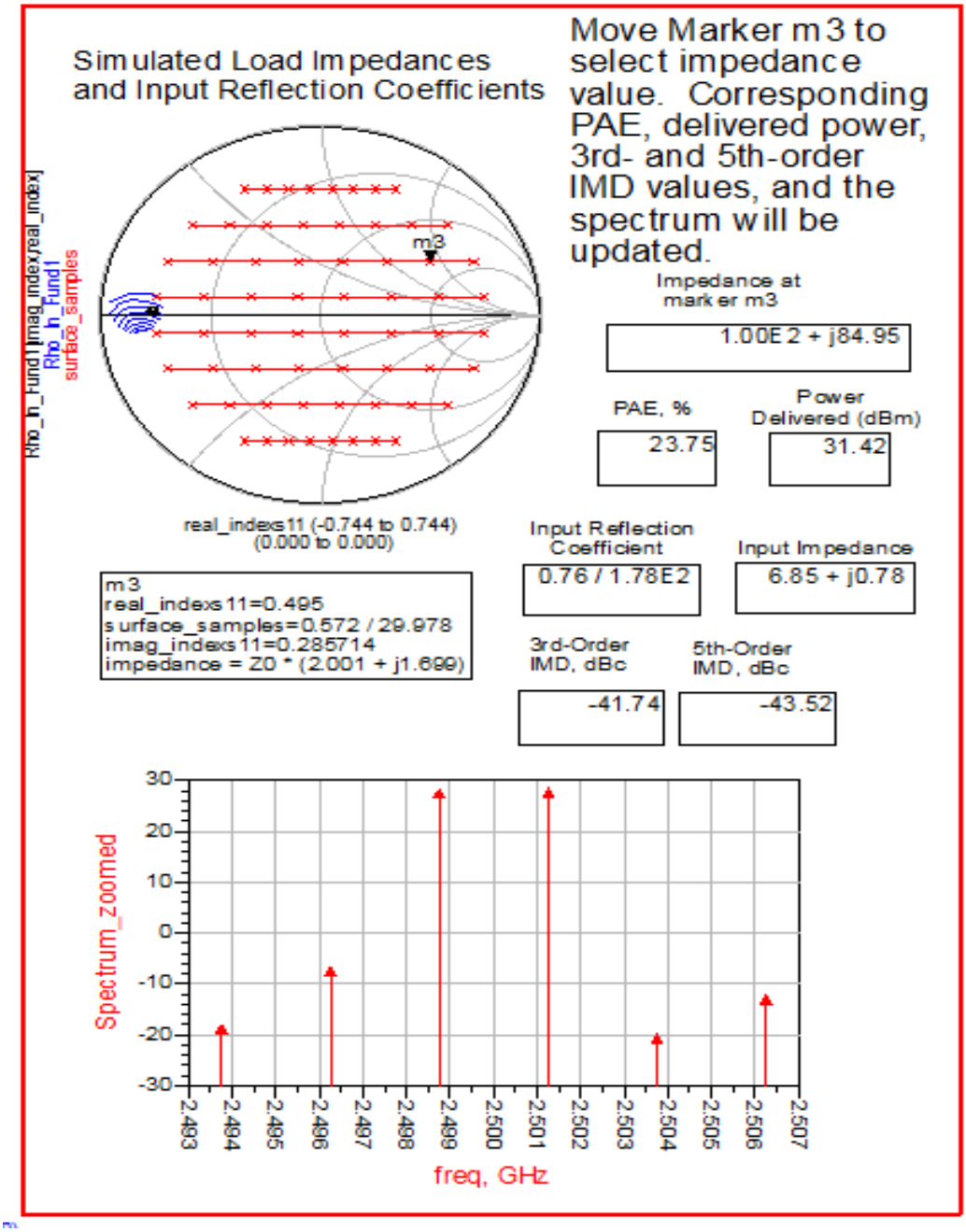
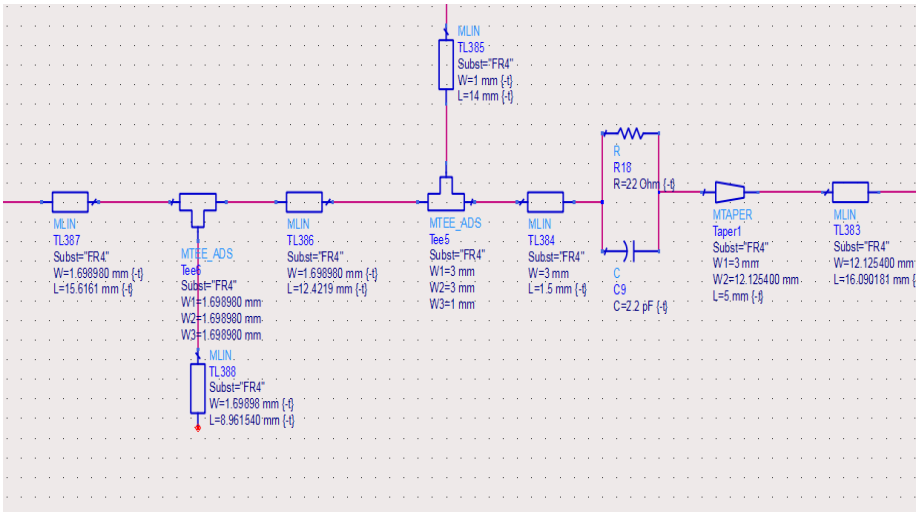
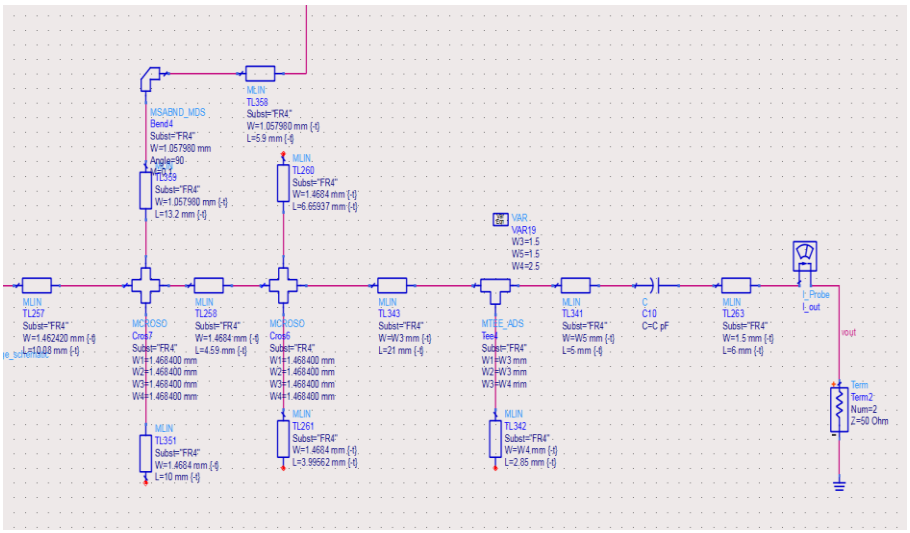


Figure A.1: (a) Simulated output power, (b) efficiency, and (c) intermodulation distortion of 6 W GaN HEMT device in ADS simulator at different load impedances.

Appendix B



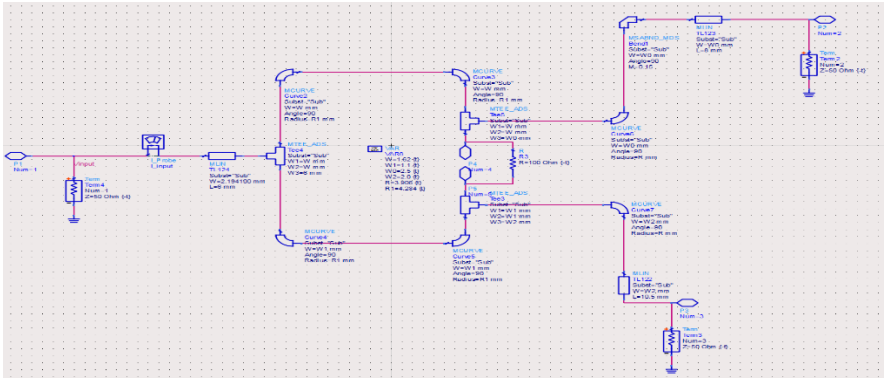
(a)



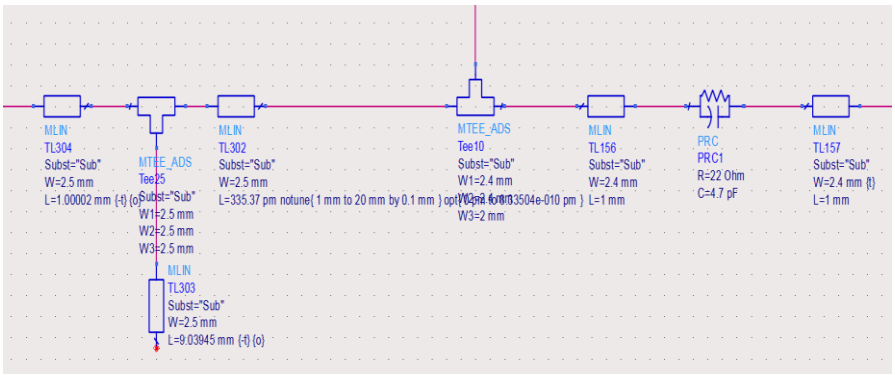
(c)

Figure B.1: (a) Input matching network and (b) output matching network ADS circuit schematic layouts.

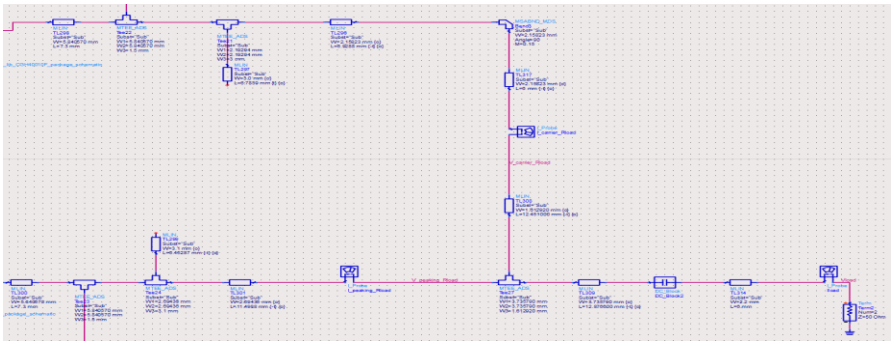
Appendix C



(a)



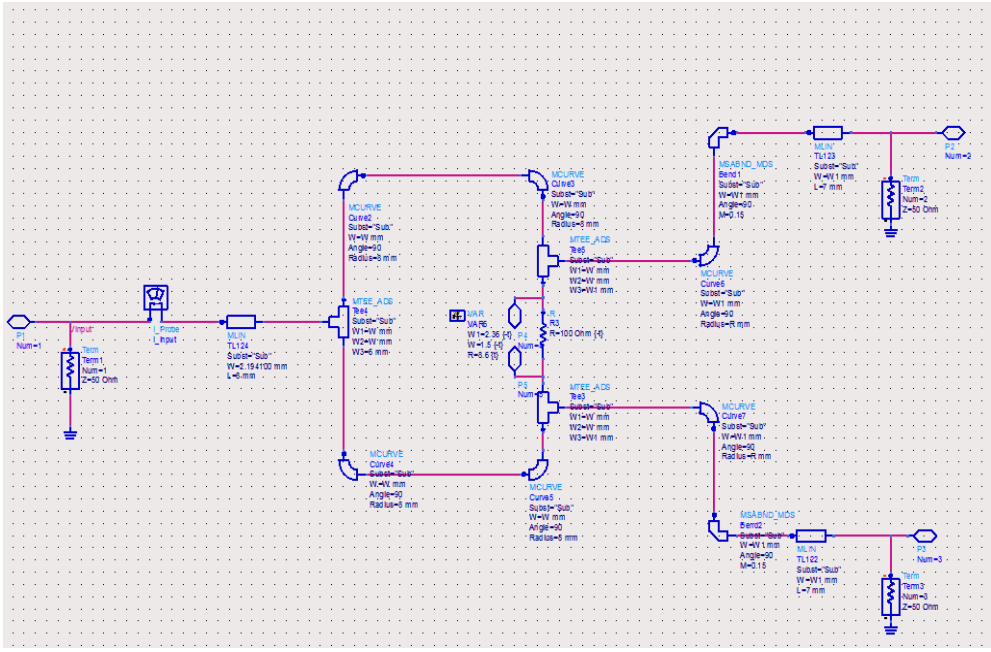
(a)



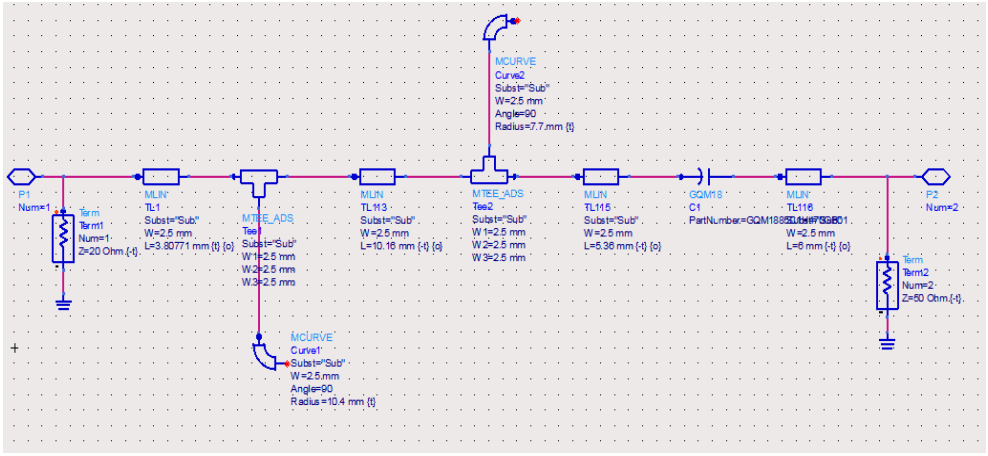
(c)

Figure C.1: (a) power divider network, (b) input matching network, (c) and combining network in ADS circuit schematic.

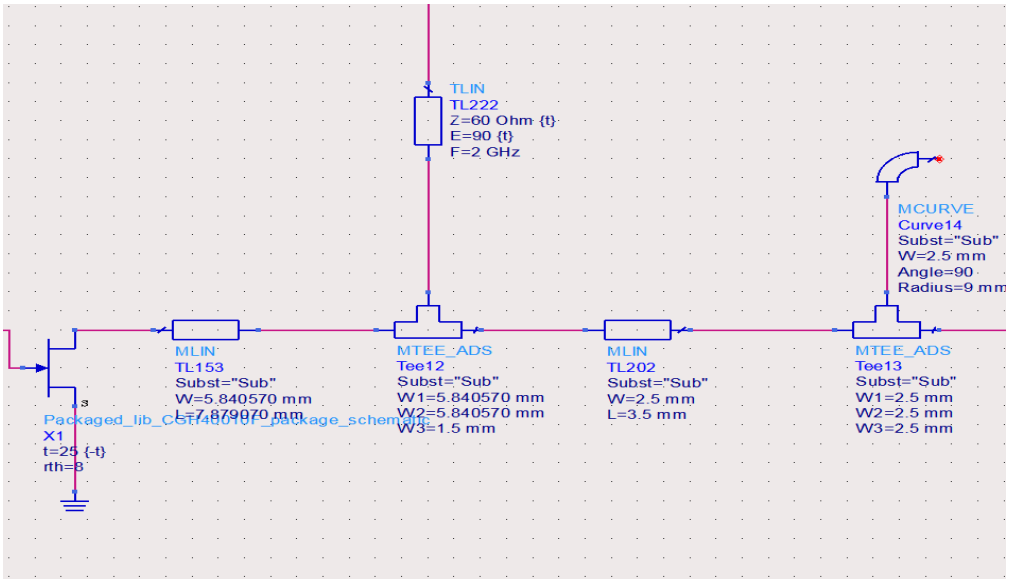
Appendix D



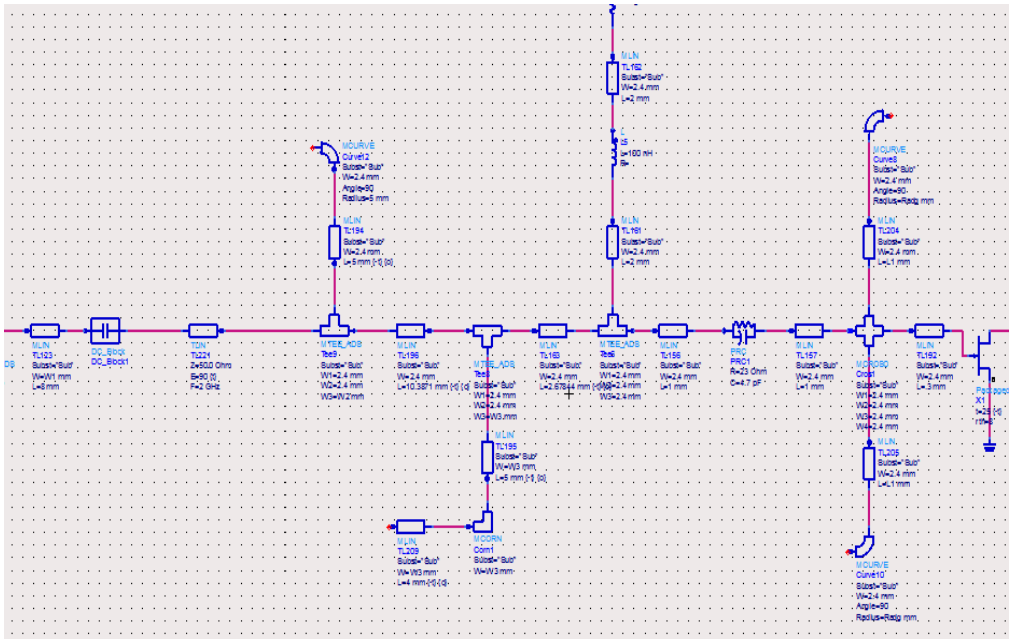
(a)



(b)

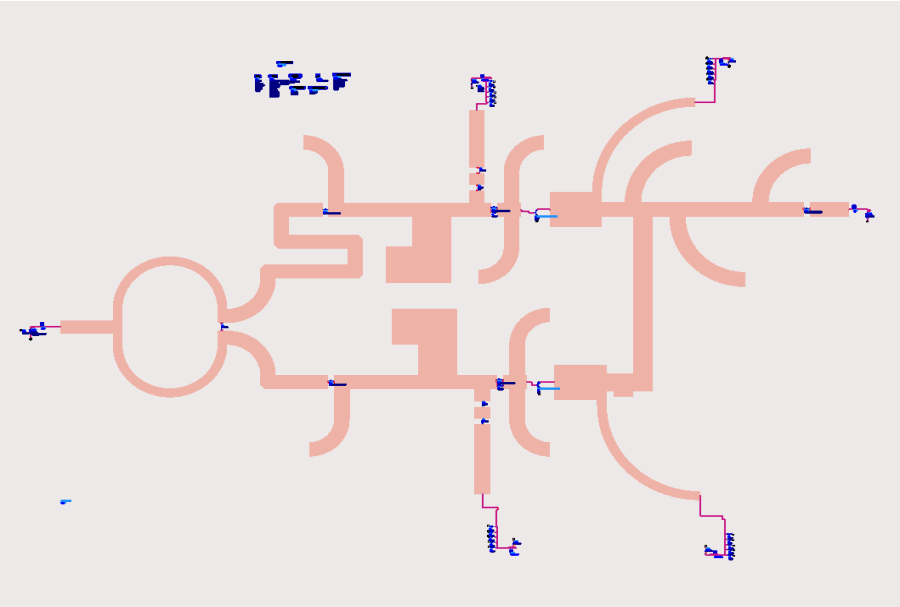


(c)

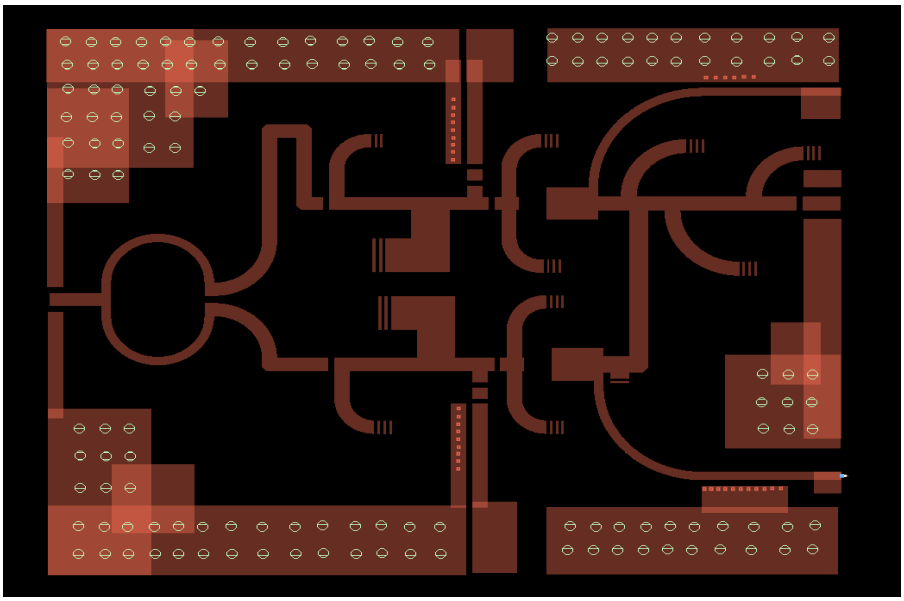


(d)

Figure D.1: (a) power divider network, (b) post-matching network, (c), output matching network and (d) input matching network of the proposed DPA in ADS circuit schematic layouts.



(a)



(b)

Figure D.2: (a) Co-simulation setup and (b) ADS layout of the proposed DPA.

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