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First Measurements of a Prototype of a New Generation Pixel Readout ASIC in 65 nm CMOS for Extreme Rate HEP Detectors at HL-LHC

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***Abstract*—A first prototype of a readout ASIC in CMOS 65 nm for a pixel detector at High Luminosity LHC is described. The pixel cell area is 50×50 μm^2 and the matrix consists of 64×64 pixels. The chip was designed to guarantee high efficiency at extreme data rates for very low signals and with low power consumption. Two different analogue front-end designs, one synchronous and one asynchronous, were implemented, both occupying an area of 35×35 μm^2. ENC value is below 100 e$^-$ for an input capacitance of 50 fF and in-time threshold below 1000 e$^-$. Leakage current compensation up to 50 nA with power consumption below 5 μW. A ToT technique is used to perform charge digitization with 5-bit precision using either a 40 MHz clock or a local Fast Oscillator up to 800 MHz.**

Internal 10-bit DAC's are used for biasing, while monitoring is provided by a 12-bit ADC. A novel digital architecture has been developed to ensure above 99.5% hit efficiency at pixel hit rates up to 3 GHz/cm^2, trigger rates up to 1 MHz and trigger latency of 12.5 μs. The total power consumption per pixel is below 5 μW. Analogue dead-time is below 1%. Data are sent via a serializer connected to a CMOS-to-SLVS transmitter working at 320 MHz. All IP-blocks and front-ends used are silicon-proven and tested after exposure to ionizing radiation levels of 500-800 Mrad.

The chip was designed as part of the Italian INFN CHIPIX65 project and in close synergy with the international CERN RD53 and was submitted in July 2016 for production. Early test results for both front-ends regarding minimum threshold, auto-zeroing and low-noise performance are high encouraging and will be presented in this paper.

I. Introduction

THE High Luminosity LHC accelerator will constitute a new frontier for particle physics after the year 2024. The major experimental challenge resides in the innermost tracking detectors equipped with pixel sensors, for which the dimension on the sensitive area has to be scaled with respect to present LHC detectors. Compared to a CMOS 130 nm process, the 65 nm technology allows more compact digital logic and memories (×4), higher speed (×2), lower digital power per single circuit (×4) and is a mature and stable technology node. For these reasons, the 65 nm CMOS technology is of great interest for the tracking detectors at the HL-LHC experiments. Much R&D work is on-going on the design of new pixel front-end ASIC and significant progress has already been made[1].

This paper will describe a innovative pixel ASIC with a matrix of 64×64 pixels each of dimension 50×50 μm^2, designed by the CHIPIX65 project [2],[3] as a demonstrator of a next generation chip for the Pixel Phase 2 Upgrade, complying with high radiation doses, providing extreme data rates with a compact design, low power consumption and working with low thresholds (below 1000 e$^-$). All the IP-blocks and the analogue front-ends were developed by the CHIPIX65 project and in the framework of the RD53 Collaboration [4],[5]. They were produced and tested proven to be radiation-hard for doses up to 500-800 Mrad.

The chip implements two different analogue front-end designs [5],[6],[7], each occupying half of the pixel matrix, with the following common characteristics: compact design with an area of 35×35 μm^2, low noise with ENC below 100 e$^-$ for an input capacitance of 50 fF (which is the expected value for the pixel sensor to be bump bonded to the chip), low power consumption below 5 μW per pixel, fast rise time allowing correct time-stamp allocation with a bunch crossing frequency of 40 MHz, signal digitization using a Time-Over-Threshold technique (ToT) and leakage current from the sensor compensated up to 50 nA per pixel by using a continuous charge reset in the preamplifier achieved through

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a Krummenacher stage. In order to isolate the analogue front-ends from the digital part, the analogue circuitry is realized in a deep n-well island of 2×2 pixels and routing is protected with shielding layers when in close proximity to the digital circuitry.

A novel digital architecture [9] has been designed in order to maintain a high efficiency (above 99%) at pixel hit rates up to 3 GHz/cm^2, trigger rates up to 1 MHz with a trigger latency up to 12.5 μs. The digital architecture is organized in *pixel regions* (PR), where the hit is stored locally and which is transmitted to the end of column only in the case of an external trigger signal.

Charge information is retrieved from pixels using 5-bit ToT counters and is stored in a centralized latency buffer for transmission to the End Of Column logic in the case of a matching trigger signal. A more detailed description of the CHIPIX65 digital functionality can be found in [9].

The particle detection inefficiency with this architecture is about 0.1% and power consumption is below 5 μW per pixel.

All global biases and voltages are provided by the chip periphery, each one generated by a 10-bit current-steering DAC [11]. All the DAC's receive a stable reference voltage provided by a Band Gap circuit [12]. Each analogue bias is derived from a global current and distributed via a single current mirror to independent bias cells placed at the bottom of each pixel column. From there each bias is propagated to all the pixels through another stage of current mirroring. This architecture is very robust, easily scalable to a large pixel chip while the effect of mismatch is kept to a negligible level. Each voltage and current generated in the chip can be monitored by a 12-bit ADC [5]. All this circuitry, with DAC's, Band Gap circuit, ADC and the bias cells with current mirrors, is enclosed in a single deep n-well in order to isolate them from the digital electronics.

Readout is performed using a column drain protocol with a FIFO for each pixel region column connected to a global dispatcher FIFO that, after 8b/10b encoding, splits the data into 20-bit chunks and sends them to a serializer [5]. Data are transmitted by the chip using a differential buffer which converts the CMOS level into the SLVS JEDEC 400 mV standard. Given the small size of the chip an output rate of 320 MHz for the serialized data is sufficient but higher output rates are possible since both serializer and SLVS transmitter are designed to sustain up to 1.2 Gb/s.

The CHIPIX65 demonstrator was submitted to the foundry in July 2016 for production and was received at the end of September 2016. This paper will describe the first test results obtained in early autumn. This chip constitutes a first milestone before proceeding to the design of a large scale prototype of the RD53 Collaboration in 2017.

II. Prototype overview

A. Analogue front-ends

The CHIPIX65 demonstrator integrates two different analogue front-end architectures:

- a synchronous one [6], with which the first half of the pixel array is equipped (see Fig. 1, label 1)
- an asynchronous one [7], with which the second half of the pixel array is equipped (see Fig. 1, label 2).

A common digital layout and configuration scheme are used instead for all the pixels.

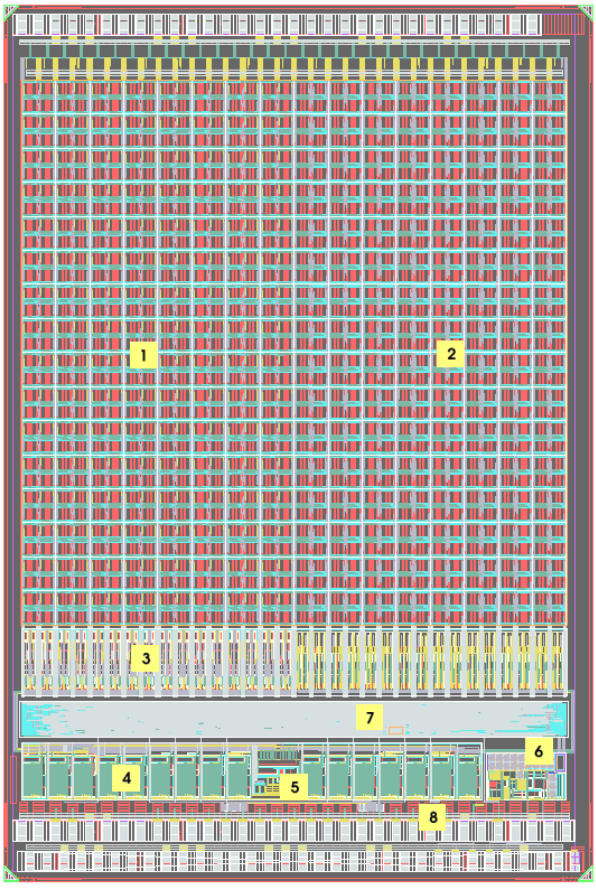

Fig. 1. CHIPIX65 demonstrator layout consists of a 64×64 pixel array (3.5 mm×5.1 mm). Synchronous Front-End Architecture (1), Asynchronous Front-End Architecture (2), Column Bias Cells with current mirrors (3), Global DAC's (4), Band Gap Reference (BGR) (5), monitoring ADC (6), End of Column and high-speed serializer (7), SLVS TX/RX and I/O cells (8).

Both solutions were designed to be radiation-hard and were validated in silicon using small prototypes of 8×8 or dedicated test structures as part of the first CHIPIX65 submission which were fully working after irradiation up to 600-800 Mrad [5],[6],[7],[8].

A schematic block diagram of the synchronous front-end is depicted in Fig. 2. The input stage uses a telescopic-cascode inverting amplifier as a gain stage with two selectable feedback capacitors for charge sensitivity selection. A track-and-latch voltage comparator is used for hit discrimination. A CMOS digital pulse is generated when a signal is above the nominal threshold and synchronized with a 40 MHz clock strobing the latch. A high-frequency pixel-level internally generated clock up to 800 MHz provides fast TOT charge digitization encoding. This is obtained by turning a latch into a VCO (Voltage-Controlled Oscillator).

Compensation of the pixel-to-pixel threshold variations is made by an auto-zeroing circuit based on Output Offset Storage (OOS) between the differential amplifier and the positive-

feedback latch. As a result there is no need for a DAC in each pixel in order to tune the threshold value.

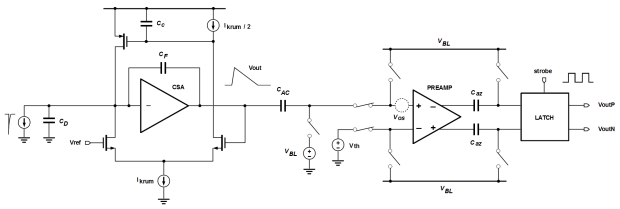

Fig. 2. Synchronous front-end chain. From left to right: charge-sensitive amplifier with Krummenacher feedback, AC coupling and track-and-latch voltage comparator with auto-zeroing obtained with the Output Offset Storage (OOS) technique.

A schematic view of the asynchronous front-end is shown in Fig. 3.

While sharing a common architecture choice regarding the Krummenacher feedback, in this solution different CSA and feedback-network optimizations have been opted for. A folded-cascode inverting amplifier is adopted as the gain stage with the possibility to set the charge sensitivity. A current-comparator is used for hit discrimination. In this case, for the conversion from voltage to current a transconductor stage is used.

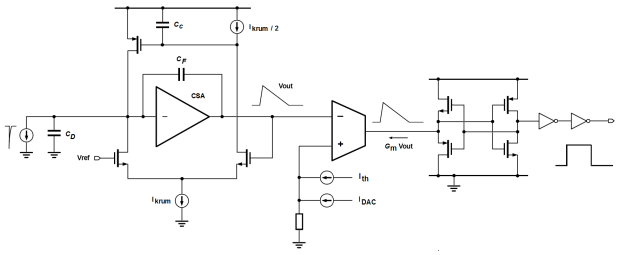

Fig. 3. Asynchronous front-end chain. From left to right: charge-sensitive amplifier with Krummenacher feedback,voltage-to-current transconductor and fast current comparator.

In order to get a full-swing rail-to-rail digital pulse CMOS inverters are also used. The threshold value is defined by a current flowing into a diode-connected MOS device. The global current reference is provided by all pixels while the pixel-to-pixel threshold compensation here is performed using local 4-bit binary-weighted DAC's.

Encouraging results were obtained from the preliminary characterization of the two front-end versions. They are shown in the III.

B. Region digital architecture

A novel region-based digital architecture [9] for latency buffering and trigger matching, able to withstand extended trigger latencies and unprecedented data rates at HL-LHC, has been studied and implemented. Pixels are grouped in *pixel regions* (PR) made of 4×4 pixels, as illustrated in Fig. 4, allowing an improved sharing of resources and overcoming freezing problems seen in early work [10]. Each region includes sixteen analogue front-ends arranged in so-called *analogue islands*. A common digital logic shared among pixels stores hits information, handles the local configuration, performs trigger matching and sends zero-suppressed hit data to the readout block at the chip periphery in the case of a trigger request. Automated digital synthesis and place-and-route tasks were performed on an entire pixel region including analogue front-ends treated as macros. A region-based digital architecture offers many advantages such as the possibility of sharing among pixels common functionalities and temporary storage capabilities. The basic replica-unit layout for clock distribution and pixel array assembling is represented by a single pixel region.

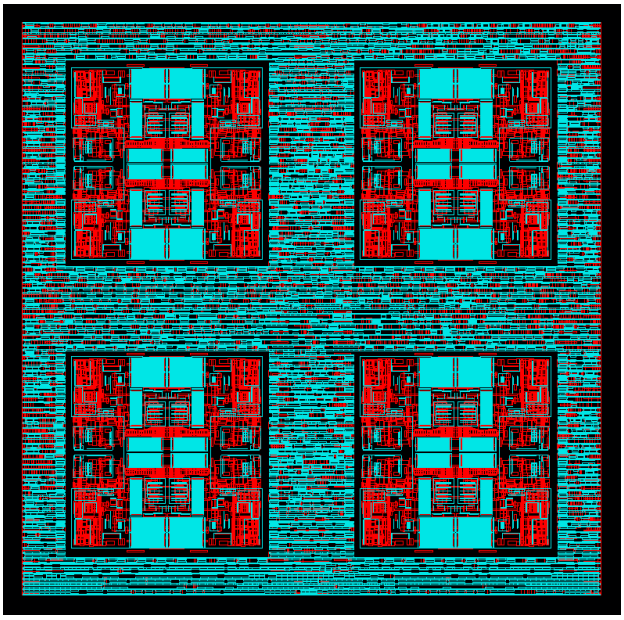

Fig. 4. Layout of a 4×4 pixel region (PR). Every PR comprehends sixteen analogue front-ends organized into 2×2 analogue islands enclosed into a common readout and configuration digital logic.

C. Bias network and monitoring

A schematic of the chosen bias and monitoring network is shown in Fig. 5. Programmable DAC's [11] generate and distribute to the pixel columns all the bias currents and voltages allowing the fine-tuning of the analogue performance.

On-chip monitoring capabilities are provided by a 12-bit ADC. Nine DAC's are utilized for the synchronous front-end, while six are employed for the asynchronous analogue front-ends. For both front-ends a common DAC is used for DC calibration level programming when injecting selected pixel with a test charge signal. A bandgap voltage reference (BGR) [15] provides a 4 μA reference current to all the global DAC's.

D. End of Column readout, chip configuration and I/O

In order to carry out both readout and chip configuration, additional digital blocks are placed in the periphery of the prototype. Macro-Column Drainers (MCD) replicated modules read-out all the triggered data coming from the pixel regions. Each MCD module manages triggers and pixel outputs for a macro-column composed of sixteen pixel regions. The chip normally runs in a triggered mode, but can also be configured

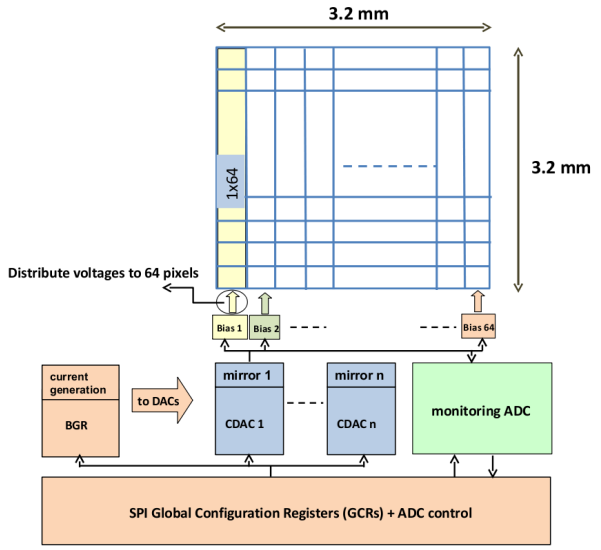

Fig. 5. Block diagram showing bias and monitoring network.

for a trigger-less mode, useful for laboratory testing, especially for taking signals from a bump-bonded sensor exposed to a radiation source. A Fast-OR of all the discriminators of the pixel matrix can be provided as an output signal, a useful option for test-beams. Configuration is performed via fully-duplex synchronous SPI-master/slave transaction, using 24-word SPI frames to read and write pixels and end of column registers including commands for the ADC. The I/O interface uses custom-designed JEDEC-compliant SLVS transmitters and receivers.

III. Test results

The prototype ASIC is wire-bonded to a custom test board developed by the INFN-Torino group which provides test points for measuring global bias voltages and currents. The test board is connected via an FMC connector to a Xilinx KC705 FPGA Evaluation Board running custom firmware which communicates with LabVIEW control and calibration software using a custom UDP-Ethernet protocol.

The rest of this article will be dedicated to the preliminary results obtained so far.

A. Calibration DAC and monitoring ADC

Fig. 6 shows the variation of the output voltage with the DAC code for both measurement and SPICE simulation, with good agreement between the two.

Fig. 7, instead, illustrates the variation of ADC code with respect to the input voltage, for both measurement and SPICE simulations and, again, with good agreement between the two.

B. Synchronous front-end

In order to obtain some information regarding minimum thresholds and the noise of the synchronous front-end, there are two approaches: the first being to hold the threshold fixed and vary the calibration charge while the second is to maintain the calibration charge constant and vary the threshold value.

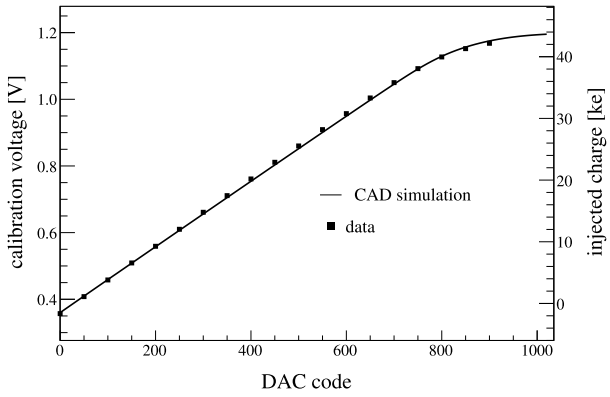

Fig. 6. Test results and CAD simulation data of calibration DAC.

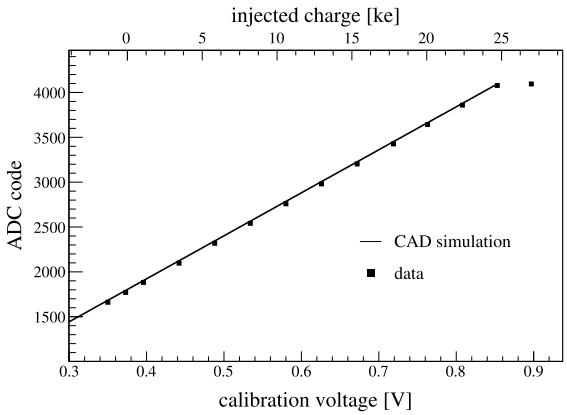

Fig. 7. Test results and CAD simulation data of monitoring ADC.

1) Calibration voltage scans: for this kind of analysis, noise and threshold values are extracted from means and variances distributions. All pixels were tested by performing an auto-zeroing procedure 75 ns long each 100 μs and with a hit efficiency recorded for 100 charge-injection pulses for each point. Measured points are fitted by using an error function (sigmoid) that provides the effective threshold (the mean of the underlying gaussian distribution) and the sigma (Fig.8).

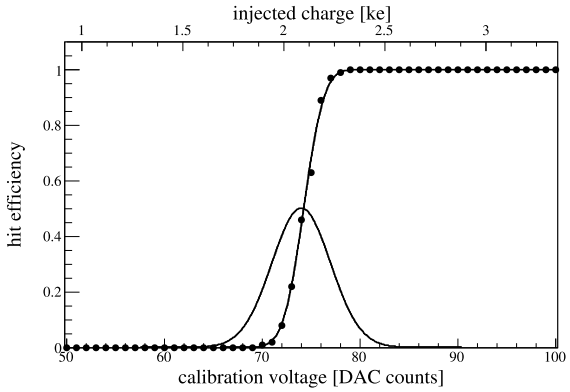

Fig. 8. Measured points fitted by using a sigmoid error function.

In Fig. 9, the calibration voltage scans for all the synchronous front-end pixels are shown together with their as-

sociated fits.

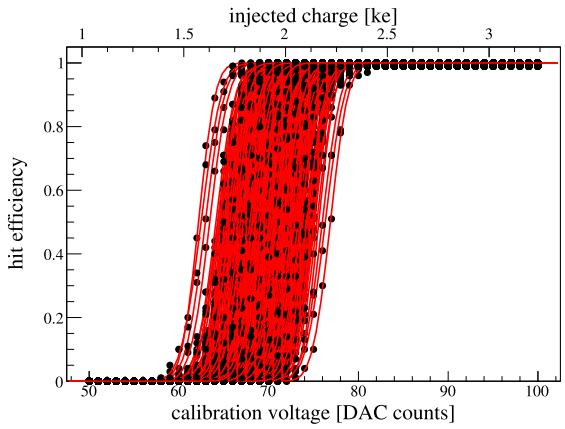

Fig. 9. Calibration voltage scan for all the synchronous front-end pixels.

In Fig. 10, the results of fixed-charge threshold scans are presented. Effective threshold measured for different values of fixed global threshold are shown for a ∼2000 e$^-$ fixed injected charge.

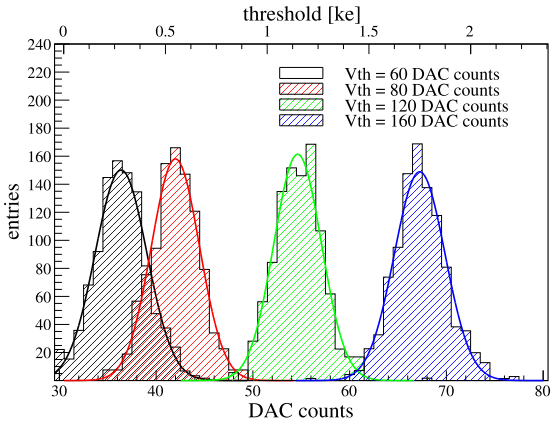

Fig. 10. Distribution of effective threshold measured for different values of fixed global threshold for the synchronous front-end.

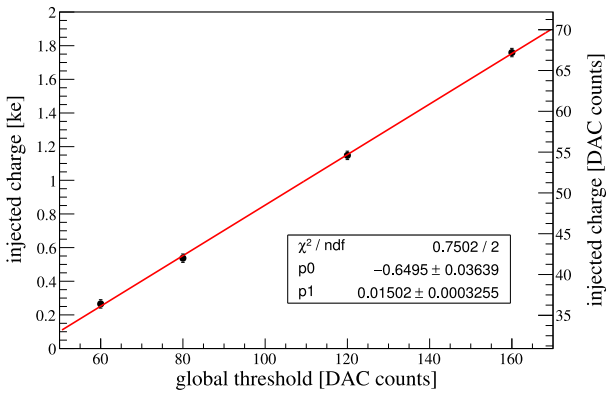

Fig. 11. Injected charge vs. global threshold with linear fit.

The residual latch dynamic offset value of about 100e$^-$ RMS is in good agreement with CAD simulations (∼70 e$^-$ RMS latch dynamic offset). The results demonstrates that the auto-zeroing process is working correctly.

In Fig. 11 the peak of the distributions in Fig. 10 is plotted against global threshold with a clearly linear behaviour as seen from the quality of the fit.

In Fig. 12 ENC (Equivalent Noise Charge) measured for different values of fixed global threshold is depicted and shows, as expected, a constant behavior with threshold values. ENC ∼45 e$^-$ RMS is in good agreement with CAD simulations and therefore that very low noise performance is assured despite intense latch and region-logic switching activity.

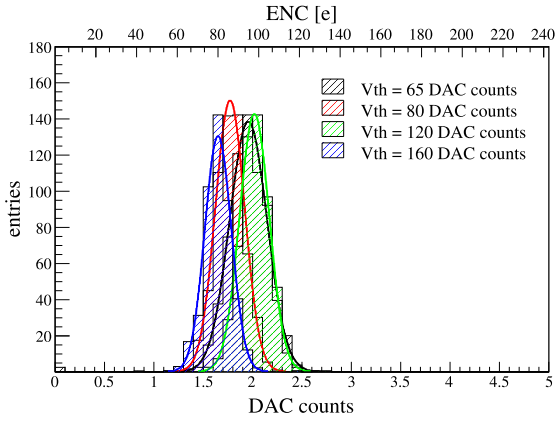

Fig. 12. Equivalent Noise Charge (ENC) values measured for different values of fixed global threshold for the synchronous front-end. A minimum threshold of ∼250 e$^-$ has been used for all the pixel in the array.

2) Threshold voltage scans: in Fig. 13, threshold voltage scans are performed from a value above the nominal baseline and then reduced in order to verify the minimum detectable charge: as expected, pixels always fire due to noise fluctuations below ∼250 e$^-$.

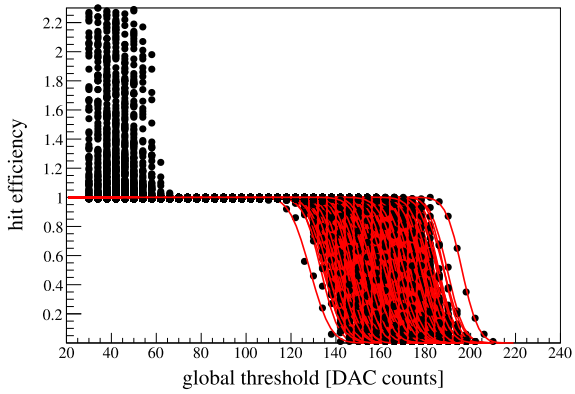

Fig. 13. Fixed-charge scan curves.

Charge digitization is performed using a Time-Over-Threshold technique. Fig. 14 shows the linearity for the 5-bit fast ToT with respect to the calibration voltage for a single pixel.

Fig. 15 shows the distribution of the slope of the linear fit of the ToT vs. the calibration voltage for all pixels.

Assuming a frequency of 320 MHz, a slope dispersion of about 10% is expected due to mismatches in the analogue part, and as such the measurements match the CAD simulations.

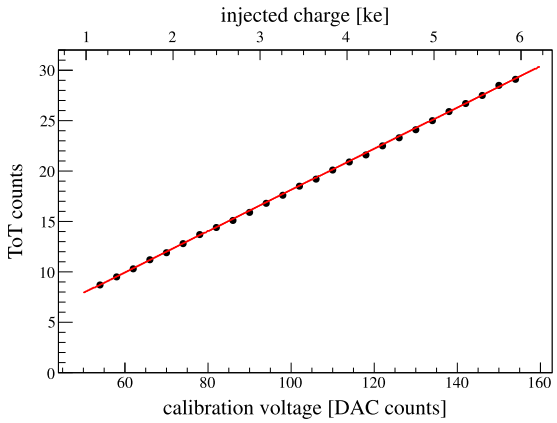

Fig. 14. Linearity of the ToT of a single pixel.

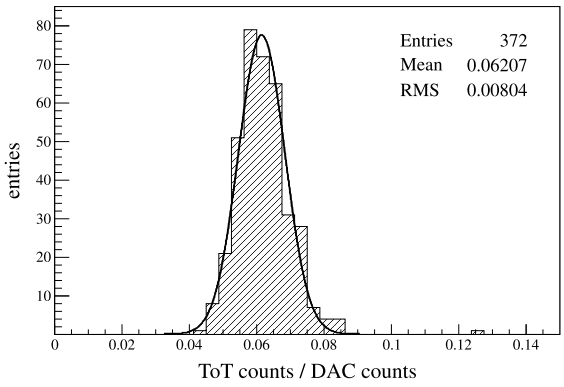

Fig. 15. Distribution of values of ToT.

C. Asynchronous front-end

The second half of the pixel array is implemented with a continuous-time front-end, equipped with a threshold discriminator architecture based on a low power trans-impedance amplifier for fast switching operation. The problem of the threshold dispersion is addressed by means of a local, in-pixel circuit for threshold correction, based on a 4-bit binary weighted DAC.

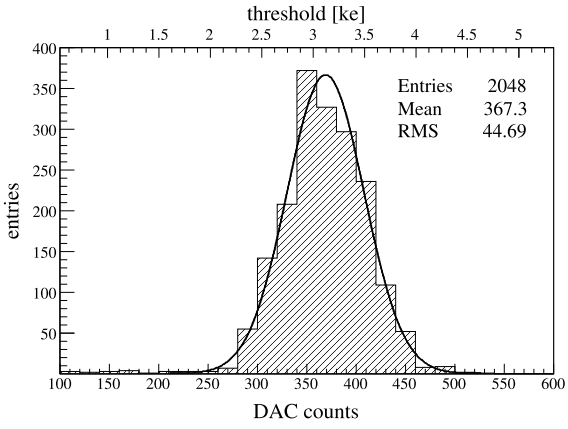

Fig. 16. Distribution of effective threshold measured for different values of fixed global threshold for the asynchronous front-end.

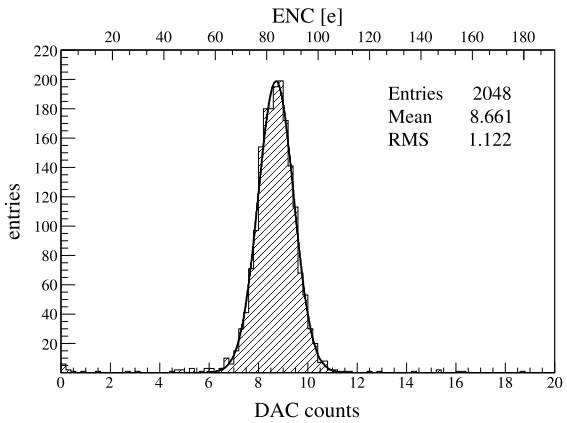

Fig. 17. Equivalent Noise Charge (ENC) values measured for different values of fixed global threshold for the asynchronous front-end.

First tests indicate that all pixels are fully working. Preliminary results show a $\sim$400 e^- threshold dispersion without trimming with a ENC $\sim$85 e^-, in agreement with CAD simulations.

IV. Conclusions

A prototype of a new-generation pixel readout ASIC has been designed as part of the Italian INFN CHIPIX65 project. The CHIPIX65 demonstrator is composed of a 64×64 pixel matrix with a cell size of 50×50 μm with a full system integration of silicon proven IP-blocks developed by the INFN for RD53 Collaboration and two different analogue front-end designs (synchronous and asynchronous architecture). A digital on top design methodology was implemented. The samples were received at the end of September 2016 and preliminary tests started in Torino in October 2016. Highly encouraging results from these preliminary tests were achieved:

- the two AFE designs, all the IP blocks and the digital architecture are fully working;
- $\sim$ 250 e^- minimum threshold with 100 e^- residual offset after auto-zeroing for the synchronous front-end pixels;
- low-noise performance (ENC $\sim$45 e^-) was obtained for both designs despite intense digital activity demonstrating successful integration and insulation between analogue and digital circuitry.

Irradiation tests are foreseen for early 2017; bump-bonding with 3D sensors (FBK, Fondazione Bruno Kessler, Trento, Italy) and planar sensors (Hamamatsu, Japan) are planned.

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REFERENCES

[1] N. Demaria, *Recent ASICs developments in 65 nm CMOS technology for high energy physics experiments*, 2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS), pag.380-383, DOI:10.1109/ICECS.2015.7440328.

[2] N. Demaria et al. *RD53 Collaboration and CHIPIX65 Project for the development of an innovative Pixel Front End Chip for HL-LHC*, PoS IFD 2014, 010 (2015).

[3] CHIPIX65 project web site: http://chipix65.to.infn.it

[4] RD53 Collaboration web site: https://rd53.web.cern.ch/RD53

[5] N. Demaria, G. Dellacasa et al. *CHIPIX65: developments on a new generation pixel readout ASIC in CMOS 65 nm for HEP experiments*, IEEE Conference Publications (2015), 6th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI), 2015, pag. 49-54, DOI: 10.1109/IWASI.2015.7184947.

[6] E. Monteil, L. Pacher, A. Paternò, N. Demaria, A. Rivetti, M. Da Rocha Rolo, F. Rotondo, C. Leng, J. Chai, *A synchronous analogue very front-end in 65nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC*, JINST (2016).

[7] L. Ratti, F. De Canio, L. Gaioni, M. Manghisoni, V. Re, G. Traversi, *An asynchronous front-end channel for pixel detectors at the HL-LHC experiment upgrades*, Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2015 IEEE, doi: 10.1109/NSSMIC.2015.7581981.

[8] L. Pacher, E. Monteil. A. Rivetti, N. Demaria, M. Da Rocha Rolo, *A Low-Power Low-Noise Synchronous Pixel Front-End Chain in 65 nm CMOS Technology with Local Fast ToT Encoding and Autozeroing for Extreme Rate and Radiation at HL-LHC*, 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference.

[9] A. Paternò, L. Pacher, S. Marconi, N. Demaria, A. Rivetti, G. Dellacasa, P. Placidi, *New Development on Digital Architecture for Efficient Pixel Readout ASIC at Extreme Hit Rate for HEP Detectors at HL-LHC*, 2016 IEEE Nuclear Science Symposium and Medical Imaging Conference.

[10] E. Conti, J. Christiansen, P. Placidi, S. Marconi, T. Hemperek, *Simulation of a digital pixel readout chip architectures with the RD53 SystemVerilog-UVM verification environment using Monte Carlo physics data*, JINST (2016), Vol.11.

[11] G. De Robertis et al., *Design of a 10-bit segmented current-steering Digital-to-Analogue converter in CMOS 65 nm technology for the bias of new generation readout chips in high radiation environment*. Journal of Instrumentation (JINST), Vol.11 (2016), C01027.

[12] G. Traversi, F. De Canio, L. Gaioni, M. Manghisoni, L. Ratti, V. Re, *Design of bandgap reference circuits in a 65 nm CMOS technology for HL-LHC applications*, JINST(2010), C02004(2015).

[13] S. Marconi et al., *Reusable SystemVerilog-UVM design framework with constrained stimuli modeling for High Energy Physics applications*, 2015 IEEE International Symposium on Systems Engineering (IEEE ISSE).

[14] E. Conti et al., *Simulation of Digital Pixel Readout Chip Architectures for the LHC Phase 2 Upgrades with a SystemVerilog-UVM Verification Environment*. Journal of Instrumentation (JINST), Vol.11 (2016), C01069.

[15] G. Traversi et al., *Design of bandgap reference circuits in a 65 nm CMOS technology for HL-LHC applications*. Journal of Instrumentation (JINST), Vol.10 (2015), C02004.