A Selective Mapper for the Mitigation of SETs on Rad-Hard RTG4 Flash-based FPGAs

A Selective Mapper for the Mitigation of SETs on Rad-Hard RTG4 Flash-based FPGAs

L. Sterpone, S. Azimi, B. Du

***Abstract*—This paper proposes a mapping tool for selectively mitigate radiation-induced Single Event Transient phenomena within the silicon structure of Microsemi RTG4 Radiation hardened Flash-based FPGAs. Experimental results on three benchmark circuits demonstrated effective SET mitigation.**

I. Introduction

THE aggressive scaling trend in the nanometer technologies has significantly impacted the rates of Single Event Transients (SETs) faults within electronic circuits. When Flash-based FPGA devices are considered, the main concern is related to radiation-induced voltage glitches or SETs in the combinational logic. SETs may propagate through the circuit logic and be sampled by register or memory elements. If latched, they provoke single or multiple errors depending on the fan-out stems from the radiation-affected point.

The junction charge collection mechanism is the basic mechanism of the SET generation. When a charged particle crosses a junction area, it generates an amount of current that will cause a voltage glitch of elevated magnitude. The voltage glitch propagates through logic and routing resources for several logic levels and the SET may become indistinguishable from normal signals. The transient pulse, after propagating through the logic, can be sampled by a storage element creating a bit-flip, also called Single Event Upsets (SEUs), that can be propagated through the circuit up to the outputs and leading to an error.

Recent experiments performed in Flash-based FPGAs show an evident SET pulse width and amplitude modulation through the traversed routing and logic cells. In particular, the experiments performed in [2] [3] shows that the final SET observed at the input of a storage element, is always dependent on the propagation phenomena. As described in [4] the SET phenomena can be described in two phases: the generation of the SET due to a particle-strike into a sensitive node and the subsequent pulse propagation to the input of a user memory element, typically a Flip-Flop. The initial stages is correspondent to the formation of the SET pulse shape, its characteristics depend on different factors principally including the Linear Energy Transfer (LET) of the affecting particle, the incidence angle and the technology. In case the initial SET starts the propagation through the first logic states, the further propagation until the first encountered Flip-Flop is affected by different electrical phenomena that may change the SET pulse width broadening or filtering it in relation to the traversed routing and logic cells. Thus, it is today mandatory to evaluate and measure the effective SET pulse propagation so the most effective mitigation techniques can be adopted without additional timing penalties.

The protection of the user memory and registers against these errors required the adoption of several mitigation solutions that have been previously proposed such as Triple Modular Redundancy (TMR) and Error Correction Code (ECC). However, these techniques were not able to efficiently protect circuits versus SET [5][6][7][8]. Thanks to the technology characterization performed by means of electrical pulse injection and radiation tests, analytical methods for the modeling and the mitigation of multiple SETs has been recently proposed. These methodologies have been effectively tested through heavy-ions experimental radiation test, evaluating the mitigation capabilities of place and route-based SET mitigation algorithm we proposed in [9][10].

On the other side, in order to cope with the increasing aerospace requirements in relation to the Total Ionization Dose (TID), a new radiation-hardened Flash-based FPGA family, RTG4, has been recently manufactured [11]. The main advantage of this Flash-based FPGA technology is to guarantee a TID tolerance higher that 100 krad thanks to the complementary or C-Flash, configuration cell that, as demonstrated in [12], is able to tolerate higher level of Ionization Dose rather then the previous N-Flash. When transient radiation effects are considered, the major advantage of the RTG4 family is the availability of embedded SEU and SET mitigation scheme that rely on Triplicated Flip-Flop architecture and on internal SET mitigation scheme. Although the advantages provided by the RTG4 device family are relevant, the nowadays implementation tools do not provide an effective manageable of the SET mitigation solution since the implementation tool does not allow the designer to effectively select the proper redundancy and SET filtering setup.

The main contribution of the present work is a new mapper algorithm able to selectively introduce SET-filtering scheme while optimizing the circuit performance and reducing the overall SET sensitivity. In details, the SET-filtering of the proposed approach is applied selectively to the relevant logic gate thus reducing the sensitive area and the performance degradation. This represents an enormous benefit versus previously used implementation tools that apply SET-filtering and guard-gate for all the user memory or Flip-Flop resources. Besides, the algorithm, which has been implemented as a software tool, is based on the elaboration of the RTG4 cell library and it is interfaced with the available tools.

II. Background On RTG4 Architecture

The RTG4 Flash-based FPGA technology is based on an array of Flash-technology based radiation tolerant logic elements embedding some hard ASIC blocks such as RAM memory modules and DSP blocks. All the elements are clustered inside the fabric and interconnected by a clustered routing architecture. The embedded registers have the possibility to mitigate Single Event Transients (SETs) while memories have a built-in error detection and correction mechanism (EDAC). The major resources of the RTG4 FPGA architecture are: logic elements, interface logic elements and I/O modules [13]. For the purpose of this work we concentrated exclusively on the logic elements that compose the larger part of the FPGA resources [16].

The RTG4 logic element consists of a 4-inputs Look-Up Table (LUT), a self-corrected Triple Modular Redundancy (S-TMR) Flip-Flop and a dedicated carry chain as illustrated in the scheme reported in Figure 1.

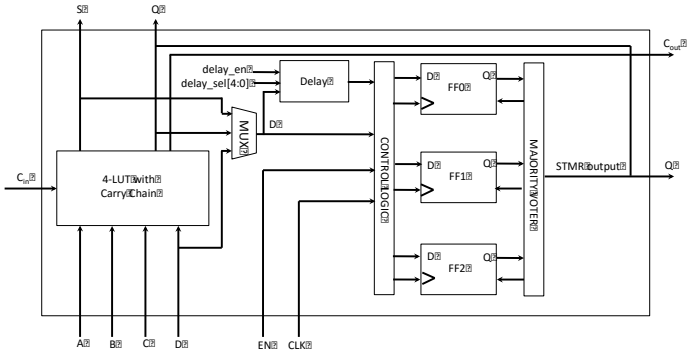

Fig. 1. The functional block diagram of logic element of the RTG4 Flash-based FPGA family.

The 4-LUT with carry chain logic can be configured to any 4-input combinational function where the LUT output is XORed with the carry input signal (C_{in}). The output S is the principal output used when the LUT implements a combinational function. The carry chain has a specific hardwired interconnection between the logic elements able to reduce the propagation delay through the carry chain. The main innovation of the RTG4 logic cell consists in the SET-mitigated asynchronous self corrected TMR-D Flip-Flop (S-TMR). In particular each STMR Flip-Flop has an Asynchronous majority voter logic that ensures SEU immunity when the SET pulse width at the input D of the functional logic block is comprised within the user defined SET filtering delay coefficient (*delay_sel*). The RTG4 implementation tools are used in order to set the mitigation properties. When the SET filtering is activated, the timing performances of the circuits can be drastically reduced. The degradation is proportional with the width of the SET delay.

Whatever the RTG4 architecture provides the user definition of the SET filtering capability, the commercial tools are not able to provide the effective width of the SETs. In our approach we rely on the Single Event Transient Analyzer (SETA) approach for obtaining an effective estimation of the SET broadening through the logic paths.

III. The Developed SET mitigation Mapper

The developed environment consists on the diagram illustrated in Figure 2. In order to apply the proposed algorithm it is preliminary required to use a commercial-based tool chain able to generate a pre-layout netlist (*EDIF netlist*) where the netlist file contains the full functional description of the circuits using the RTG4 library cells. All the FPGA implementation tools commonly generate this file.

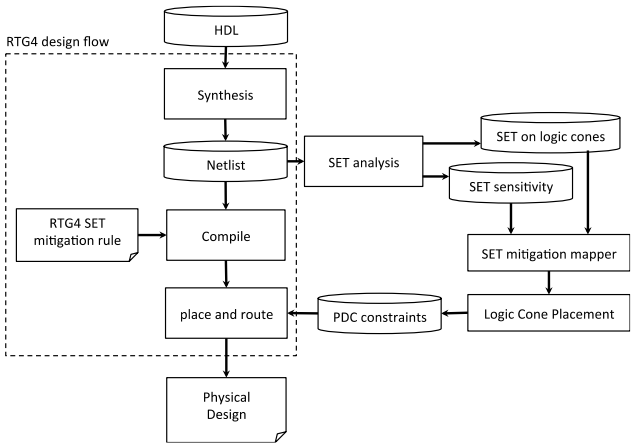

Fig. 2. The integrated implementation flow of the proposed SET mitigation mapper tool.

Our method starts elaborating the EDIF netlist of the circuits by means of the SETA tool, which consist of an algorithm able to perform the exhaustive evaluation of SET effects on all the sensitive nodes of a circuit mapped on a Flash-based FPGA. Since the SETA tool requires the characterization of the FPGA cells in order to provide an accurate analysis, in the present work we generated a preliminary logic cells characterization by means of the post-layout RTG4 simulation library. The results of the SETA tool are two profiles database: a SET sensitivity database including a broadening coefficient for each used resources and a database including the logic cone with shared logic gates.

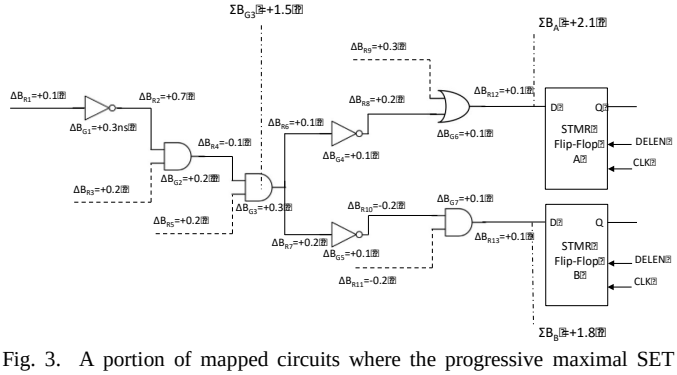

Fig. 3. A portion of mapped circuits where the progressive maximal SET broadening width contribution (ΔB) and the total SET broadening contribution (ΣB) are represented for each logic gate and routing segment. Please note that without any filtering scheme the maximal SET width at the input of the Flip-Flop A and B is 2.1 ns and 1.8 ns respectively.

An example of the information contained into the two databases is illustrated in Figure 3, where the broadening coefficients are provided for each logic gate as ΔB_{Gi} with *i* representing the gate index and for each routing net as ΔB_{Rj}

with *j* representing a specific routing segment. Each coefficient is computed by the SETA tool as the maximal SET width observed by the SET pulse at the input of a given resource and it is measured in nanoseconds. A positive value corresponds to a broadening, while a negative value is related to the filtering of the SET. The database provides further information related to the entire broadening contribution of each logic path, represented by ΣB. The broadening contribution is calculated for each Flip-Flop element and for all the gates shared between two or more logical path. As illustrated in Figure 3, the gate G3 has a maximal broadening contribution of 1.5 ns, which is calculated as the sum of the maximum broadening coefficient of the fan-in logic path. The Flip-Flops A and B have a maximal broadening contribution of 2.1 ns and 1.8 ns respectively.

A. SET mitigation mapper

Previously developed Flip-Flop-based SET filtering methods insert a guard gate logic structure on the input of the selected Flip-Flop [14]. By this way the Flip-Flop is filtering any type of SET reaching its input and having SET width lower than the filtering delay. This solution has two main disadvantages. The former is related to the need of insert the filtering scheme at the input of all the selected Flip-Flops provoking a drastic increase of the area overhead. The latter is related to the performance degradation, since the guard gate scheme requires not only a given number of gates to implement the SET-filtering scheme but also at least 4 gates for each Flip-Flop for implementing the guard-gate structure, as it is illustrated in Figure 4.a.

The proposed mapper algorithm inserts the SET-filtering scheme illustrated in Figure 4.b for all logic gates shared between logic cones. The identification of the insertion point is performed by the SET mitigation mapper, which calculates the effective SET-filtering delay on the basis of the Flip-Flop SET filtering capabilities. As illustrated in Figure 5, the SET mitigation algorithm inserts a filtering scheme able to filter pulses having as maximal width 1.6 ns by inserting the proper filtering logic gates after the shared gate G3. As illustrated in the example of Figure 5, the filtering scheme nullifies any type of SET coming from the top part of the logic cones. On the other side the SET broadening contributions at the Flip-Flop A and B, are reduced to 0.6 and 0.3 ns, these SET widths can easily be filtered by the internal RTG4 register cell pulse filtering.

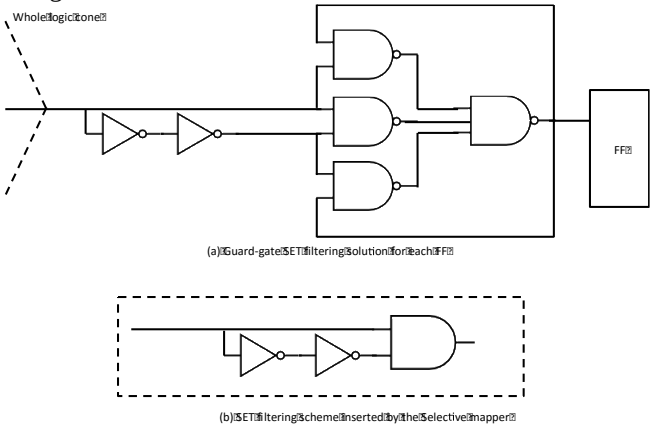

Fig. 4. Traditional Flip-Flop based guard-gate and SET-filtering solution (a) compared to the SET-filtering scheme inserted by the selective mapper on logic gates shared by logic cones (b)

IV. EXPERIMENTAL RESULTS

The experimental analysis of the proposed method has been performed on three different ITC'99 benchmark circuits implemented on a Microsemi RTG4 RT4G150-CG1657 Rad-Hard Flash-based FPGAs [15]. The three benchmarks have been implemented in four different versions: original unhardened, commercial tool-based SET filtering *(_SET*), Flip-Flop-based guard-gate solution (*_GG*) and the proposed approach (*_SEL_MAP*). The circuit area characteristics are reported in Table I, we applied a guard gate mitigation of 1.5 ns and the commercial tool has been settled to 0.6 ns.

As it possible to notice, the proposed solution minimize the area overhead reaching an average of 25% with respect to the original circuit without mitigation. This percentage is extremely effective if compared with the guard-gate solution, which has as an overhead of about 135%.

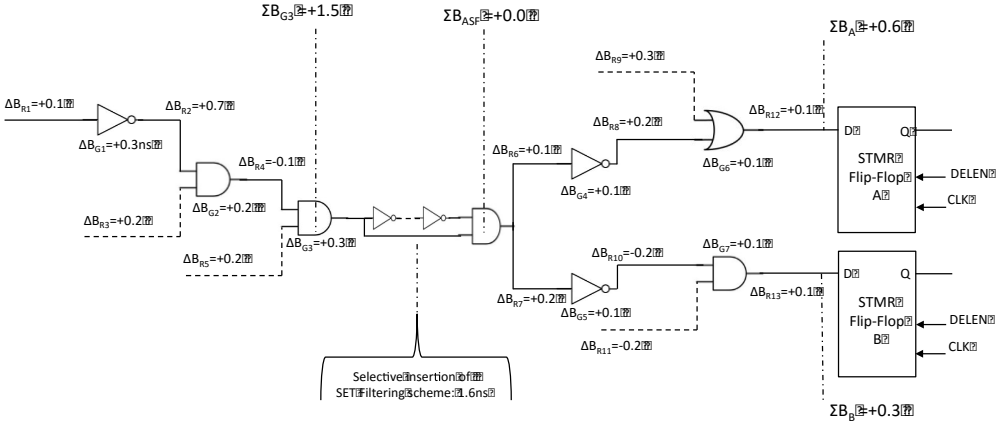

Fig. 5. The proposed selective insertion of the SET-filtering scheme. Please note that the maximal SET of 0.6 ns on the Flip-Flop A and 0.3 ns on the Flip-Flop B are filtered by the internal RTG4 SET logic filtering.

Table I. Characteristics of the implemented circuits

Circuit	4LUTs [#]	DFF [#]	Area Overhead [%]	Max Clock Period [ns]
B05	205	46	-	10.49
B05_SET	205	46	0	11.22
B05_GG	481	46	134	16.31
B05_SEL_MAP	255	46	24	12.10
B12	378	119	-	8.47
B12_SET	378	119	0	9.40
B12_GG	1,092	119	189	15.45
B12_SEL_MAP	502	119	33	9.82
B14	1,607	216	-	21.14
B14_SET	1,607	216	0	22.09
B14_GG	2,903	216	81	28.44
B14_SEL_MAP	1,895	216	18	22.20

Besides, considering the timing characteristics of Table I, it is possible to observe that all the proposed techniques introduce a not negligible timing overhead. However, the proposed approach has a timing overhead lower than 10%.

The SET mitigation capabilities have been evaluated by means of SET fault simulation. We evaluated the injection of 10,000 SETs in random locations and sensitive nodes of the benchmark circuits. The SETs have been injected with a pulse width between 0.01 ns and 1.00 ns in all the possible sensitive points of the netlists. During the simulation-base fault injection the circuits have been stimulated with input random input patterns. The results have been classified as follow: SET provoking erroneous circuit behavior (*Observed SET*) and SET filtered.

Table II. SET fault simulation results

Circuit	Observed SET [%]	Filtered SETs [%]
B05	85	15
B05_SET	32	68
B05_GG	12	88
B05_SEL_MAP	1	99
B12	87	13
B12_SET	33	67
B12_GG	16	84
B12_SEL_MAP	3	97
B14	89	11
B14_SET	36	64
B14_GG	15	85
B14_SEL_MAP	3	97

As it is possible to notice from the achieved results, the proposed solution performs a mitigation that is 4 times better the guard-gate solution. It is necessary to mention, that the actual results are related to the commercial solution that does not allow a SET filtering delay greater than 0.6 ns.

V. Conclusions and Future works

In this paper we present a selective mapper tool for implementing SET resilient circuits on state-of-the-art radiation-hardened Flash-based FPGAs. The solution we propose is able to minimize the impact on the performances by reducing the area overhead and it is able to guarantee an optimal protection versus SET pulses. In particular our approach is able to mitigate SET one order of magnitude better than available solutions maintaining the area overhead within a reasonable level. As future research we plan to execute proton radiation test experiments to completely validate the proposed design method

References

[1] J. J. Wang, N. Rezzak, D. Dsilva, J. Jia, A. Cai, J. McCollum, E. Hamdy, "A Novel 65 nm Radiation Tolerant Flash Configuration Cell Used in RTG4 Field Programmable Gate Array", IEEE Transactions on Nuclear Science, Vol. 65, No. 6, December 2015.

[2] S. Rezgui, R. Won, J. Tien, "SET Characterization and Mitigation in 65-nm CMOS Test Structures", IEEE Transactions on Nuclear Science, Vol. 59, No. 4, August 2012

[3] Wang J. J., Samiee, S., H.-S. Chen, Huang C-K., M. Cheung, J. Borillo, S. N. Sun, Cronquist B., J. McCollum, "Total Ionizing dose effects on Flash-based Field Programmable Gate Array", IEEE Transactions on Nuclear Science, Volume 51, Part 2, Dec. 2004, Page 3759 – 3766.

[4] S. Rezgui, J. J. Wang, Y. Sun, B. Cronquist and J. McCollum, "Configuration and routing effects on the SET propagation in Flash-based FPGAs", IEEE Transaction on Nuclear Science, Vol. 55, No. 6, pp. 3328 – 3335, Dec. 2008.

[5] M. Berg, H. Kim, M. Friendlich, C. Perez, C. Seidleck, K. LaBel, R. Ladbury, "SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA Devices", IEEE Transactions on Nuclear Science, Vol. 58, Issue 3, Part 2, pp. 1015 – 1022.

[6] L. Sterpone, N. Battezzati, V. Ferlet-Cavrois, "Analysis of SET Propagation in Flash-based FPGAs by means of Electrical Pulse Injection", IEEE Transactions on Nuclear Science, Vol. 57, Issue 4, Part. 1, 2010, pp. 1820 – 1826.

[7] N. Battezzati, S. Gerardin, A. Manuzzato, D. Merodio, A. Paccagnella, C. Poivey, L. Sterpone, M. Violante, "Methodologies to Study Frequency-Dependent Single Event Effects Sensitivity in Flash-based FPGAs", IEEE Transactions on Nuclear Science, Vol. 56, Issue 6, Part 1, 2009, pp. 3534 – 3541.

[8] L. Sterpone, N. Battezzati, F. L. Kastensmidt, R. Chipana, "An Analytical Model of the Propagation Induced Pulse Broadening (PIPB) Effects on Single Event Transient in Flash-based FPGAs", IEEE Transactions on Nuclear Science, Vol. 58, Issue 5, Part 2, 2011, pp. 2333 – 2340.

[9] L. Sterpone, V. Ferlet-Cavrois, D. Merodio Codinachs, C. Poivey, "SETA: A New Analytical Tool for Single Even Transient Analysis on Flash-based FPGAs", RADEC 2012 proceedings.

[10] Z. Wang, M. Karpovsky, A. Joshi, "Reliable MLC NAND Flash memories based on nonlinear t-error-correcting codes", Dependable Systems and Networks (DSN), 2010, pp. 41- 50

[11] M. P. Baze, S. P. Buchner and D. McMorrow, "A Digital CMOS Design Technique for SEU hardening", IEEE Transactions on Nuclear Science, 2000, Issue 6, pp. 2603 – 2608.

[12] Microsemi aa.vv., "Using Synplify to Design in Microsemi Radiation-hardened FPGAs", Applicatio Note AC139, 2012, pp. 9.

[13] F. Abate, L. Sterpone, M. Violante, F. L. Kastensmidt, "A study of the Single Event Effects impact on functional mapping within Flash-based FPGAs", IEEE Design, Automation and Test in Europe, 2009, pp. 1226 – 1229.

[14] L. Sterpone, N. Battezzati, "On the mitigation of SET broadening effects in Integrated Circuits", IEEE Design and Diagnostics of Electronic Circuits and Systems, 2010, pp. 36 – 39.

[15] www.opencores.org

[16] UG0574 Userguide, "RTG4 FPGA Fabric", 114 pp, 2015.