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# Transmitter made up of a Silicon Photonic IC and its Flip-Chipped CMOS IC Driver Targeting implementation in FDMA-PON

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***Abstract* - We report on the design, fabrication and characterization of a reflective transmitter targeting implementation in Passive Optical Networks (PON) with Frequency Division Multiplexed Access (FDMA). It is made up of a Silicon Photonic Integrated Circuit (Si-PIC) comprising a Reflective Mach Zehnder Modulator (R-MZM) and its flip chipped CMOS Electronic Integrated Circuit (EIC) driver, the two ICs being interconnected by means of high density and low parasitic copper micro pillars. Several transmissions, in an FDMA PON context, are successfully demonstrated using 500MBaud QPSK and 16-QAM modulated subcarriers, achieving Bit Error Rate (BER) below $2.10^{-3}$. For QPSK-modulated subcarriers (respectively 16-QAM), the available access frequency bandwidth is measured to be [1-7GHz] (respectively [2-4GHz]) with an available loss budget of 9dB (respectively 5dB). Improvements of the Si-PIC are further identified to achieve compliancy with 31dB ODN loss.**

***Index Terms*—PON, FDM/FDMA, Silicon Photonics, CMOS electronics, 3D stacking, micro-pillars, Reflective MZM, QAM modulation, Faraday Rotator Mirror effect.**

## I. Introduction

Frequency Division Multiple Access (FDMA) was proven to be an efficient architecture compliant with ITU-T class N2, as defined in the XG-Passive Optical Network (PON) standard (up to 40km and a 31 dB loss budget for the Optical Distribution Network-ODN) [1][2]. The upstream transmissions from the users' Optical Network Units (ONUs) to the Central Office (CO) receiver were made using off-the-shelf $LiNbO_3$ modulators and Semiconductor Optical Amplifiers (SOAs) as the ONUs' transmitters. In order to meet the challenges of the mass market PON application, the ONU must be manufactured in very large scale and at low cost. In [3], we proposed to implement the ONU transmitter and receiver using Si-Photonics and CMOS electronics. We report here on the design, fabrication and experimental demonstration of such an ONU transmitter. Thanks to the latter, an upstream transmission can be established from the ONU to the CO, where single polarization homodyne coherent detection is implemented.

## II. Up-Link From the ONU to the CO

The overall architecture of the uplink transmission, from a user ONU to the CO, is reminded in Fig. 1. The Si-PIC operation was previously described in [4], highlighting the Faraday Rotator Mirror (FRM) effect it enables.

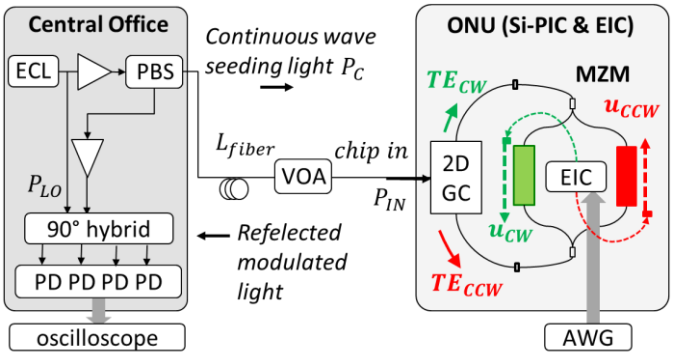


Fig. 1 - Up-link transmission and ONU Si-PIC.

The continuous wave seeding light of an External Cavity Laser (ECL) with output power $P_c$ is sent to the Si-PIC at the ONU. The Si-PIC comprises a 2D-surface Grating Coupler (2D-GC) which splits the light into two Transverse Electric (TE) waveguide modes, $TE_{CW}$ and $TE_{CCW}$, propagating, respectively Clock Wise (CW) and Counter Clock Wise (CCW) towards the Si-MZM. As the input state of polarization is unknown the splitting ratio is also random. The electrical signal $u(t)$ (defined below) is applied on the phase modulation sections of each arm of the Si-MZM, in opposite directions, $u_{CW}(t)$ and $u_{CCW}(t)$, co-propagating in the same direction respectively as $TE_{CW}$ and $TE_{CCW}$, and modulating them.

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Afterwards $TE_{CW}$ and $TE_{CCW}$ recombine in the 2D-GC, the splitting of the input signal is thus reversed. The recombined signal is transmitted back to the CO, carrying the upstream data of the user. If the two MZM arms have a π phase difference, the reflected modulated light has a polarization orthogonal to that of the seeding light when arriving at the CO [4] , independently of the state of polarization at the input of the device. The resulting homodyne detection signal is shown to be proportional to:

$$\sqrt{P_c}.Loss_{Fiber}.\sqrt{Loss_{R-MZM}}.\varepsilon_{co} \times \left[1 - \frac{\varepsilon_{counter}}{\varepsilon_{co}}\right].u(t) \quad (1)$$

where $\varepsilon_{co}$ (respectively $\varepsilon_{counter} \ll \varepsilon_{co}$) are the phase-modulation efficiencies in case of a modulating wave $u(t)$ co-propagating with the optical wave (respectively counter-propagating), $Loss_{Fiber}$ and $Loss_{R-MZM}$ are respectively the losses of the fiber from the CO to the ONU, and the round trip losses through the Si-R-MZM. Although this is beyond the scope of this paper, it is worth noting that the coherent receiver could also be fabricated using Silicon Photonics technology [5] [6].

The electrical signal applied to the R-MZM arms ($u(t) = \cos[2\pi f_{RF}t].S(t)$) is an individual 16-QAM-modulated subcarrier whose frequency $f_{RF}$ (allocated to one user-ONU) and bandwidth, $B_{RF}$, are reminded in Table 1 [1]. In [1], a 32 Gbps upstream capacity was demonstrated, with 32 users being allocated each a different subcarrier frequency $f_{RF}$ comprised in the [1-12] GHz frequency range. Each user having a 330MHz $B_{RF}$ bandwidth, was able to transmit 16-QAM signals at a Baud rate of 300MBaud over a 31dB loss ODN.

| $f_{RF}$, & $B_{RF}$ | Up Stream capacity (FDMA) |
|---|---|
| 32 users with<br>$1 < f_{RF} < 12$GHz<br>$B_{RF} = 330$MHz | 32 users x 1Gb/s/user<br>Per user : 16QAM x 300MBaud<br>x 0.8 (FEC overhead) |

Table 1 - Modulating signal features at one user ONU.

The signal $u(t)$ can be generated directly by a very high speed DAC (≈25 GS/s) or, as indicated by Fig. 2, by a lower speed dual output DAC (≈1 GS/s) followed by individual RF up-conversion stages (IQ mixers and Local Oscillators). While the first solution is useful in prototype experiments, the second solution is much more appropriate for a real application in a low-cost ONU scenario.

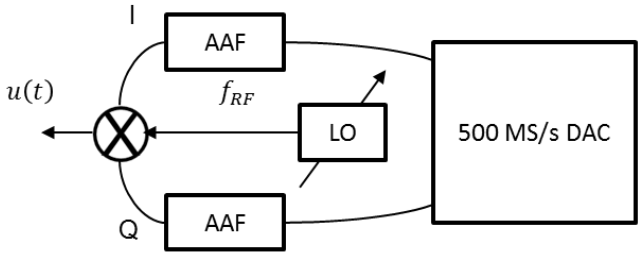


Fig. 2 - $u(t)$ Signal generation at the ONU. AAF = Anti-Aliasing Filter.

## III. Si-PIC and EIC driver Design and Performances

A first version of the PIC which does not integrate an SOA was designed and fabricated (Fig. 3-left). This version is intended to verify the R-MZM and its driver operation, as well as its implementation in the upstream coherent transmission, as described in Section 1. This version will not allow to reach the targeted power budget of the ODN. A second version integrating a heterogeneous III-V/ Silicon SOA (Fig. 3) is being fabricated according to the fabrication process reported in [7]. With 10dB gain per SOA, an additional power budget of 20dB is expected for this second version.

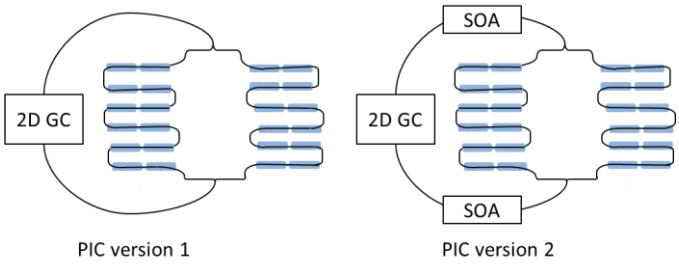


Fig. 3 – Schematics of Version 1 and Version 2 of the Silicon PIC, respectively without and with III-V/Silicon heterogeneously integrated SOA.

A segmented MZM structure (which top view is given in Fig. 4) is chosen to overcome the trade-offs of traditional travelling wave electrodes modulators [8][9]. Each arm is segmented into 12 phase modulation sections with length of 500µm each. Considering one single section, no propagation effects have to be taken into account and a simple lumped circuit model can be used. Besides, the required voltage levels along the whole modulator-arm-electrodes can be guaranteed without suffering from the propagation attenuation featured by integrated transmission lines. The circuit is designed so that the EIC driver is flip-chipped on top of the Si-PIC, reducing the path between the output stages of the driver and the modulation sections.

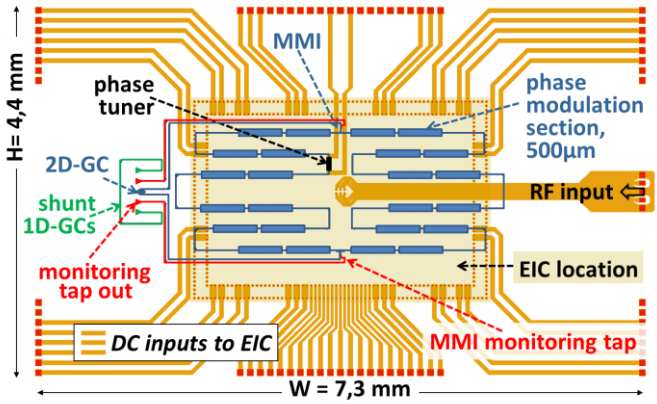


Fig. 4 - Top view of the Si PIC.

The Si-PIC was fabricated at CEA-Leti. The waveguides are etched in a 220nm-thick silicon layer, on top of a 2µm-thick buried oxide (BOX). A rib structure is used with a 100nm-thick slab for both passive components of the PIC (MMI, 2D-GC) and the phase modulation sections of the modulator. The latter are made from PN doped waveguides. A 50µm-long phase tuner is arranged in one arm of the R-MZM, consisting of a passive waveguide section heated up by flowing a current in a TiTiN layer placed on top of the waveguide. It purpose is to precisely set a π phase difference between the two arms of the R-MZM. Fig. 5 gives the cross section of the phase modulation and phase tuning sections.

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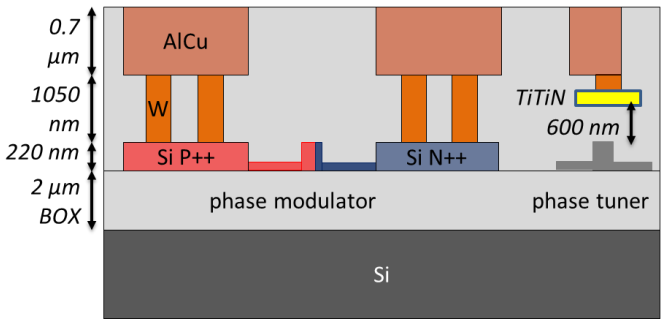


Fig. 5 – Cross section of the phase modulation and phase tuning sections.

The components integrated in the R-MZM were characterized separately. Their performances are reported in *Table 2*. The 2D-GC exhibits -7dB Insertion Loss ($IL_{2D-GC}$). The 33.5µm-long MMI has Insertion Losses ($IL_{MMI}$) of ~0.25dB. It is centered at 1550nm and has a -1dB BW greater than 100nm. The Figures of Merit of the phase modulation sections, $V_\pi.L_\pi$, propagation loss, $PL$, and E/O bandwidth, BW, are measured to be respectively 4V.cm, 1dB/mm and 20GHz when biased at -1V. The round trip losses through the Si-R-MZM are then written as follows:

$$Loss_{R-MZM} = 2.[IL_{2D-GC} + IL_{MMI}] + L_{el}.PL \quad (2)$$

where $L_{el}$ is the sum of the active distributed Phase Modulation sections.

| $IL_{2D-GC}$ | $IL_{MMI}$ | Phase modulation section, 500µm-Long (PN doped Si-waveguide) | | |
|---|---|---|---|---|
| -7 dB | -0.25 dB | $V_\pi.L_\pi$ @-1V = 4V.cm | $PL$ = 1dB/mm | BW @-1V >20 GHz |

Table 2 - Performances of the elementary devices of the Si-PIC. '$IL_{2D-GC}$' stands for 'Insertion Loss of the 2D-GC', '$IL_{MMI}$' stands for 'Insertion Loss of the MMI', '$PL$' stands for 'Propagation Loss of the phase modulation sections'.

For the R-MZM reported here, only 6 out of 12 modulation sections were made active (i.e. $L_{el}$=3mm). The reason for having limited the number of active doped sections was to limit the R-MZM losses. At the same time, this limits the signal strength. These trade-offs are further discussed below. The R-MZM round trip losses are therefore estimated to be $Loss_{R-MZM}$~17.5dB.

The measured efficiency of the phase tuner is ~0.056.π/mW (~18mW are required for a π phase shift).

From Equation (1), simulations can be driven in order to assess the trade-offs of the device [10][11]. Maximizing the demodulated signal reflected back from the R-MZM requires to null the counter modulation efficiency $\varepsilon_{counter}$. For that purpose, cumulating more phase modulation sections makes counter propagating RF and optical waves having bigger delay mismatches, and therefore reduces down the counter modulation efficiency $\varepsilon_{counter}$. In addition with reducing down counter-propagation efficiency, this provides higher phase modulation. On the other hand, as more phase modulation sections are cumulated, the insertion loss of the MZM increases. Assuming a 1.6Vpp modulating voltage provided by the CMOS driver, one can quantify these trade-offs. Fig. 6 plots the R-MZM contribution to the homodyne detection signal level '$\sqrt{Loss_{R-MZM}}.\varepsilon_{co} \times \left[1 - \frac{\varepsilon_{counter}}{\varepsilon_{co}}\right]$' against frequency, for two lengths $L_{el}$ (3mm and 6mm) of phase modulation sections and two types of such sections (with different $PL$ and $V_\pi.L_\pi$). $\varepsilon_{counter}$ is evaluated by computing the phase mismatch between the optical and RF waves along the MZM arm length [10][11]. As described in [11], at low RF frequencies ($f_{RF}$<2GHz), the counter-propagating modulation efficiency stays high and equal to the co-propagating efficiency ($\varepsilon_{counter}$~$\varepsilon_{co}$). This is because the RF wavelength is several 10 times longer than $L_{el}$).

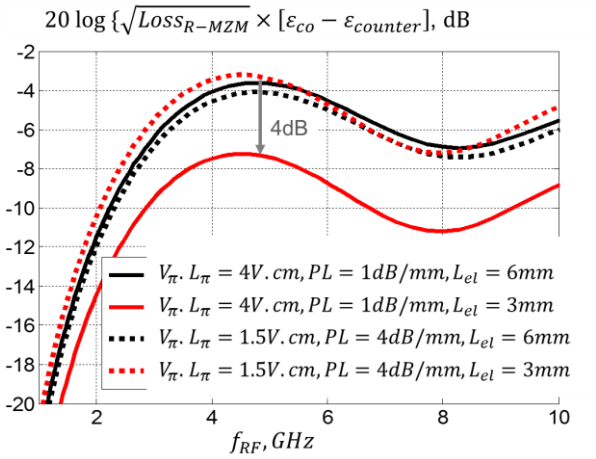


Fig. 6. Contribution of the R-MZM to the homodyne detection signal.

This shows that with the phase modulation sections used in this experiment ($V_\pi.L_\pi$ = 4V.cm and $PL$ = 1dB/mm) a longer active section would have performed better (4dB gain improvement with $L_{el}$= 6mm versus 3mm). On the contrary, with a phase modulation section with $V_\pi.L_\pi$ = 1.5V.cm and $PL$ = 4dB/mm, active section with length $L_{el}$= 3mm would behave equal or better than active section with length $L_{el}$= 6mm versus 3mm).

The EIC was fabricated on STMicroelectronics 65nm CMOS technology. On each MZM arm, 12 differential driving stages are used, based on Current Mode Logic differential pairs with inductive peaking. The driving stages for each pair of adjacent 500µm-phase-modulation-sections can be independently switched ON/ OFF. The delay matching between the optical and electrical waves is ensured by making use of active delay matching between 1mm-long MZM sections, and of passive delay matching within each pair of 500µm-modulation-sections. The active delay chain has been designed as a cascade of 6 active delay elements, each featuring a programmable delay (set to 24.5ps). The nominal differential signal at the input of the active delay chain at $f_{RF}$=3GHz is 340mVpp. Each driving stage is designed to generate at the output a 1.6Vpp differential signal which is AC coupled to the phase-modulation-section-electrodes using an integrated MIM capacitor, and achieving a low frequency pole at 3MHz. In order to verify the standalone electrical performance of the driver, a dedicated IC version was fabricated for electrical probe testing. A lower gain is expected for this test version due to the 100Ω differential load added at the output of each driving stage, in parallel with an integrated capacitance that mimics the load of each modulator stage.

The measured small signal transfer function is shown in Fig. 7, comparing with simulations. Good agreement is demonstrated. The small signal bandwidth is in line with target: 8GHz at the

output of driving stage #1, 10.3GHz at the output of driving stage #12.

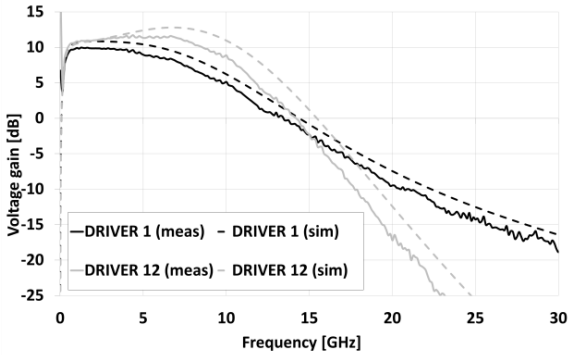


Fig. 7 – Measured small signal transfer function of the EIC driver elements

The measured large signal transfer function at an input signal of 340mVpp is compared with simulations in Fig. 8. Less than 0.2dB gain mismatch per driver stage is observed. The Total Harmonic Distortion is measured to be better than -15dB.

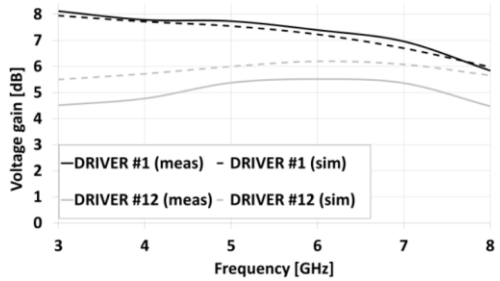


Fig. 8. Large signal transfer function of the EIC driver elements

In the measurements reported below, only the first 6 stages of the driver are switched ON. For the E/O chip, the achievable modulation voltage is expected to be $Vmod$=±0.8V, corresponding to a modulation depth of ± 0.06.Vπ.

## IV. Packaging of the Silicon ONU

The EIC driver was flip-chip mounted on the Si-PIC using 20µm diameter (40µm pitch) copper pillars which were deposited on the EIC wafer [12][13]. These copper pillars were capped with a SnAgCu eutectic solder layer. The corresponding bond pads on the Si-PIC consisted of Al with a Ti/Ni/Au Under Bump Metallization (UBM). Solder reflow was used as the flip-chip bonding method. With this approach, both the chip-alignment and solder-joints were much improved over the results from the thermo-compression bonding. Moreover, this solder reflow is more attractive than thermo-compression as the standard flip-chip bonding process for the mass reflow in industry, due to cost-effectiveness. The quality of the flip-chip bond was checked using cross-sectional grinding and die peeling-off tests, along with electrical tests. All individual copper/solder pillar bumps were found to be well connected.
Fig. 9 shows a cross section and top view of the EIC/PIC stacking.

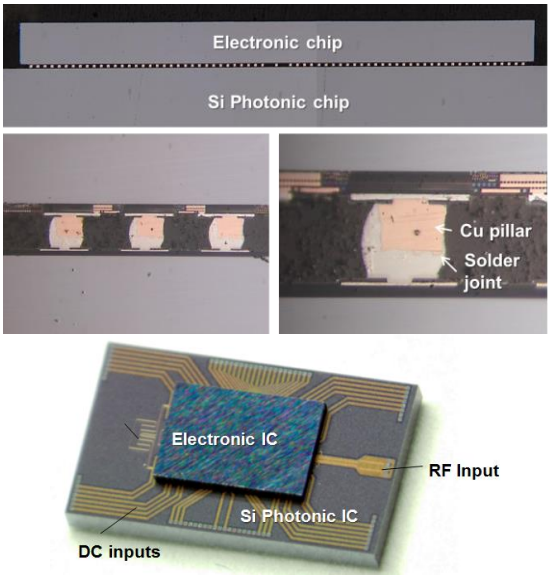


Fig. 9. Cross-section of the flip-chip bonded EIC and PIC, showing the Cu-Solder pillars between the two chips. Microscope images of the Cu-Solder pillars after cross-sectional grinding.

Using the software modelling tool SolidWorks, a complete virtual mock-up of the full-module was designed, including the flip-chip bonded EIC/PIC, heat-spreader, Peltier-cooler, Al base-plate, PCB, and fibre-array. The test PCBs were designed and fabricated, consisting of three layers with a Rogers-4350B interposer for wire-bonding to the PIC, and containing MSMP-connectors for the RF signals, with surface-mounted electrical components to handle the DC signals. The EIC/PIC assembly is attached to the PCB using Au wire-bonding (Fig. 10 top-left), together with the Al heat-spreader and a Thermo Electric Cooler (TEC). An 8-channel fibre-array was aligned and bonded to the grating-couplers on the Si-PIC (Fig. 10 top-right). Fibre-to-PIC alignment is achieved using active optical feedback through 1D shunt GCs (Fig. 4). The fibre-to-fibre transmission was -11dB, indicating a coupling insertion loss of -5.5dB for each 1D-GC.

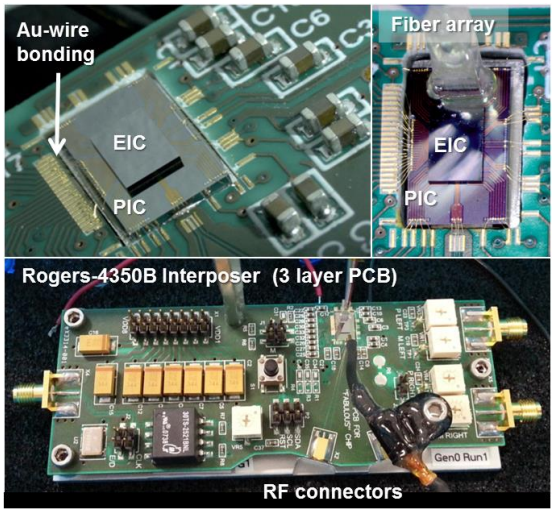


Fig. 10 – Overview of the EIC/PIC packaged mockup.

In order to design a thermally optimized package structure, a good working knowledge of the thermal characteristics of the EIC/PIC stacking is important, not only because the stability of filters and SOAs of the Si-PIC are strongly temperature sensitive, but also because it helps determine the appropriate thermal-management solution, which contributes to the overall power consumption- of the device. With this motivation, the temperature increase of the EIC and Si-PIC were measured with the EIC drivers fully switched ON (1.5 Watt-input power). Without TEC control, the temperature increase of the EIC and Si-PIC were +24°C and +17°C respectively. Although the PIC temperature can be stabilized to 20°C±0.01°C using the TEC, no active cooling was implemented for the reported transmission experiments.

## V. Transmission Experiments

Referring to Fig. 1, an Arbitrary Waveform Generator (AWG) with 340mVpp-output voltage feeds the input of the EIC driver for generating the modulating signal $u(t)$ (with QPSK or 16QAM). A high speed oscilloscope is used after the Photo Detector (PD) array to compute the Error Vector Magnitude (EVM) of the transmitted signal. While the phase difference between the two MZM arms is biased and locked at π and $B_{RF}$ is set to 500 MHz, several measurements are performed.

Fig. 11 reports the measured EVM as a function of the frequency $f_{RF}$ (which is allocated to the ONU) as the light polarization is randomly rotated over 100 states on the way to the ONU in order to demonstrate the insensitivity to input polarizations. The optical power $P_c$ of the seeding light is set to +11.5dBm and the VOA loss is set such that the optical input power, $P_{IN}$, feeding the R-MZM equals +7.5dBm. The low dispersion of the EVM confirms the polarization insensitivity of the device thanks to the FRM effect. The EVM is kept below -15.9dB (respectively -9.1dB) over a frequency range of [2-4] GHz (respectively [1-7] GHz) which is below the maximum EVM required for achieving a $2.10^{-3}$-BER with 16-QAM modulation (respectively QPSK) [14]. This represents a ~2Gbps (respectively 1Gbps) bit rate per user.

Fig. 12 reports the measured EVM as a function of $P_{IN}$ when $f_{RF}$ is set to 3GHz. $P_c$ is set to +11.5dBm and measurements are made by tuning the VOA losses and using 0 and 10km-fiber-length, $L_{Fiber}$. A minimum power $P_{IN}$ of ~6.5dBm (respectively 2.5dBm) is required for achieving a 16-QAM transmission (respectively QPSK), leading to an available loss budget, $(P_C - P_{IN})$, of 5dB (respectively 9dB). No fiber transmission penalty is observed.

In order to increase the available power budget for the ODN, we increased the optical power $P_C$ of the seeding light, from 11.5dBm to 15.5 dBm. Fig. 13 reports the measured EVM as a function of $P_{IN}$ when $f_{RF}$ is set to 3GHz. Measurements are made by tuning the VOA losses and using 0 km-fiber-length. A noise degradation is clearly brought by the increased EDFA noise at the CO. Besides we suspect that increasing Pc leads to increased Brillouin back scattering, even though over very small fiber length.

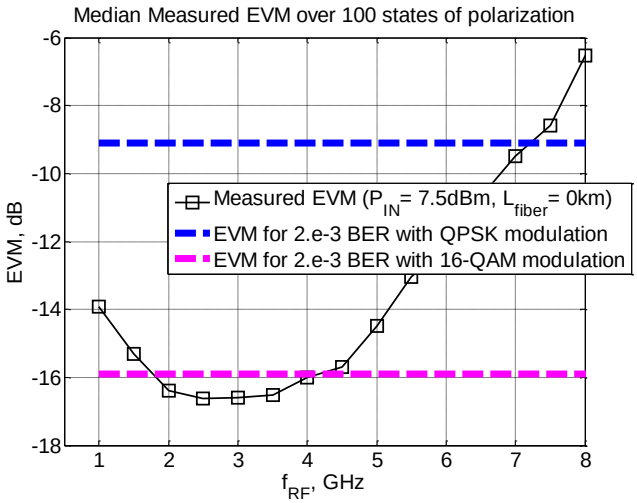


Fig. 11 - Median measured EVM against user frequency $f_{RF}$ over 100 states of polarization, $L_{Fiber}$=0km, $P_C$=11.5dBm, $P_{IN}$=7.5dBm.

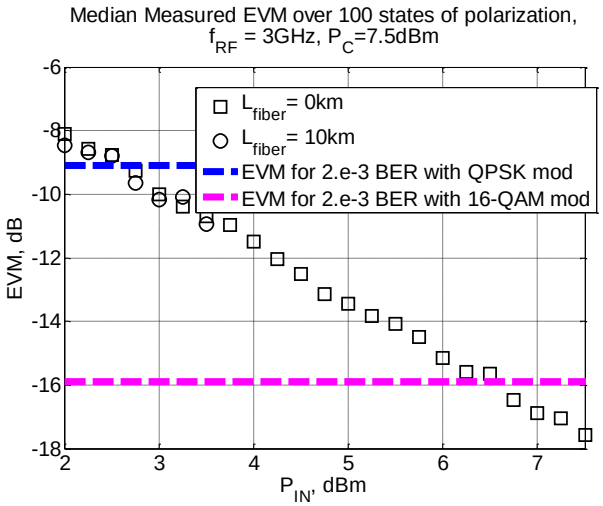


Fig. 12 – Median measured EVM against R-MZM input power $P_{IN}$, $f_{RF}$=3GHz, $L_{Fiber}$= 0km and 10km, $P_C$=11.5dBm.

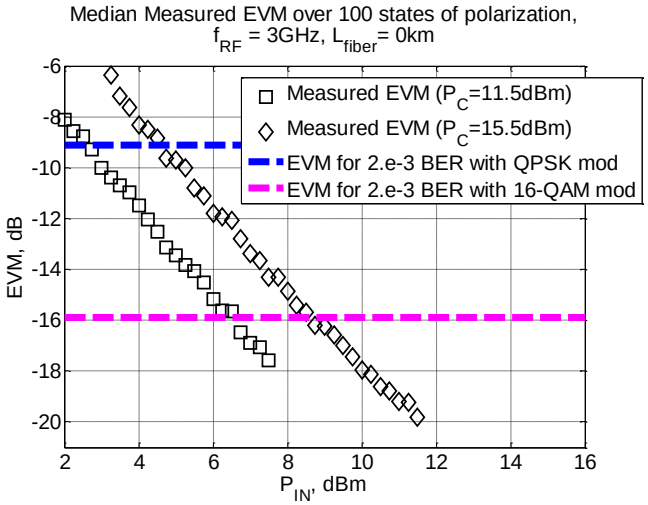


Fig. 13 - Median measured EVM over 100 states of polarization against $P_{IN}$, $L_{Fiber}$=0.

Fig. 14 displays some acquired QPSK and 16-QAM constellations with 12% EVM.

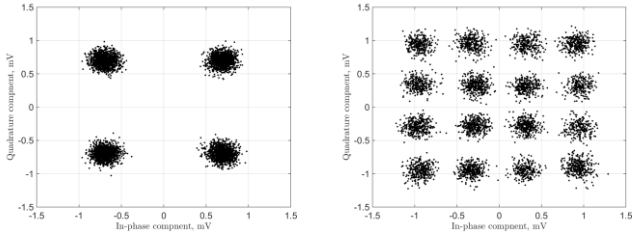


Fig. 14 - QPSK&16 QAM constellations, EVM~12%, $f_{RF}$=3GHz, $L_{Fiber}$=0, $P_{IN}$=7.5dBm, $P_C$=11.5dBm.

## VI. Discussion And Conclusion

We demonstrated a novel reflective transmitter targeting implementation in Passive Optical Networks (PON) with Frequency Division Multiplexed Access (FDMA). It is made up of a Silicon Photonic Integrated Circuit (Si-PIC) comprising a Reflective Mach Zehnder Modulator (R-MZM) and its flip chipped CMOS Electronic Integrated Circuit (EIC) driver. Transmissions are successfully demonstrated using 500MBaud QPSK and 16-QAM modulated subcarriers, achieving Bit Error Rate (BER) below $2.10^{-3}$. For QPSK-modulated subcarriers (respectively 16-QAM), the available access frequency bandwidth is measured to be [1-7GHz] (respectively [2-4GHz]) with an available loss budget of 9dB (respectively 5dB).

A second version of the PIC is being fabricated (Fig. 3-right), integrating two heterogeneous III-V/Si SOAs with >10dB gain [7]. Also by reducing the losses of the 2D-GC (achievable loss of 3.5dB [16] as compared with 7dB), an improved loss budget of 27dB is expected, as detailed in Table *3*. In addition an improved driver bandwidth from 8 to 12GHz will enable full compliancy with the work demonstrated in [1] and making use of off-the-shelf non-integrated fiber pigtailed devices (PBS, $LiNbO_3$ modulator, and SOA).

| PIC versions | |
|---|---|
| First version (this work): measured performances | Second version (future work): expected improvement in performances |
| Round trip -2D-GC loss:<br>-14dB (-2 x 7dB)<br><br><br>= -14 dB | Round trip -2D-GC loss reduction:<br>-7dB (- 2 x 3.5dB)<br>Addition of SOA gain:<br>+20dB (+2 x 10dB)<br>= +13 dB |
| Current Available power budget (demonstrated here)<br>= + 5dB (16-QAM) | Expected Improved power budget<br>= +5dB +27dB (16-QAM) |

*Table 3 – PIC versions: Version 1 (this work): measured performances, Version 2(future work): expected performances comparison*

## VII. Acknowledgment

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## References

[1] S. Straullu, P. Savio, J. Chang, V. Ferrero, A. Nespola, R. Gaudino, S. Abrate, "Optimization of Reflective FDMA-PON Architecture to Achieve 32 Gb/s Per Upstream Wavelength Over 31 dB ODN Loss," J. Lightwave Technol., vol. 33, no.2, pp. 474-480, Jan. 2015

[2] S. Straullu, A. Nespola, P. Savio, J. Chang, V. Ferrero, A. Lebreton, J. Le Masson, R. Dong, P. Chanclou, B. Charbonnier, S. Abrate, R. Gaudino, "System aspects of the FDMA PON conceived within the FABULOUS European project," in Proc. of International Conference on Transparent Optical Networks, ICTON'2014, Graz, Austria. pp. 1-4, Jul 2014

[3] B. Charbonnier, S. Menezo, P. O'Brien, A. Lebreton, J.M. Fedeli, B. Ben Bakir, "Si-Photonics for Next Generation FDM/FDMA PON," IEEE/OSA JOCN, vol. 4, no. 9, pp. A29-A37, Sept. 2012

[4] S. Menezo, B. Charbonnier, G.B. de Farias, D. Thomson, P. Grosse, A. Myko, J.M. Fedeli, B. Ben Bakir, G.T. Reed, A. Lebreton, "Reflective silicon Mach Zehnder modulator with Faraday rotator mirror effect for self-coherent transmission," in Proc. of OFC'2013, paper JTh2A, Anaheim, March 2013

[5] M. Sakib, M. Hai, and O. Liboiron-Ladouceur, "A Silicon Photonic Integrated Packaged Coherent Receiver Front-End For Soft-Decision Decoding," J. Lightwave Technol., vol. 32, no. 24, pp. 4151-4156, Dec. 2014

[6] C. R. Doerr, L. L. Buhl, Y. Baeyens, R. Aroca, S. Chandrasekhar, X. Liu, L. Chen, and Y.-K. Chen, "Packaged monolithic silicon 112-Gb/s coherent receiver," IEEE Photonics Technol. Lett., vol. 23, no. 12, pp. 762–764, June 2011

[7] P. Kaspar, e.a., "Packaged hybrid III-V/silicon SOA", in Proc. of ECOC'2014, Tu.1.1.6, Cannes, 2014

[8] M. Cignoli, G. Minoia, M. Repossi, D. Baldi, A. Ghilioni, E. Temporiti, F. Svelto, "A 1310nm 3D-integrated silicon photonics Mach-Zehnder-based transmitter with 275mW multistage CMOS driver achieving 6dB extinction ratio at 25Gb/s," in Solid- State Circuits Conference - (ISSCC), 2015 IEEE International, paper 22.9, pp.416-418, Feb. 2015

[9] W. Xiaotie, B. Dama, P. Gothoskar, P. Metz, K. Shastri, S. Sunder, J. Van der Spiegel, W. Yifan, M. Webster, W. Wilson, "A 20Gb/s NRZ/PAM-4 1V transmitter in 40nm CMOS driving a Si-photonic modulator in 0.13µm CMOS," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International , paper 7.7, pp.128-129, Feb. 2013

[10] R. Spickermann, S.R. Sakamoto, N. Dagli, "In traveling wave modulators which velocity to match?," in Proc. LEOS'1996, vol. 2, paper WM3, pp 97-98, 1996

[11] A. Lebreton, B. Charbonnier, G.B. de Farias, P. Chanclou, R. Dong, J. Le Masson, S. Menezo, "Low Complexity FDM/FDMA Approach for Future PON," in Proc. OFC'2013, paper OTh3A.7, Anaheim, March 2013

[12] S. Saeedi, S. Menezo, G. Pares, A. Emami, "A 25Gb/s 3D-Integrated CMOS/Silicon-Photonic Receiver for Low-Power High-Sensitivity Optical Communication," J. Lightwave Technol., vol. PP, no. 99, pp. 1-9, oct. 2015

[13] N. Pavarelli, L. Jun Su, M. Rensing, C. Eason, P.A. O'Brien, "Optical and Electronic Packaging Process for Silicon Photonic Systems," J. Lightwave Technol., vol. 33, no. 5, pp. 991 – 997, March 2015

[14] R.A. Shafik, M.S. Rahman, A.R. Islam, "On the Extended Relationships among EVM, BER and SNR as Performance Metrics," in Electrical and Computer Engineering, 2006. ICECE '06. International Conference on, pp.408-411, Dec. 2006

[15] F. Boeuf, S. Cremer, E. Temporiti, M. Fere, M. Shaw, C. Baudot, N. Vulliet, T. Pinguet, A. Mekis, G. Masini, H. Petiton, P. Le Maitre, M. Traldi, L. Maggi, "Silicon Photonics R&D and Manufacturing on 300mm Wafer Platform", J. Lightwave Technol., vol. PP, no. 99, pp. 1-11, Sept 2015

[16] L. Vivien, A. Polzer, D. Marris-Morini, J. Osmond, J.M. Hartmann, P. Crozat, E. Cassan, C. Kopp, H. Zimmermann, J.M. Fédéli, "Zero-bias 40Gbit/s germanium waveguide photodetector on silicon", Optics Express, vol. 20, no. 2, January 2012

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