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Understanding CMOS Technology through TAMTAMS Web

Fabrizio Riente, Izhar Hussain, Massimo Ruoch and Marco Vacca

Abstract—In the last decades CMOS technology has undergone an extraordinary evolution. Thanks to the continuous scaling process, CMOS transistors are now so small that millions can be easily fitted in a single chip. Shrinking transistor sizes has complex consequences on the performance of both the transistor itself and the system that is based upon it. Understanding and teaching the CMOS scaling process and its consequences on circuits is an increasingly difficult task. Furthermore the scaling process is reaching an end, due to the continuously growing fabrication costs and the unavoidable physical limits on the smallest size achievable. As a consequence many emerging technologies, like carbon nanotubes and nanowires, are being studied as possible CMOS substitutes. Describing and teaching these new technologies, alongside the scaled transistor itself, adopting a complete and well organized approach is a process that presents further difficulties.

To solve these problems we have started in the past years the development of TAMTAMS, a tool conceived to analyze CMOS circuits, from device to system level. The tool is based on models derived from the literature or, in some cases, internally developed and verified. It allows to analyze the main characteristics of a CMOS transistor, like currents, threshold voltage or mobility, considering different technology nodes and parameters, and to understand how they influence circuits performance. The tool structure is open and modular, allowing therefore easy integration of further CMOS technologies and to compare them. In this paper we present a total overview of the original tool, TAMTAMS Web. While the general concept behind the tool is still the same, the tool was completely rewritten around a web interface. TAMTAMS Web is freely accessible to students and to any one interested in CMOS technology. As a future development several post-CMOS technologies will be added to TAMTAMS Web, allowing therefore a comparison with state of the art CMOS. TAMTAMS Web is actively used in the Integrated System Technologies (IST) held at Politecnico di Torino. It defines a new way of learning, because students learn and understand modern electronic technology both using TAMTAMS Web as an instrument, and being part of the development process, as part of the IST course.

Index Terms—Scaling Process, Emerging Technologies, Web-based Services, Education

1 INTRODUCTION

THE foundation of the “Digital Age”, the period of history in which we live, lies deeply in the MOS-FET (metal-oxide-semiconductor field effect transistor) technology. The continuous scaling of transistors size, from few tenth of microns to few tenth of nanometers, has allowed the development of all kind of electronics devices. Nowadays commercial devices based on the 14nm node are available. This is an incredible achievement, but to obtain this goal the technology behind it has greatly increased in complexity. The scaling process involves no more just a scaling in transistors size, but many subtle solutions must be adopted to obtain a working device. Every small change to the fabrication process has however deep consequences on the device itself and on the system built upon it. Furthermore, the scaling process is reaching an end. There is clearly a fundamental physical limit to the minimum size achievable [1]. Not to mention fabrication costs that are rising exponentially. The main consequences is that many new devices are studied as possible substitute for CMOS transistors. From Graphene transistors to Silicon Nanowires

[2] [3] and Carbon Nanotube structures [4], to radically different technologies like NanoMagnet Logic [5] [6] and Molecular QCA [7], an incredible number of new devices are being studied and developed. As a consequence, the complexity of the micro and nanoelectronics galaxy further increases.

While the scaling process and its consequences are well known and easy to understand for people working in this field, they remain a very complex subject for all others. This is true also in case of people with a strong technical background, like engineering students. Different approaches can be used in studying the scaling process. However, the above mentioned complexity of the scaling process and its consequences, coupled with the huge number of emerging devices, lead to a very steep learning curve and increasing difficulties in the teaching activity. To enhance the learning experience the instruments available in the “Digital Age” can be successfully employed. Software tools are available to analyze transistors performance considering the scaling process. The most prominent exponent of this family of tool is MASTAR [8], a tool used by the International Roadmap for Semiconductors to evaluate and forecast transistors performances. MASTAR limits its analysis mostly to device level. To analyze the behavior at system level, i.e. logic gates and complex circuits, BACPAC [9] and more extensively GTX [10] can be used. The evaluation

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of circuits performance at system level is however more complex than the analysis at device level. Different circuits architectures have different needs. For example in large diffusion applications [11] [12], the most important issue is the speed [13]. In data processing architectures like in GPUs or NoC [14] [15] or microprocessors [16] [17] power consumption is more important in most of the cases. For emerging technologies a possibility is represented by NANO HUB [18], which is a web based resource where a set of tools and documents can be freely used to enhance the learning experience. While MASTAR and BACPAC are focused on MOSFET technology, NANO HUB considers also emerging technologies.

Both these tools are very useful but they lack focus. What we believe it is necessary to successfully teach micro and nanoelectronics, is an instrument to analyze electronics devices, from device level to system level also considering emerging technologies, in an well structured and systematic way. For this purpose we started the development of TAMTAMS (Torino Assessment of Mos Technology and Advanced perfoRmance of System calculator) to reach exactly this goal [19]. TAMTAMS was originally developed as a small tool written and developed in OCTAVE, a free Software similar to Matlab. The idea behind TAMTAMS was to merge the device level analysis of MASTAR of device performance considering technology scaling, with the system level analysis of BACPAC. Not only we successfully reached this goal with TAMTAMS, but we went beyond providing additional functionalities. First, TAMTAMS is based on an open structure, different models and technologies can be added and analyzed. Second, TAMTAMS will allow in the future the seamless integration of new emerging technologies, opening up new interesting possibilities, like a direct comparison between scaled MOSFET transistors and emerging devices [20].

However, TAMTAMS is a different tool with respect to SPICE simulators. TAMTAMS, like Mastar and Bacpac, are performance estimators, while SPICE is a low level simulator of electric circuits. In SPICE an equivalent electric circuit of the device is designed and the whole device behavior is then simulated using electric equations. In TAMTAMS or Mastar, models for specific quantities, like threshold voltage, are implemented and calculated. For example, in SPICE it is possible to automatically obtain the complete I-V curve of a transistor, while in Mastar or TAMTAMS the goal is generally to calculate the transistor current in specific parts of the I-V curve, like the saturation value. However, due to the flexibility of TAMTAMS, it is possible to implement a module that evaluates the I-V curve. As a consequence TAMTAMS and SPICE allow to get similar results if necessary, but they are designed with different goals. Another difference is that in SPICE it is impossible to analyze very large circuits due to the high computational power required. In TAMTAMS, given that it is an estimator and not a simulator, it is possible to analyze high complexity circuits. Another comparison can be done regarding the accuracy of this two

instruments. SPICE can generate very accurate results, but only if a sufficiently detailed model of the device is provided. At the same time the accuracy of TAMTAMS depends on the accuracy of the model and parameters used. Most of the models of TAMTAMS are taken from literature, where their accuracy is generally verified against physical simulators or experimental measurements. As a consequence the accuracy of TAMTAMS can be higher or lower than the accuracy of SPICE, depending on the accuracy of models used in both tools.

To be effective as a teaching instrument, it is not sufficient for a tool to simply provide a good and reliable analysis, it must also exploit the potential of the "Digital Age". To reach this result we conceived the new version of TAMTAMS from scratch around a web interface, creating therefore TAMTAMS WEB. The tool is available at the following link, <http://tamtams.vlsilab.polito.it>. After a simple registration it can be used by anyone interested in CMOS technology. For now TAMTAMS WEB includes only CMOS technology, considering state of the art BULK and SOI devices. FinFet technology is starting to be exploited at commercial level, so we plan to add it to TAMTAMS as soon as possible completing the CMOS analysis. Then post-CMOS technologies will be added, as TAMTAMS WEB is conceived as an always evolving tool. which is indeed already used by students of the master level course INTEGRATED SYSTEMS TECHNOLOGY (IST) for the Electronics Engineering Master degree held at Politecnico di Torino. In this work we present TAMTAMS WEB, describing its general structure and the basic ideas behind it in Section 2. In Section 3 we describe with greater detail the three main types of analysis that are possible in TAMTAMS WEB. Finally, in Section 4, we present a throughout case of study of three representative analysis. These analyses are performed taking the role of a student that wants to understand CMOS technology. As a whole TAMTAMS WEB provides an experience, in case of MOSFET and emerging technologies study, that cannot be find in any other tool in this field.

2 TAMTAMS WEB: STRUCTURE AND INTERFACE

In micro and nanoelectronics systems, three main entities can be identified. The first one is the transistor, that represents the DEVICE level. The second one is represented by the logic gates based on transistors. The circuits and systems organized using specific connections of logic gates represent instead the top level entity, the SYSTEM level. How these levels are related, how much and in which measure a variation at the technological level influences device and logic and system level features is not straightforward to be identified. For example, it is well known that the strength of MOSFET technology lies in the scaling process. It should be easy to understand that making transistors smaller directly affects device parameters. For example the transistors threshold voltage nor-

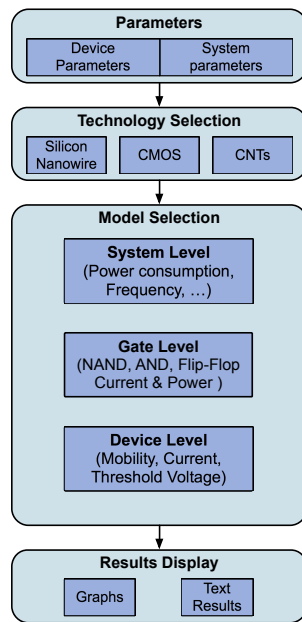


Fig. 1. TamTams structure. Two kind of parameters are used in the analysis, system parameters (like the total number of transistors) and device parameters (like transistor gate length and gate oxide thickness). Device parameters depends on a specific technology, while system parameters are independent. The tool core part is represented by the three analysis types, device, logic gates and interconnections and system level. Results can be viewed both in graphical form, with run-time generated graphs, or in text form.

mally decreases and the drive current increases reducing transistor sizes. However, this is not always true, since with some technology nodes (a nodes is identified by the transistor gate length) the opposite happens. Moreover, how the change on transistor parameters affects the performance of logic gates and complex circuits? It is a complex matter, since many interdependent parameters are involved. Finally, different mathematical models can be used to analyze a particular parameter. Every model generally provides different results. How it is possible to evaluate and compare them effectively? The structure of TAMTAMS WEB is built around the three main electronics entities, DEVICE, LOGIC GATE and SYSTEM, with the aim of solving these issues. The tool structure is summarized in Figure 1.

The analysis performed by TAMTAMS WEB are based on two sets of parameters. **System level parameters** represents a set of characteristics that a generic circuit can have. For example the total number of transistors, the percentage of logic and memory are both system parameters. Transistors scaling is identified by technology nodes. A technology node can be represented either with the transistor gate length or the year where that transistor was introduced. These parameters are technology independent and are used only in the SYSTEM

level analysis. **Device level parameters** represent instead the physical characteristics of transistors. As an example, the gate length [21], the gate oxide thickness, the level of doping and the type of dielectric used are all device level parameters. These parameters are technology dependent, so users must select a specific technology and one or more technology node. TAMTAMS WEB is now already a complete tool that allows the analysis of existing state of the art technologies, BULK and SOI, considering all three common device families, High Performance (HP), Low Operating Power (LOP) and Low Stand-by Power (LSTP). Since recently FinFet technology is starting to be exploited at commercial level, we are working toward the integration of this technology, completing the CMOS analysis. However, by its nature, TAMTAMS WEB is a tool that tries to follow the evolution of electronics, as a consequence its structure will always change and improve. We will continue to modify it, adding for example support for emerging technologies or additional modules.

The tool core part is composed by the *Module Selection*. For each level, device, logic gate and system, different figures can be analyzed. For example drive current (I_{on}) and subthreshold current (I_{off}) are among the device level figures. At logic gate level, performance of simple gates (NAND/AND, Flip-Flop) can be evaluated alongside with parasitic parameters of interconnection wires. At system level several options are available, most of them provide performance analysis in terms of power and timing of generic complex circuits and memories. For a specific *module* (i.e. a software element in the tool that identifies one or more figures specific for a device or another element under analysis) different *models* are available (i.e. the set of mathematical formula based on input parameters and model based on literature and other features calculated in other modules). In the I_{on} case for example, two models can be selected, one based on the standard equation used currently in at scholastic level and one based on the MASTAR model. This is the most important part and it uses a system of hierarchical dependencies among every module. Modules have a specific hierarchy, for example to evaluate the I_{on} current the threshold voltage must be previously evaluated. TAMTAMS WEB is based on a system that automatically keep tracks of every dependency, so, after the selection of a specific module the tool will automatically select all the other modules that are required. For each module loaded by TAMTAMS WEB a default model is selected, however the default model can be changed by the user. This is a very powerful feature, not available in both MASTAR and *Bacpac*, allows to compare different models of the same quantity derived from the literature and seeing their effects on higher hierarchical levels. As an example it is possible to evaluate the same quantity, I_{on} , using two different models of threshold voltage (V_{th}), comparing the result and understanding therefore the accuracy of each model. Results can be visualized either using a text format or using dynamically generated graphs. Figure

```

1 %% THRESHOLD VOLTAGE WITHOUT CORRECTION FACTORS
2
3 % Band Gap Narrowing model
4 a=log(Nbulk/N_zero);
5 % Energy gap variation
6 deltaEg=9*(a+(a.^2+0.5).^0.5);
7 % Intrinsic doping value
8 ni_temp=ni_zero*exp(deltaEg*1e-3*q/(2*Kb*Temp));
9
10 % Phi_f
11 Phi_f=Vt*log(Nbulk/ni_temp);
12
13 % Flat-band voltage evaluation
14 Vfb= Phi_m -(Xs + Eg/2 + Phi_f);
15
16 % Vbi
17 Vbi=Vt*log(Nbulk*Next/ni_temp^2);
18
19 % Depletion capacitance evaluation
20 Qdep=sqrt(2*es*e0*q*Nbulk*(2*Phi_f));
21
22 % Electrical oxide thickness evaluation
23 Tox_el = Tox * 3.9/esio2;
24
25 % Oxide capacitance evaluation [F/cm^2]
26 Cox=esio2*e0/(Tox_el*1e-7);
27
28 % Base value of threshold voltage calculation
29 Vth_base=Vfb+2*Phi_f+Cox;
30
31 % The correction factors calculated by relative modules (if selected)
32 % are shown when the option "Print results" is selected
33 DIBL;
34 SCE;
35 QME;
36 PDE;
37
38 % Final value of threshold voltage calculation [V]
39 Vth = Vth_base - DIBL - SCE + QME + PDE;
40
41 %% I ON MODEL WITH MASTAR EQUATIONS
42
43 % Oxide capacitance evaluation [F/cm^2]
44 Cox=esio2*e0/(Tox_el*1e-7);
45
46 % Depletion charge evaluation
47 Qdep=sqrt(2*es*e0*q*Nbulk*(2*Phi_f));
48
49 % Depletion depth calculation
50 Tdep=1e7*Qdep/(q*Nbulk);
51
52 % d
53 d=Sigma*q*Nbulk*Tdep/(2*Cox*(2*Phi_f))*1e-7;
54
55 % Electrical channel length [nm]
56 Lel = Lgate - Gamma * Xj;
57
58 % Evaluation of the value of E critic field for the electrons and
59 % holes with the approximation of saturation velocity of carriers
60 Ecrit_n=2*Kvs*vsat/mueff_n;
61 Ecrit_p=2*Kvs*vsat/mueff_p;
62
63 % Evaluation of Vdsat with approximation of high field and body
64 % linearization of the Qn charge
65 Vdsat_n=(1/(Lel*1e-7*Ecrit_n)+(1+d)/(Vdd-Vth))^(-1);
66 Vdsat_p=(1/(Lel*1e-7*Ecrit_p)+(1+d)/(Vdd-Vth))^(-1);
67
68 % Evaluation of the saturation current without the channel resistance
69 Idsat0_n=0.5*mueff_n*Cox*(Wt/Lel)*(Vdd-Vth)*Vdsat_n;
70 Idsat0_p=0.5*mueff_p*Cox*(Wt/Lel)*(Vdd-Vth)*Vdsat_p;
71
72 % Evaluation of the Ion current by adding the contribute of channel
73 % resistance
74 Ion_n=Idsat0_n/(1+(2*Rconst_n*Idsat0_n/(Vdd-Vth))-Rconst_n*Idsat0_n/
75 (Vdd-Vth+Lel*1e-7*Ecrit_n*(1+d))*1e6; %uA/um
76 Ion_p=Idsat0_p/(1+(2*Rconst_p*Idsat0_p/(Vdd-Vth))-Rconst_p*Idsat0_p/
77 (Vdd-Vth+Lel*1e-7*Ecrit_p*(1+d))*1e6; %uA/um

```

Fig. 2. Example of octave code describing two TAMTAMS modules, threshold voltage and drive current. The threshold voltage is recalled inside the drive current module, TAMTAMS will automatically load and calculate them in the correct order.

2 depicts as an example the code of two modules, the threshold voltage and the drive current. The model is described in OCTAVE [22], a mathematical program similar to MATLAB but open source. For the threshold voltage module, for example, first the threshold voltage of long channel MOS devices is evaluated, then correction factors are introduced to keep into account the effects of channel scaling. These correction factors, Drain induced Barrier Lowering (DIBL), Short Channel Effect (SCE),

Poly Depletion Effect (PDE) and Quantum Mechanical Effect (QME), are calculated on separate modules and are used or not used in the evaluation of threshold voltage depending on the choices made by the TAMTAMS user. This approach is adopted for teaching purposes, since it helps students to understand the impact of each correction factor. The threshold voltage, along several other parameters, is recalled inside the drive current module. The drive current module of Figure 2 is the Mastar model. The accuracy of the overall calculation depends on the accuracy of the models. If the accuracy of device parameters used is good the overall accuracy of the TAMTAMS calculation can be similar or higher than the results provided by SPICE simulations. Device parameters are taken from different sources, like Mastar, the ITRS Roadmap and published experimental data.

2.1 Web Interface

TAMTAMS WEB uses a web interface, while the core computation is based on OCTAVE scripts. Some screenshots of TAMTAMS WEB are depicted in Figure 3. This choice was made to couple the power of a web tool with the power and flexibility of an easy-to-use (Matlab-like) open source language and compiler (OCTAVE) to solve mathematical equations. Furthermore, using octave as a base for the core calculation allows to easily write and add new mathematical models. The structure of the web interface is adapted to the tool structure and it is developed with the aim of guiding the user through the analysis. A typical analysis is organized according to the steps described in the following (more details, complete with all screenshots can be found in Section 4).

- **Technology type selection.** The first page consists in the selection of the type of technology to use. As a matter of fact right now only MOSFET BULK technology can be selected, but we are already working to add further technology types, like MOSFET SOI and FinFet, and emerging technologies.
- **Edit system parameters.** In this web page system parameters can be changed (Figure 3.B).
- **Technology family selection.** For each technology different subfamilies can be chosen (Figure 3.C). For BULK technology three families are available, HP, LOP and LSTP. For a specific family a single technology node can be selected. An additional options allows to select all the technology nodes of a specific family. When selecting a single node, its correspondent device parameters can be changed by the user if necessary (Figure 3.A).
- **Module selection.** This is the most important part of the analysis where the user can select any of the available modules in one of the three levels, device, logic gate and system (Figure 3.D).
- **Model selection.** For the module previously selected, different mathematical models can be chosen (Figure 3.C). More models can be easily added and analyzed in parallel.

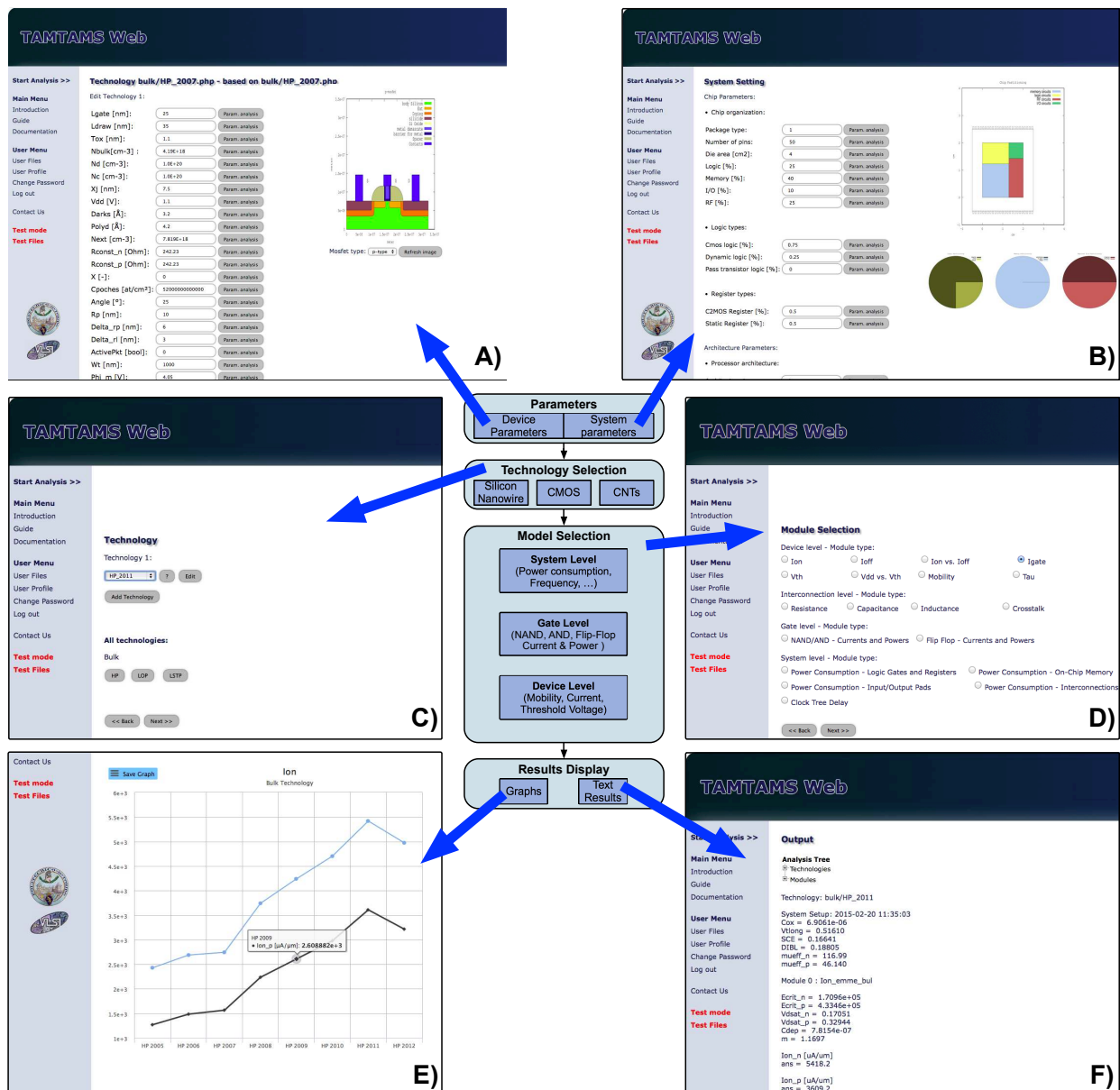


Fig. 3. TAMTAMS WEB. While the core calculation in TAMTAMS WEB are obtained using OCTAVE scripts, the tool is based on a web interface. A series of sequential web pages guides the user throughout the analysis. A) Device parameters. B) System parameters. C) Technology selection. D) Module selection. E) Graphical output result. F) Text based output.

- **Dependencies selection.** For each module selected TAMTAMS WEB automatically defines and load all the modules that are required for its calculation. Each module is assigned to a default mathematical model, but the model associated can be changed manually by the user in this web page.
- **Output mode selection.** Results can be printed on screen both as a graph (Figure 3.E) or in text form (Figure 3.F). In both cases results can be downloaded for post processing.

After completing an analysis the user can start a new one from the beginning or just go back of few pages, selecting for example a different model and seeing the new result. TAMTAMS provides **three main type of analysis**, each of them can be performed on any module of the three levels. 1) The first analysis is the technology node analysis, where a specific module (for example Ion) can be evaluated for different technology nodes. An example can be seen in Figure 3.E. 2) The second option allows to analyze a module, selecting a single technology node, but varying, in a given range, one device parameter.

3) The third option is again a parametric analysis but performed on a system parameter. This last option can be used only with system level modules.

To improve the usability of TAMTAMS WEB a small **guide** is provided to help users in their first steps. Since TAMTAMS WEB was conceived as a teaching tool, a documentation of all modules and technologies is available. The documentation provides the **source code** of modules and the value of all device parameters, and a pdf file with the **description and explanation** of the available models. Further options are possible, like the possibility to download locally the results of the analysis or the ability to enter in a *TEST* mode. Selecting this option it is possible to upload a new user created model for a specific module (for example a new model of Ion), to test it and to compare the results with TAMTAMS WEB models.

2.2 Tamtams Web in IST course

TAMTAMS WEB is actively adopted for the Integrated Systems Technology master level course at Politecnico di Torino from the Master Degree in Electronics Engineering. It enhances the teaching activity in two different ways. First, it is used by students as a tool to understand MOSFET technology and the scaling process. Students can launch their analysis and experiment how different parameters change device and system performance. This is a more efficient way of learning because students are actively involved with a learning-by-doing approach. Moreover, TAMTAMS WEB enhances in a further way the learning experience, because students actively participate in the development of new modules for TAMTAMS WEB as part of the final exam. As an homework students are asked to develop a new module or feature for TAMTAMS WEB. The fundamental idea is that the tool is developed by students for other students. This is by far the most efficient way to learn MOSFET technology, because it forces student to do a throughout literature analysis, to implement a specific model and to compare the results with the original work and to other models. As a consequence students have the possibility to go into details for the MOSFET world, and are actively involved in this process, since the homework is counted for the final mark.

3 TAMTAMS MODULES

One of the most prominent features of TAMTAMS WEB is the possibility to analyze not only simple devices but complex systems built upon these devices. This is a very useful feature both for teaching and for research purpose. When a new device is developed it is relatively easy to measure its parameters, but it is difficult to verify how these parameters influence the system behavior. However with TAMTAMS WEB this is a result that is very simple to obtain. In this section we briefly describe all the modules available at the time of writing in TAMTAMS WEB. The web page containing the modules selection

can be observed in Figure 3.D. The list of modules available was decided with the aim of evaluating the most important metrics for devices used in the digital electronics field. Digital electronics is the field where the CMOS scaling has the highest impact [23]. However TAMTAMS Web is an always evolving tool, as a consequence new modules to evaluate additional performance metrics will be added in the future.

3.1 Device

The device level is the most basic analysis currently available. In electronics, the “devices” are the basic building block of circuits. For examples transistors and diodes are normally classified as “devices”. Figure 4.A shows the device structure of a NMOS, while Figure 4.B depicts the device structure of a PMOS. NMOS and PMOS are the main “devices” available in CMOS technology. A device level analysis consists in the study of a device basic figures. In MOSFET technology dif-

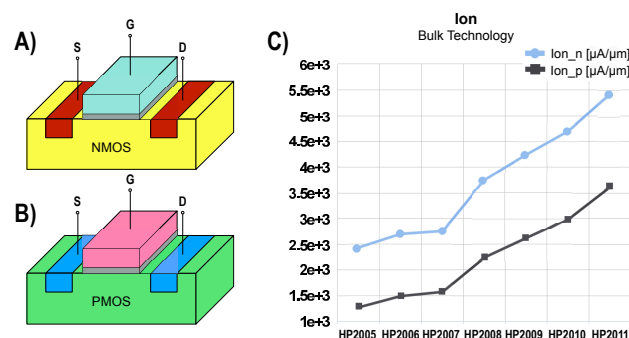


Fig. 4. Device Level. It is characterized by the basic devices and their parameters, like direct and leakage currents and voltages. The basic device in case of MOSFET technology is either a NMOS (A) or a PMOS (B). C) Example of results obtained by a device level analysis, Ion current behavior for different technology nodes.

ferent figures can be identified, however the most important ones are the THRESHOLD VOLTAGE (V_{TH}) [24], the ELECTRONS/HOLES MOBILITY, the DRIVE CURRENT (ION) [25] and the SUBTHRESHOLD CURRENT (IOFF) [26]. In TAMTAMS WEB for all these figures few different mathematical models are available. The V_{TH} calculation requires some additional modules, that evaluates correction factors required to obtain an accurate result. To get a better idea of the kind of results that can be obtained using TAMTAMS WEB, Figure 4.C depicts a Ion analysis considering several technology HP nodes, both for a NMOS and for a PMOS. The typical behavior of Ion can be observed, it increases with the technology advancement and transistors scaling. Alongside these fundamental parameters, TAMTAMS WEB allows the evaluation of some important benchmarking quantities, like the ratio between the supply voltage and threshold voltage (V_{DD}/V_{TH} , the ratio between Ion and Ioff (I_{ON}/I_{OFF})).

and the transistor timing constant (τ). The last parameter that can be evaluated is the GATE TUNNEL CURRENT (I_{GATE}) [27], the most important source of leakage in scaled MOSFET transistor. I_{gate} is a critical parameter in current technology. It increases exponentially with the reduction of gate oxide thickness, so it represents one of the most important limiting factors to the transistors scaling. At the time of writing several mathematical models are available to analyze I_{gate} .

3.2 Gates and Interconnection

The device level analysis is clearly fundamental, but alone it is not enough. Logic gates are built upon transistors, their performance are related not only to the value of device parameters but they are also related to the gate behavior. As an example it is possible to consider a simple NAND gate, which 3D-structure is depicted in Figure 5.A (just a simple example). Depending on

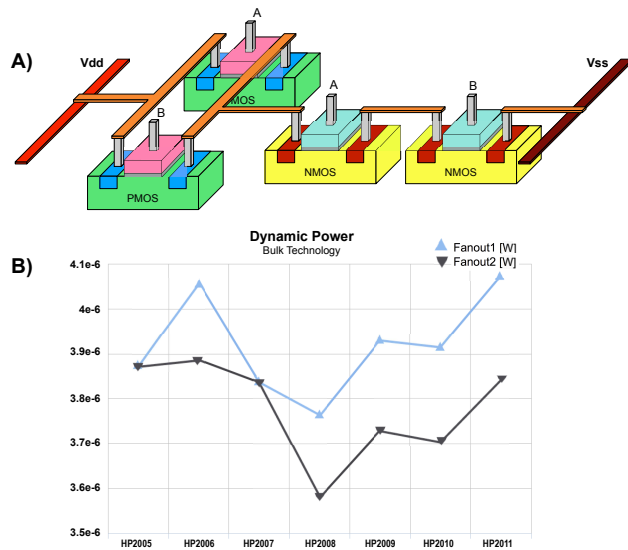


Fig. 5. Logic Gate Level. It is characterized by logic gates performance and interconnection parasitic parameters, like Capacitance and resistance. A) Example of CMOS NAND gate. B) Example of results obtained by a logic gate level analysis, dynamic power consumption of an NAND gate considering a different fanout and several technology nodes.

the input signals fed to the gate, in a given time some transistors will be active and some will be switched off. As a consequence, to evaluate the power consumption of the gate, for the active transistors the I_{on} current must be considered, while for the transistors switched off the I_{off} must be instead used. This example clearly highlights the difficulties encountered studying the transistors scaling process. If a smaller transistor has a higher I_{on} but a much smaller I_{off} , it is possible to expect a global reduction in power consumption for the whole gate. If instead a scaled transistor has a slightly smaller I_{on} and

a much bigger I_{off} , it is possible to expect an increment in power consumption. The situation is much more complex considering the possibility of having different gate types, and big circuits built using those logic gates. TAMTAMS WEB offers a good solution to this problem, with its ability to tackle the entire analysis flow, from device to system level. At this moment only NAND/AND gates and FLIP-FLOPS can be studied. The NAND/AND gate was chosen because complex circuits are often represented in terms of number of equivalent gates. The NAND gate is one of the most common choices in terms of equivalent gates selected. The figures evaluated by TAMTAMS WEB are mainly power consumption and currents. Figure 5.B highlights the analysis results of a NAND gate, considering the dynamic power consumption with different fanout configurations, with several technology nodes.

Additional analysis includes the parasitic characteristics of interconnection lines. Interconnection wires are a fundamental part of any electronic circuit. There are different types of interconnections, from local interconnections among logic gates to global interconnections. Interconnections are therefore related to both logic gate and system level. The interconnection parameter that can be studied are RESISTANCE, CAPACITANCE, INDUCTANCE and CROSSTALK among wires. Interconnection parameters are important because in scaled circuits, delay of interconnection wires is becoming a critical issue [28] [29].

3.3 System

The system level is represented by large circuits made by hundred of thousands of logic gates and transistors. The characteristic of such system is that they are normally composed by many different parts interconnected. For example a real chip will probably have a part made by logic gates, another part made by flip-flops and possibly also an embedded memory. A thorough analysis of such system is almost impossible, given the total amount of possible combinations available. Up to now in TAMTAMS WEB four modules are available, each module represents a simplified system. The LOGIC GATES AND REGISTERS module allows to evaluate power consumption of a generic system made by an arbitrary number of logic gates and registers, the amount is set in the system parameter page (Figure 3.B). Similarly the ON-CHIP MEMORY module allows the evaluation of a generic memory. Memory characteristics, like size, are decided in the system level page (Figure 3.B). The other two options, the INPUT/OUTPUT PADS and the INTERCONNECTIONS modules, allow the estimation of power consumption for I/O pads and interconnections respectively. Together with this generic high level modules we are developing a series of modules tailored on specific circuits, like FPGAs, memories and several combinational blocks.

Examples of results that can be obtained at system level are depicted in Figure 6. Figure 6.A depicts the

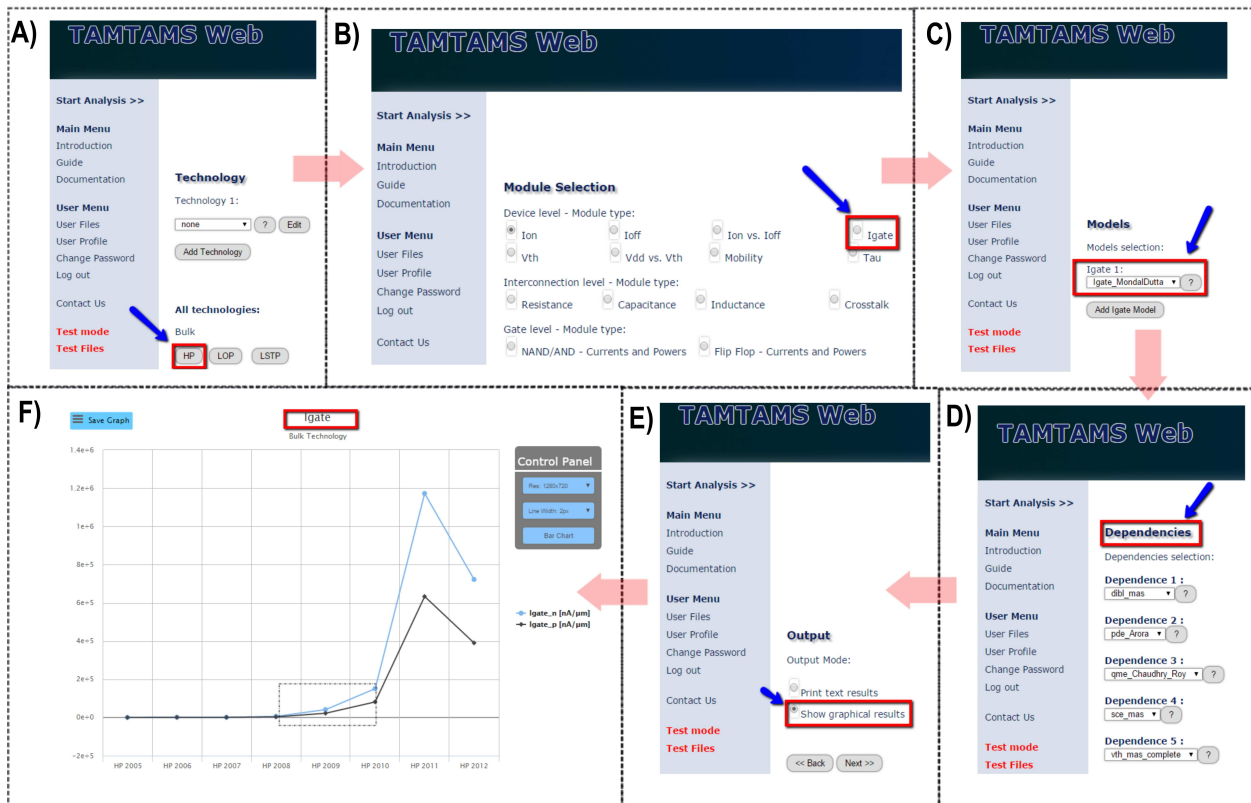


Fig. 7. Case of study. Igate analysis considering several technology nodes. A) Technology selection. B) Module selection. C) Model selection. D) Dependencies selection. E) Output type selection. F) Output result.

estimated dynamic power consumption of a CLB block of an FPGA considering BULK technology. Figure 6.C depicts instead the same result obtained for SOI technology. It is important to remark that system level modules are based on both device and logic gate level modules, so changing the technology node lead to a change in power consumption at system level. Further system level blocks are in development to further enhance the capabilities of TAMTAMS WEB. These new models will be focused on specific circuits and architectures, but they will also improve the number of analysis that can be done, considering for example circuits timing, IR Drop, thermal issues and electromigration [30].

4 CASE STUDY

In this section we describe three examples representing possible analyses that students can perform using TAMTAMS WEB. The aim of this section is twofold. To highlights how TAMTAMS WEB is useful and powerful as a learning tool, and to provide to the reader of this paper a better understanding of the features previously described.

The **first analysis** is the most classical available in TAMTAMS WEB, the study of how a specific parameter change with the technology node. The parameter of

choice is the Igate. As previously stated the leakage current due to the tunnel effect in the gate oxide is one of the most critical issues in scaled CMOS transistors. TAMTAMS WEB enables the analysis of this concept according to the following steps.

- 1) The analysis starts choosing the technology node to be used (Figure 7.A). For this example we have chosen the High Performance (HP) family. By selecting the option *HP* (Figure 7.A) an automatic selection of all the technology nodes available for HP family is executed.
- 2) Advancing to the next page the student is prompted the selection of the module type (Figure 7.B), which in this case is Igate.
- 3) For Igate different mathematical models are available, in this case in the next page (Figure 7.C) we have selected in this example the model created by Mondal and Dutta in [31].
- 4) The next page leads to the dependencies selection (Figure 7.D). To calculate the value of Igate some quantities calculated in the Vth module are required. The system automatically loads the Vth module and other four modules required to evaluate Vth. TAMTAMS WEB is able to recognize all the modules required in the dependency tree. For each

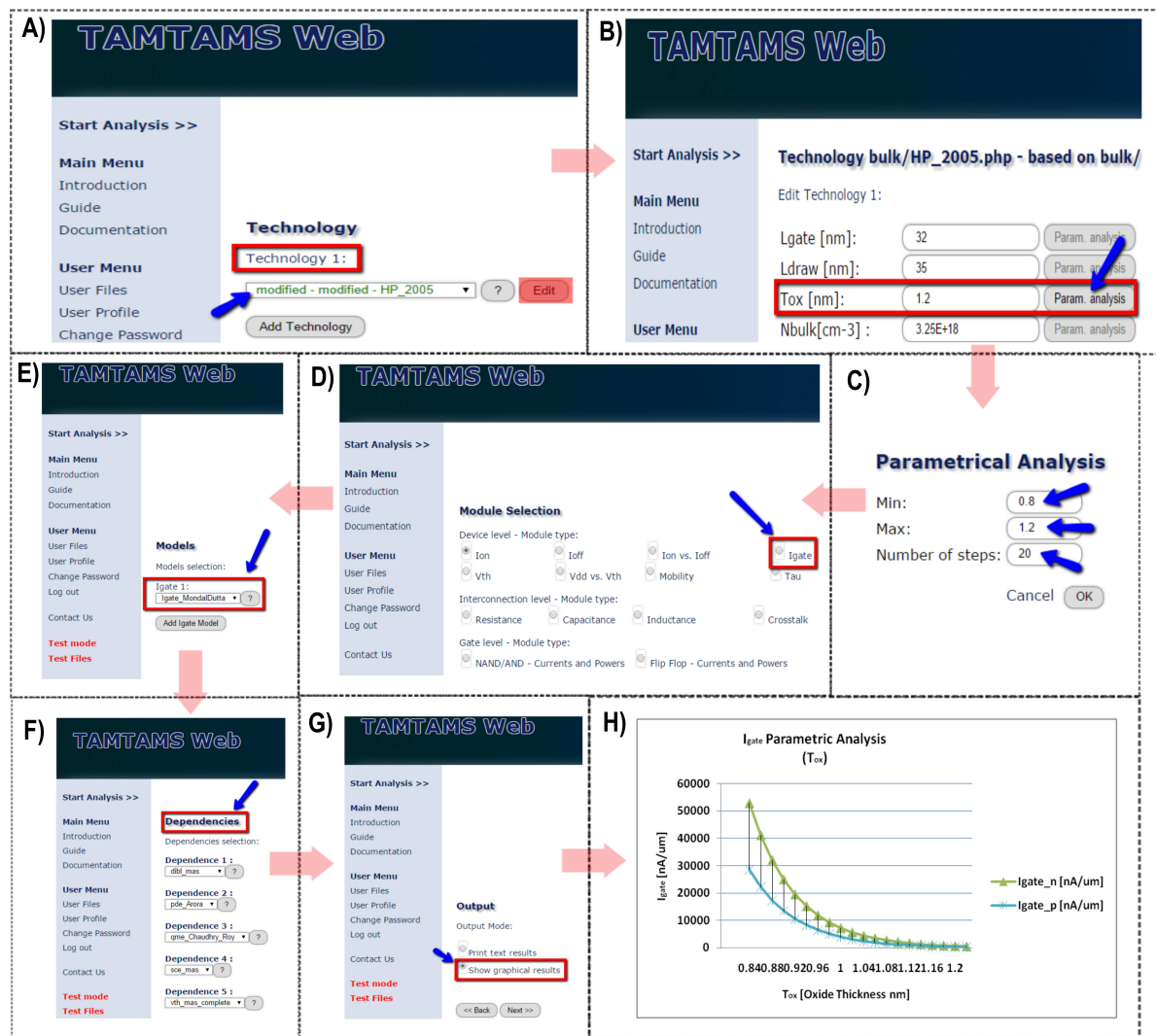


Fig. 8. Case of study. I_{gate} parametric analysis choosing one specific technology node and varying the oxide thickness. A) Technology selection. B) Choice of the parameter to be changed. C) Setting of the parameter range to be used in the analysis. D) Module selection. E) Model selection. F) Dependencies selection. G) Output type selection. H) Output result.

module a default mathematical model is selected, but they can be changed by the user (Figure 7.D). In this case we leave all the models as default.

- 5) The next page allows the selection of the output format (Figure 7.E). In this case we choose "Show graphical results".
- 6) Finally in the next page the graph is generated (Figure 7.F). The results show the value of I_{gate} for NMOS and PMOS for all the HP technology nodes from 2005 to 2012.

Looking at the results of (Figure 7.F) a student appreciates that I_{gate} increases in the case of most recent nodes, as expected, but also notices the strange unexpected huge spike in the most recent nodes. the explanation relies on the fact that I_{gate} is related to the tunnel barrier in the gate oxide, so the two key parameters

that influence its value are the oxide thickness and the oxide material. Both contributions can be analyzed using TAMTAMS WEB in the **second analysis**. The oxide used in the previous analysis was silicon dioxide (SiO_2). Let us start from the oxide thickness doing a parametric analysis and leaving the oxide type unchanged.

- 1) From the technology selection page, a single technology node, the HP2005 is selected (Figure 8.A). Selecting the *Edit* option, leads to the web page that allows to change the value of technology parameters.
- 2) After being prompted in the technology parameter web page, the line corresponding to the gate oxide thickness (T_{ox}) should be found. the selection of the option *Param. analysis* (Figure 8.B) allows to change the parameter range for the parametric



Fig. 9. Case of study. System level analysis considering two different models of Igate. A) Technology selection. B) Module selection. C) Models selection. Two models are analyzed in parallel in this case. D) Dependencies selection. E) Output type selection. F) Output result.

analysis.

- Now it is possible to set the range to be used in the parametric analysis and the number of steps in which the range is divided. For this analysis we choose as minimum value 0.8nm, a value similar to the oxide thickness of HP2011 and HP2012 nodes. The maximum value is instead equal to the nominal HP2005 value, 1.2nm. The number of steps is set to 20.
- The next steps are similar to the previous case, first it is necessary to select the module, Igate in this case (Figure 8.D).
- We choose again the Mondal-Dutta [31] model for Igate (Figure 8.E).
- Dependencies are left with the default value (Figure 8.F), in order to perform the analysis in the same conditions of the previous case.
- The output mode is set again in graphical mode (Figure 8.G).
- The next page shows the results of the analysis (Figure 8.H). Two curves, one for NMOS and one for PMOS are generated, showing the behavior of Igate with the decrement of oxide thickness. The graph depicted in Figure 9.H is obtained with a post-processing for clarity purposes.

The results are coherent with Figure 7.F. When the oxide

thickness is similar to the HP2011 and HP2012 cases, the Igate current is extremely high, but it decreases exponentially increasing the oxide thickness. With a thickness of 1.2nm, the value is orders of magnitude smaller. As a consequence students learn the critical effect that the oxide thickness has on scaled transistors.

However, the gate leakage current is also influenced by the type of oxide used. To understand this behavior and, at the same time, to understand the impact of gate leakage current on power consumption a **third analysis** is described. The analysis is performed considering again all the HP technology nodes, evaluating power consumption with a system module. Two analysis are carried on in parallel using two different mathematical models for Igate and two different types of oxide.

- In the technology selection page, all HP technologies are selected (Figure 9.A).
- In the module selection page, the *Power Consumption - Logic Gates and Registers* is selected (Figure 9.B).
- In the model selection page (Figure 9.C) only one model is available. However, by selecting the option *Add Static Power Model*, it is possible to perform two analyses in parallel on the same system model. This can appear pointless but the reason behind this choice will be clear in the dependencies selec-

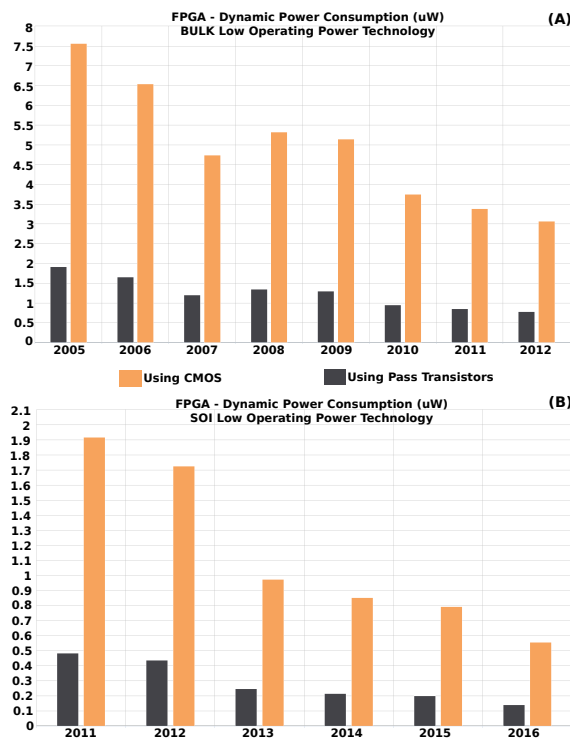


Fig. 6. System Level. It is characterized by performance analysis of generic circuits made by a large number of devices and logic gates. A) Dynamic power of a CLB block of an FPGA considering BULK technology. B) Dynamic power of a CLB block of an FPGA considering SOI technology.

tion page. It is worth noticing that further analysis (theoretically an infinite number) can be conducted in parallel.

- 4) In the dependencies selection page (Figure 9.D), all the dependencies for the two modules previously selected will be automatically loaded. A system module is at the top of the hierarchy, so the list of dependency modules is very long and not reported in Figure 9.D for space reason. However, this page explains while we have selected to perform in parallel two analysis on the same system module. The reason is simple, we are going to change the default model for Igate. In this way it is possible to launch two parallel analysis on the same system model, but one analysis will use the Mondal-Dutta model using SiO_2 as oxide, while the second analysis will use the model developed by Yeo and all in [32] using Hafnium Dioxide (HfO_2) as gate oxide. This choice was made to highlight the flexibility of TMTAMS WEB, that allows to compare different models and different combination of models.
- 5) The output mode is set again in graphical mode (Figure 9.E).
- 6) Advancing to the next page prompts the user to the generation of the final graphs. Figure 9.F shows a

post-processed graphs, where only the static power consumption of the two analysis is depicted. This choice was made to obtain a more clear figure. The graphs highlight that the Yeo model, which uses a better oxide material, leads to a power consumption orders of magnitude lower. As a consequence the influence of gate oxide material can be clearly understood.

The analyses here reported are just three of many possibilities offered by TMTAMS WEB. However they highlight the power and flexibility of our tool as teaching instrument. Furthermore we are continuing to work on it expanding the options available to further enhance its teaching potential

5 CONCLUSION

In this work we have presented TMTAMS WEB, a tool that we specifically developed to analyze, predict and compare scaled MOSFET transistors and emerging technologies. With the goal to make micro and nanoelectronics technologies easy to understand, TMTAMS WEB was developed around a web interface. It was created having in mind with students and researchers to effectively teach the technology to the first and to help the second in their research activity. This tool has the advantage to merge seamlessly device and system analysis together, considering different technologies, wrapping the analysis in a easy-to-use and open web structure.

Our current activity is focused mainly on improving the number of technologies and models available for the analysis. At the same time we are tweaking and improving the web interface, to enhance the tool capabilities. In the future we are planning a complete renovation of the interface, transforming the sequence of web pages that now compose TMTAMS WEB in a parallel interface, where all the options are available in a more refined and easy to use structure.

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