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Enhanced Macromodels of High-speed Low-Power Differential Drivers

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Abstract—**High-speed differential interfaces implementing specific solutions for low-power consumption and low-EMI disturbances are vastly used in mobile platforms. In these devices, the slew rate is suitably controlled, the communication scheme alternates data-bursts followed by power-saving states, the voltage swing and the common-mode level are reduced. To achieve these targets, a key role in voltage-mode output drivers is played by an internal voltage-regulator. The latter exhibits a rich dynamic behavior, with non-negligible effects on the transmitter outputs, that need to be carefully characterized. In this paper, a modeling strategy based on a few key enhancements of state-of-the-art solutions is presented, leading to compact and accurate models. The feasibility and strengths of the proposed approach are verified on a low-power high-speed voltage-mode driver.**

I. Introduction

In recent years, the amount of data being transferred between processing units on a mobile device has been significantly and continuously increasing. High-speed communication protocols, whose physical layer implements differential signaling, are vastly used (USB, PCIe, MIPI DigRF, MIPI LLI, MIPI CSI/DSI, etc.). Differential signaling enables high datarates (up to several Gbps), offers good crosstalk immunity, and requires a very limited number of pins. The most advanced communication protocols carefully handle and try to minimize power consumption, using several techniques. For example, data-transfer modes (often called *burst*-modes) are alternated with power-saving modes, the signaling datarate is dynamically adapted based on the instantaneous amount of data to be transmitted (ranging from kbps up to several Gbps), and output voltage swing and the common-mode level are reduced.

This paper focuses on high-speed low-power voltage-mode drivers for mobile applications. Specific emphasis is placed on the effects of internal voltage regulators, that unavoidably introduce a rich dynamic behavior on the output common-mode voltage. This behavior can be hardly reproduced by the existing state-of-the-art modeling solutions (e.g., IBIS [1] or Mπlog [3]–[5]). To overcome the above limitation, enhanced models based on the Mπlog class are presented and demonstrated on a high-speed driver for Gbps-range data transfer, implemented in a leading-edge silicon CMOS technology.

II. Low-power High-Speed Voltage-Mode Drivers

A common circuit topology for high-speed low-power differential transmitters is depicted in Figure 1; a similar topology is presented in [2]. A voltage-mode output driver (*H-bridge*) is supplied by a low-dropout voltage regulator (LDO) and driven by a Pre-Driver stage. The Pre-Driver implements slew-rate control, output impedance configuration, and PVT compensation, by activating a certain amount of the n available replicas of the output-stage. The internal LDO is a fundamental component: it shifts the supply voltage from a higher level (VDDLDO) to a lower one (V_{LDO}), contributing to reject supply-noise and attempting to prevent voltage ripples on its output due to the switching activity on the H-bridge.
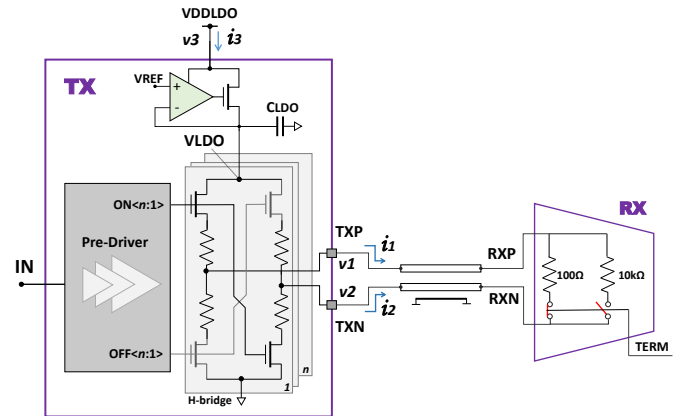

Fig. 1. Topology of a high-speed differential transmitter and its connection to a target receiver.

For a given logic state, when the transmitter is terminated with 100Ω (*burst*-mode), a constant current is provided by the LDO to the output stage, and the capacitor C_{LDO} is charged to V_{LDO}. $ON \langle n:1 \rangle$ and $OFF \langle n:1 \rangle$ signals are driven in a complementary manner by the Pre-Driver, and determine whether the current to the load is positive or negative, implementing the differential signaling. However, asymmetries during switching events create dynamic current variations around the constant value provided by the LDO. Small current variations can be sustained by C_{LDO}. Larger variations require instead the intervention of the slower regulation loop, which originates a voltage bounce on V_{LDO}. This bounce is visible only on the output terminal connected to the pull-up resistor, hence building an instantaneous common-mode variation (e.g., at the receiver side $VCM_{RX} = (V_{RXP} + V_{RXN})/2$). Figure 2 illustrates the dependency of the dynamic fluctuations of V_{LDO} on C_{LDO}.
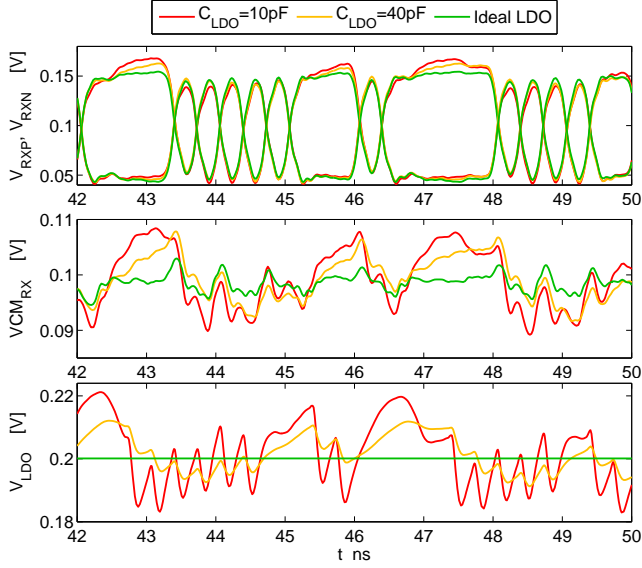
Fig. 2. Impact of C_{LDO} on V_{RXP}, V_{RXN}, VCM_{RX} and V_{LDO}.

The LDO is usually composed of an operational amplifier in negative feedback configuration, that suitably drives a MOS transistor and, together with C_{LDO}, provides a regulated and stable output voltage V_{LDO} equal to V_{REF}. A highly stable V_{LDO} would be desirable, but this would require a large C_{LDO}. On top of requiring a large area, this would also limit the performance during mode-switching among burst (terminated receiver) and power-saving (unterminated receiver) states. The activation/deactivation of the termination causes a large variation of the LDO output current, partially discharging C_{LDO} and triggering a slow transient on V_{LDO}. The resulting voltage bounce heavily depends on the value of C_{LDO} and on the operational amplifier bandwidth and gain figures. Capacitance of C_{LDO} is thus a critical design parameter for the LDO.

For this class of high-speed driver topology, if common-mode noise figures are of particular concern for the target differential interface to be supported, a suitable macromodeling flow needs to be adopted, in order to carefully reproduce these LDO-induced effects (see the middle panel of Fig. 2).

III. MπLOG MACROMODELING

This Section proposes a strategy for the generation of accurate and efficient macromodels for the output and supply ports of high-speed differential drivers, considering the above-described effects.

Two-piece representations based on the so-called MπLog modeling methodology [3] have been successfully exploited for describing both the output and the supply currents i_1, i_2 and i_3 as functions of the port voltages (figure 1). These currents are modeled for $\ell = 1, 2, 3$ as

$$i_\ell(t) = w_{\ell H}(t)\, i_{\ell H}(v_1, v_2, v_3, d/dt)$$
$$+ w_{\ell L}(t) i_{\ell L}(v_1, v_2, v_3, d/dt) + \delta_\ell(t), \quad (1)$$

where $w_{\ell H}$ and $w_{\ell L}$ are time-dependent weights accounting for state transitions driven by the input voltage $v_{in}(t)$. In fact, the above representation does not include the input voltage in the model structure explicitly, in order to simplify the identification of the model parameters. In (1), $i_{\ell H,L}$ are parametric submodels describing the device behavior at fixed logic state, and $\delta_\ell(t)$ is an optional additional term taking into account the current drawn by the corresponding pin during state switching, and arising from some specific internal features of the device.

Submodels $i_{\ell H,L}$ are conveniently decomposed into the sum of static and of dynamic parts:

$$i_{\ell H,L} = F_{\ell H,L}(v_1, v_2, v_3) + f_{\ell H,L}(v_1, v_2, v_3, d/dt) \quad (2)$$

where $F_{\ell H,L}$ is a multidimensional static surface, and $f_{\ell H,L}$ is a parametric linear dynamic submodel formulated in the discrete-time $t = kT$, being k the discrete-time variable and T the sampling period.

The key steps of the proposed modeling procedure are summarized below.

- *Multivariate static characteristics*. The first step of model identification is the approximation of the device static characteristics by means of compact representations of the mutivariate maps $F_{\ell H,L}$. A number of alternative approximations have been proposed in the past, based on radial or sigmoidal basis functions, global or piecewise polynomials, or even more complex structures belonging to the class of neural networks. All these approaches, however, share the same limitations arising from the application of general nonlinear optimization methods, leading to possible inaccuracies and/or involving a large number of model components.

  We adopt here the alternative yet effective solution recently proposed in [4], based on the construction of empirical basis functions obtained from a set of "measurements" collected from reference transistor-level SPICE simulations. This approach is general and robust. In addition, it offers intrinsic compression capabilities, since a minimal number of basis functions is obtained via standard Singular Value Decomposition (SVD) or its higher-dimensional tensor generalization. What is even more important, the SPICE implementation of the model turns out to be very efficient and can be achieved using standard voltage controlled sources.

- *Dynamic submodels*. Once the static submodels $F_{\ell H,L}$ are available, the identification of the dynamic parts $f_{\ell H,L}$ is performed via standard tools for system identification. Among the large number of linear system identification methods, we adopt here the Time-Domain Vector Fitting (TD-VF) algorithm [6]. The main advantages offered by this method is its robustness and its ability to handle stiff systems, with poles having different orders of magnitude. This is a specific feature of the system under consideration, due to the slow dynamic components introduced by the LDO. A rational approximation of the frequency response of submodels $f_{\ell H,L}$ is obtained by detrending
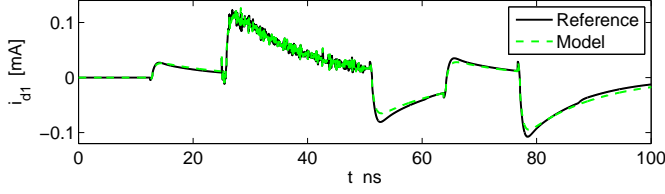
Fig. 3. Dynamic contribution of the current $i_1(t)$ for a driver forced in the 'H'-state and connected to a noisy multi-step voltage excitation signal $v_1(t)$. Solid line: reference; dashed line: rational-based model response with three poles.

transient SPICE responses of the full transistor-level circuit from their static contribution $F_{\ell H, L}$, and feeding the resulting signals to the TD-VF scheme. Figure 3 demonstrates the good accuracy that is obtained. The curves highlights also that a linear rational-based model unavoidably introduces some minor differences, mainly due to residual nonlinear dynamic components, which are ruled out by the assumed model structure.

- *Weighting functions*. Once the submodels are completely defined, the computation of the weighting functions $w_{\ell H, L}(t)$ is carried out via linear inversion of (1) form from a set of switching voltage and current waveforms recorded during state transitions events on two lumped loads [3].

As suggested in [5], to further improve robustness of the identification process, and to improve the accuracy of the generated models, the representation (1) is recast in terms of transient (discrete-time) scattering waves. The port voltage and current variables v_ℓ and i_ℓ are suitably replaced by the corresponding scattering companion variables. Readers are referred to [3]–[5] and references therein for an in-depth discussion and additional details.

IV. APPLICATION TESTCASE

The enhanced Mπlog macromodeling flow has been applied to a high-speed voltage-mode differential driver for a low-power differential signaling, implemented in a leading edge CMOS technology. The output voltage levels are compatible with state-of-the-art electrical specifications of real communication interfaces in mobile platforms, with a datarate set to 3 Gbps. Two scenarios have been analyzed: a driver with an ideal LDO (replaced with an ideal DC voltage source), and the same driver but using a real LDO and $C_{LDO} = 40\text{pF}$.

Mπlog and IBIS models have been generated for each of the two cases. Figure 4 demonstrates how a non-ideal LDO introduces variations on the output terminal, whose connection to the pull-up resistor depends on the logic-state, resulting in increased common-mode noise. Mπlog models show a good accuracy compared with the results obtained using the reference transistor-level netlists; this is valid both for the ideal and non-ideal LDO case. IBIS models, in a pseudo-differential configuration, appear to limited for this specific application: being the LDO dynamics usually much slower than the bit period, this effect cannot be reproduced in the IBIS *V-t* tables.
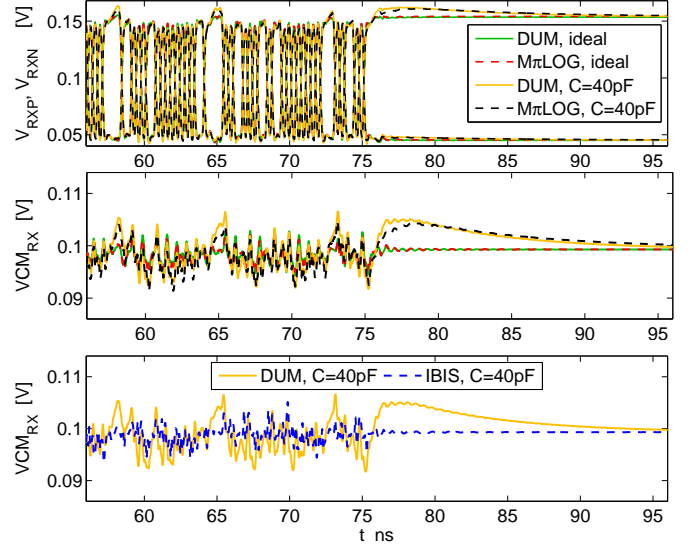

Fig. 4. Waveforms comparison: Transistor-level (DUM, Device Under Modeling) versus Mπlog-based and IBIS-based time-domain simulations

V. CONCLUSIONS

A systematic discussion on the effects of voltage regulators on the outputs of low-voltage differential drivers is presented; a specific emphasis is placed on the modeling aspects that are critical for reproducing common-mode voltage fluctuations. To achieve this goal, enhanced Mπlog-class macromodels are presented. The rich dynamic effects of internal LDOs are captured by rational submodels identified using the Time-Domain Vector Fitting algorithm. The multivariate static characteristics in fixed logic states are instead captured by a truncated Singular Value Decomposition, leading to optimal compact sparse representations. The proposed macromodeling technique was successfully applied to a real transmitter for low-voltage differential signaling operating at 3 Gbps.

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