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29 June 2024

Hierarchical Modeling of OPV-based Crossbar Architectures

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Abstract— **Recently, molecular devices with interesting behaviour like conductance, switching, rectification, gate modulation and negative differential resistance were realized. In this paper we propose a method to model hierachical logic circuits based on Oligo-Phenylene Vinylene (OPV) molecular field effect transistor (MOLFET). The modeling is based on a device level spice equivalent model and on a versatile language (VHDL-AMS) assuring a hierarchical description and a successive approximation approach. Elementary logic blocks as well as a more complex circuit (RCA) were designed and simulated with a crossbar organization, both in a NMOS-like and in a CMOS-like configuration.**

Molecular transistor, Circuit Modelling, Nonlinear devices.

I. INTRODUCTION

Molecular devices can play an important role in emerging future nanoelectronics with advantages in terms of functional density and integration. These devices were able to provide features like rectification, negative differential resistance and conductance switching [1]–[6]. Recently molecular electronics has gained a great interest from both a theoretically and an applied electronics point of view. A lot of work, mostly based on first-principle or semi-empirical , has been performed in order to understand the physics of molecular devices. The commonly used methods include Density Functional Theory [7], [8], Non-Equilibrium Green's Function [9], [10] and semi-empirical methods [11], [12].

However, less effort has been devoted for the circuit modelling of molecular system. Some studies were focused to provide a circuit analogy to first principle calculation [13]. A circuit model for bistable molecular crossbars was presented in [14]. Recently, a modeling methodology for molecular devices in terms of circuit elements was introduced in [15]. The behavior of logic systems based on sets of molecules as elementary devices can be well predicted by such concrete models. And beyond, a crucial leverage resides in the possibility on the one hand to refine the model according to the level of accuracy required, and in the other hand to describe complex logic circuits, for evaluating the impact of detailed physical level characteristics on realistic circuits performance. With these purposes we adopted a flexible methodology based on a versatile hardware description language favoring both hierarchical descriptions and successive approximation modeling.

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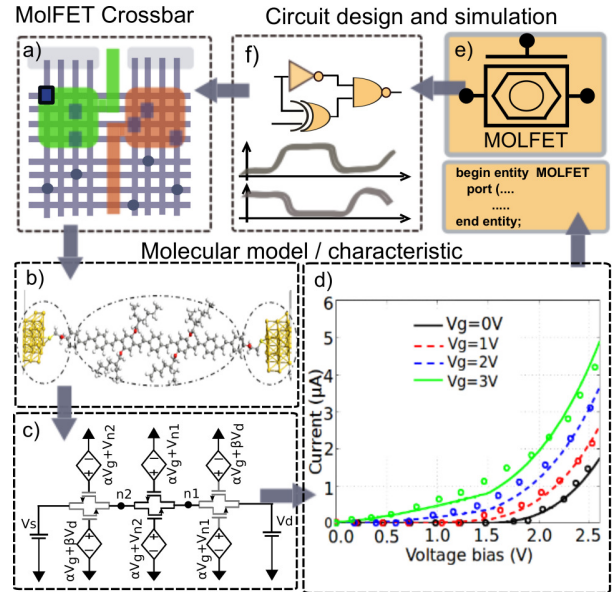
Fig. 1. From device modelling to circuit simulation: (a) molecular transistor (MT) based crossbar architecture, (b) OPV molecular transistor (MT) with the oxygen linker group on both terminals, (c) equivalent circuit model for MT, (d) current-voltage (IV) characteristic, (e) modular HDL circuit description, (f) hierarchical circuit implementation and simulation.

In this paper, we use a molecular circuit modeling methodology involving a gated OPV device presented in [15] to build elementary logic circuits based on a crossbar architecture [16]. Figure 1 shows the design flow for hierarchically creating the circuit. Figure 1(b) shows the OPV molecule [17] with two oxygen linkers on both sides employed. The corresponding circuit modeling detailed in [15] is shown in Figure 1(c).

The employed molecular circuit modeling methodology allowed to obtain a strong matching of the I-V characteristics of the gated OPV device [15] as shown in Figure 1(d). The transistor model is included in a VHDL-AMS description (Figure 1(e)) and is enclosed within a hierarchical device-to-logic-elements structure (Figure 1(f)). We then defined the structure of a library of elementary logic circuits using a crossbar architecture [16] and exploiting the features of VHDL-AMS for the hierarchical modeling and the structure organization. We built elementary logic blocks such as inverters, NOR gate, NAND gate and Half Adder. We used the library to design more complex logic architectures based on a hierarchical organization. Here we consider a 3-bit Ripple Carry Adder (RCA) as a simple case of study.

The paper is organized as follows. First the methodology

used in this paper is discussed. Afterwards, issues related to non-linear behavior of molecular devices in circuit simulation are explained. Finally, the simulation results of different logic circuits in crossbar like architecture using OPV-based molecular transistor are discussed.

II. METHODOLOGY

In this section we firstly explain the electrical behavior of the molecular transistor and how the equivalent electrical model is defined (see Section II-A). In Section II-B the equivalent electrical model implemented in Spice is described and then a description of how it is encapsulated in a hierarchical system design is reported. The section ends with the extension of this method to the complementary MOLFET architecture (see Section II-C).

A. Circuit implementation with N-type MOLFET and molecular resistor

The circuit in Figure 2 resembles the implementation of an N-type MOS logic. The resistors in the circuit can be realized using molecules with high insulating property, like the saturated methyl chain [18] illustrated on top of Figure 2(a). The simplest logic gate we tested is the cascade of two logic inverters (Figure 2(a)). It is important, for obtaining a proper logic operation, i) to set-up the resistance values, ii) to define the logic levels, and iii) to define the input and output voltages for the two stages. The first stage IN and OUT voltages are V_{in}^1 and V_o^1, respectively, that are chained with the second stage IN and OUT voltages $V_{in}^2 = V_o^1$ and V_o^2, respectively. Similarly to MOS logic, in order to guarantee the proper switching, V_{oH}^1 has to be higher than V_{inH}^2 (recognized as high input level), while V_{oL}^1 has to be lower than V_{inL}^2 (defined as low input level). Differently from an ideal MOSFET, the output value (i.e V_{ds}) influences strongly the behavior of the MOLFET: as shown in Figure 1(d), for $V_g = 0V$ the molecular device starts conducting when the bias voltage (V_{ds}) is greater than approximately $1.5V$, which is defined as a threshold voltage for the low logic level, V_γ (V_{inL}) (which depends on the input voltage). Since $V_{oH} = V_{ds}$, to keep the MOLFET off V_{oH} has to be lower than $1.5V$. If the low logic level at the input is not exactly equal to $0V$, V_{oH} should be reduced to avoid that the MOLFET starts conducting. On the other hand, for high input, the V_{oL} has to be higher than the threshold voltage V_γ (V_{inH}), which depends on the high level input voltage. To summarize, for the two inverters to work properly in cascade, the following conditions have to be fulfilled:

$$V_{inH} \leq V_{oH} \leq V_\gamma(V_{inL}) \qquad (1)$$

$$V_\gamma(V_{inH}) \leq V_{oL} \leq V_{inL} \qquad (2)$$

The fulfillment of this condition could require a tuning of the MOLFET, enhancing the coupling between the molecule and gate electrode. This can be realized technologically by reducing the thickness of the oxide layer used in the device (it was originally 200nm [17]). For $\alpha = 0.08$, V_{inH} has to be higher than $3V$, but it is not compliant with the
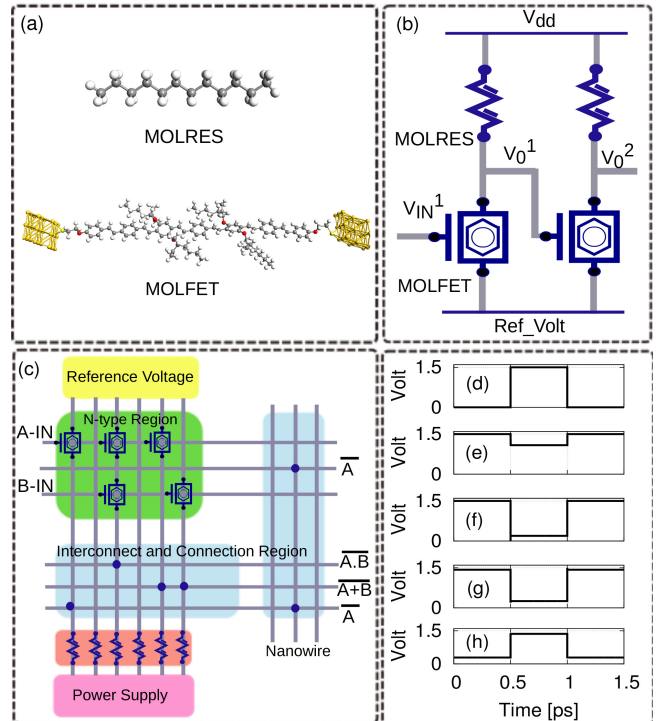

Fig. 2. (a) Saturated methyl chain used as molecular resistor and OPV molecule as Molecular transistor. (b) Logic structure of two cascade inverters. (c) Crossbar architecture of basic logic circuits. (d) Input waveform for inverter. (e) Output waveform of inverter having bad swing for next cascade inverter ($\alpha = 0.08$). (f), (g) and (h) Output waveforms of 1st, 3rd and 6th stage inverter, respectively, with improved gate coupling ($\alpha = 0.2$).

maximum allowed output voltage of the previous stage. Thus, cascading more than one inverter would not work properly, as demonstrated in Figure 2(e). We therefore set the coupling α to 0.2, which allows a complete switching at bias gate smaller than $1.5V$, see Figure 2(f).

B. Circuit level description

We simulated all the blocks using Advance MS (ADMS) 2008.1 by Mentor Graphics and verified the correct circuit behavior. ADMS is a powerful designing tool that allows us mixed signal analysis. Spice circuits and models can be integrated into VHDL-AMS. ADMS uses Eldo engine for this purpose. An example of the methodology adopted with both the electrical and structural descriptions is reported in Figure 4 for the case of an inverter. In first part of the code (as shown in Figure 4), the spice description of molecular resistor $mol\_resistor$ and molecular transistor mol_fet are reported and linked to VHDL-AMS source file. In particular, the molecular resistance is modeled with a simple resistor, whose value is estimated from experimental measurements of current in methyl chain [4]. The SPICE model of the N-type molecular transistor is based on NMOS level 1 FET-model with typical parameter values of $Kp = 5 \times 10^{-7}$, $\lambda = 0$, $\gamma = 0.586$ and V_{th} fitted on experimental results [15]. The spice models is then incorporated by using property attribute in VHDL-AMS and used to build an inverter. Starting from this description, it is possible to design complex logic system
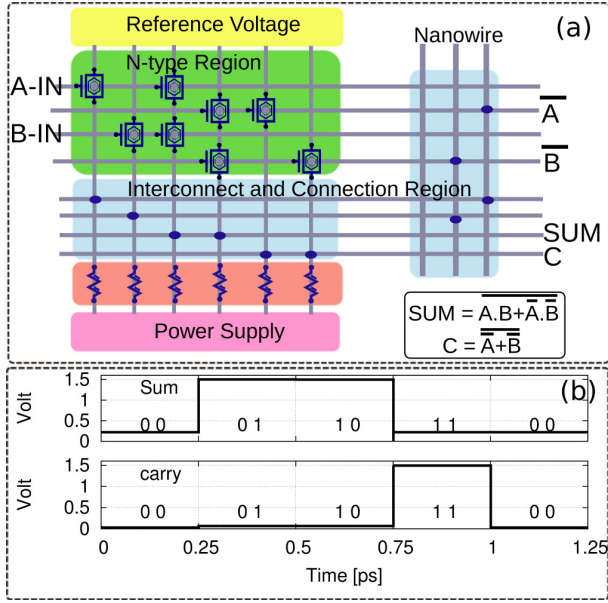
Fig. 3. (a) Crossbar architecture and (b) Output waveforms of Half Adder with improved gate coupling ($\alpha = 0.2$). Low input ($0V$) and high input ($1.5V$) values represents logic '0' and logic '1', respectively.

```
* Molecular resistor's Eldo sub-circuit
.SUBCKT mol_resistor A B
 r1 A B 50000K
.ENDS
* Molecular transistor's Eldo sub-circuit
.subckt Mol_FET NVD NVS NVG
.MODEL CMOSN NMOS (KP=5E-7 VT0=0.2 lambda=0 gamma=0.586)
.MODEL CMOSN2 NMOS (KP=5E-7 VT0=0.1 lambda=0gamma=0.586)
.PARAM ALFA1 {0.08}
.PARAM BETA  {0.46}
.PARAM BETA2 {0.8-BETA}
EVG1 NVG1 0 NVG 0 {ALFA1}
RD NVD N1 1K
RS N0 NVS 1K
**************LEFT REGION
BLU NLU NVG1 V=BETA*V(N0);BETA2*V(N0)*((VSS-
1.5)/2+ABS((VSS-1.5)/2))
 ....
**************RIGHT REGION
BRD NRD NVG1 V=BETA*V(N1);BETA2*V(N1)*((VDD-
1.5)/2+ABS((VDD-1.5)/2))
...
.ENDS
```

```
entity inverter is port (termial  inv_in, inv_out: electrical);
end entity inverter;
architecture  MOL_INV of inverter is
----- molecular resistor
component mol_resistor
        port ( terminal  A, B: electrical);
end component;
----- Attributes to link eldo and ams-----
        ...
----- molecular transistor
component mol_fet
        port (  terminal NVD, NVS, NVG: electrical);
end component;
----- link eldo and ams
----- Attributes to link eldo and ams-----
        ...
----- declaration of other components. terminals and Quantities
begin
----- N-MOLFET inverter
MOLRES1: mol_resistor port map (A => Vdd, B => inv_out);
MOLFET1: mol_fet      port map (NVG =>inv_in,
                               NVD=>inv_out, NVS=>Vss);
end MOL_INV;
```

Fig. 4. VHDL-AMS code of the N-type MT based inverter. The molecular resistor is described as a simple resistance with a value derived by experimental results. The N-type MT is based on NMOS level 1 FET-model.

using standard VHDL methodology. Moreover, in this way it is also possible to change a single parameter in the physical model without modifying the circuit level implementation and evaluate the impact on the system performance.

C. Circuit implementation with complementary MOLFET

A complementary structure based on both N-type and P-type molecular transistors would be preferable from the power consumption point of view. In this case the resistors in the crossbar are replaced by P-type MOLFETs as shown in Figure. 5(a), with the aim to reduce the dissipated power. We hereby assume having a P-type transistor of a symmetric behavior like the realized N-type one. This can be obtained modifying the molecule energy levels involved in the conduction mechanism: in the N-type case the conduction is mainly due to the Lowest Unoccupied Molecular Orbitals (LUMOs), while for the P-type MT the Highest Occupied Molecular Orbitals (HOMO) are interested. In order to address this issue, two possible solutions are available: changing the molecular structure to achieve the expected characteristics or involving a back-gate technique to shift the position of the energy levels with respect to the electrodes and thus change the type of conduction.

III. RESULTS

A. Circuit implementation with N-type MOLFET and molecular resistor

With the adjusted α and suitable methyl chain as a resistor, we designed and simulated some basic logic circuits like Inverter, NOR and NAND organized in a crossbar architecture (Figure 2(c)) [16]. The green box represents the N-type region, where the N-type MTs are placed. The light blue rectangles are the connection regions, necessary

to provide the proper interconnections among MTs in order to implement the logic functions and to forward the signals to the output pins. In the pink area, the molecular resistors are placed and connected to the power supply to provide the high logic value.

Regarding the inverter, Figure 2(d) shows the waveform provided as input signal. In Figure 2(e) an example of output waveform is reported for a wrong set of molecular parameters ($\alpha = 0.08$): the logic levels do not match with the requirements for the next cascaded inverter, as described by equations (1) and (2) in Section II-A. Considering $\alpha = 0.2$, the output waveforms of Figure 2(g)-(h) show that the voltage level for 3-stage and 6-stage cascaded inverter are maintained.

One possible nanowire crossbar architecture of an Half Adder (HA) is shown in Figure 3(a). The output waveforms for both "Sum" and "Carry" signals are reported in Figure 3(b). Also in this case with $\alpha = 0.2$ the voltage levels are maintained. Combining in a modular way the crossbar
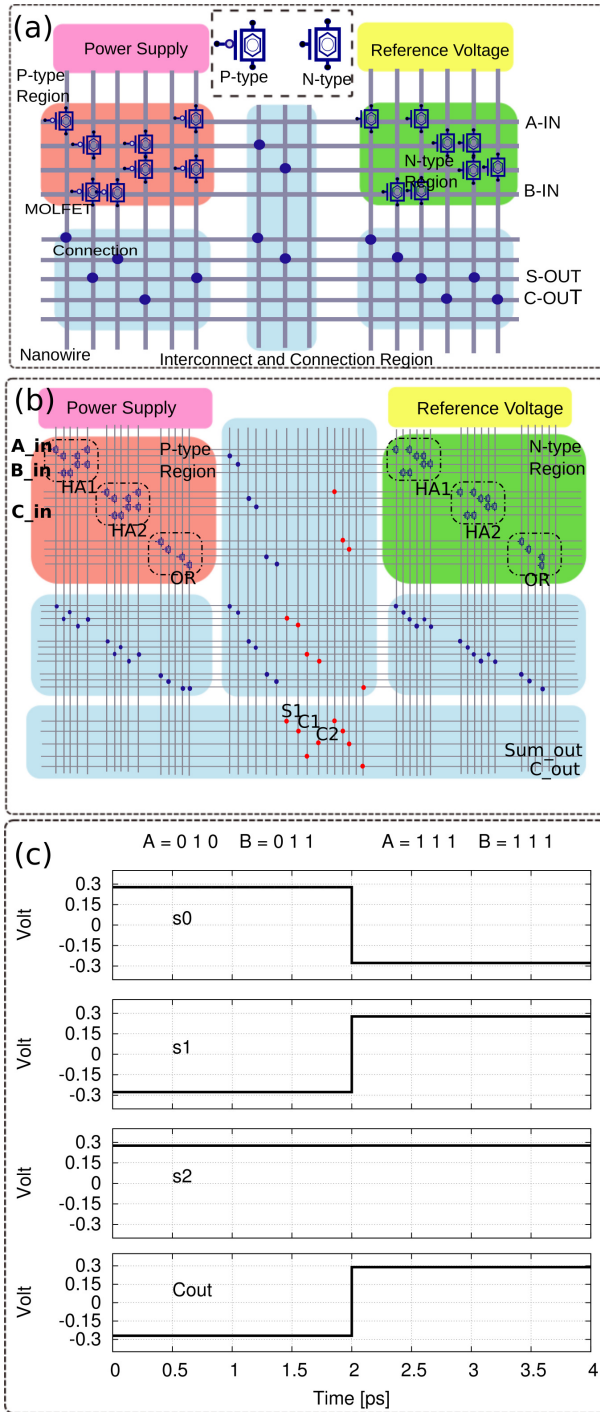
Fig. 5. (a) Crossbar architecture of an Half Adder implemented using complementary logic. (b) Crossbar architecture of a single bit Full Adder, implemented connecting two HA block and an OR gate. (c) Output waveforms of a 3-bit ripple carry adder implemented using complementary logic. In this case, the low input and high input values to encode logic '0' and logic '1' are $-0.3V$ and $1.5V$, respectively.

architectures of the inverter and the HA, it is conceptually possible to design CMOS-like complex circuits organized as chain of this basic block [16].

B. Circuit implementation with complementary MOLFET

Considering both N-type and P-type MTs, we implemented the basic logic gates (inverter, NAND, NOR and HA) with crossbar architectures. We used these gates as building blocks to design and simulate a Full Adder (FA) and then a three bit Ripple Carry Adder (RCA), as a case of study.

We started implementing the Half Adder and the related crossbar architecture is reported in Figure 5(a). In this case, the pink box represents the P-type region and proper connection regions (light blues rectangles) are considered to provide MT interconnections and output signals.

Combining properly HA blocks and OR gates, we firstly designed a single bit Full Adder, whose crossbar architecture is shown in Figure 5(b), and then a 3-bit Ripple Carry Adder.

Regarding the simulations of the 3-bit RCA, the input gate voltage swings from -0.3V (logic '0') to +0.3V (logic '1'). As an example, the output waveforms of SUM (S2-S1-S0) and carry (Cout) for two different input conditions are shown in Figure. 5(c).

IV. CONCLUSIONS

In this work, different logic circuits were simulated in a crossbar like architecture using already existing molecular transistors. Using N-type OPV transistor and saturated methyl chain as molecular resistor, some basic logic circuits are built and their functionality are simulated by using SPICE model of the molecular transistor in VHDL-AMS. To illustrate the feasibility of realizing logic with complementary transistors (both N-type and P-type MTs involved), a 3-bit ripple carry adder is implemented and simulated as case of study. The issues related to the nonlinear behavior of such devices in circuit simulation are discussed and technological aspects to be considered were suggested.

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