A quantitative approach to testing in Quantum dot Cellular Automata: NanoMagnet Logic case

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***Abstract*—With the approaching of CMOS scaling limits the interest on emerging technologies is rapidly growing. Among emerging technologies, Quantum dot Cellular Automata (QCA) is one of the most studied. Particularly the magnetic implementation, NanoMagnet Logic (NML), suffers very low power consumption and it combines logic and memory on a unique device. Despite the advantages of these technologies, QCA and NML working principle relies on the electric or magnetic interaction among neighbor cells, so it is very sensitive to process variations. The behavior of circuits is therefore largely affected by defects and fabrication variations.**

To effectively design circuits with these technologies, proper tools for testing circuits are necessary. In this work we present an innovative test environment for NML technology. The test algorithm is integrated in ToPoliNano, our design and simulation tool for emerging technologies, and it is specifically tailored to support the analysis of faults in large complexity circuits. Thanks to this tool it is possible to design and test complex NML circuits considering the effect of process variations in terms of Yield and Output Error Rate. The approach gives then feedback to the technologists, remarkably helping the future development of this technology. Moreover, notwithstanding the methodology is applied here to NML circuits only, it can also be successfully applied to QCA technology in general, greatly enhancing the value of the work we proposed here.

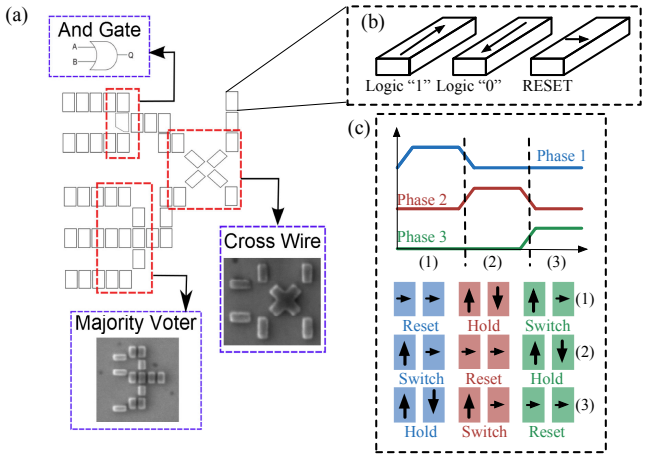

Figure 1: (a) Example of NML circuit layout. The main logic gates are highlighted, a AND, a majority voter [10] and a crosswire, a particular block that allows to cross two wires on the same plane. (b) Nanomagnets logic values. (c) Multiphase clocking scheme used with NML.

I. Introduction

According to the ITRS Roadmap [1], CMOS transistors scaling is reaching its unavoidable physical limits and therefore alternative technologies must be developed. Among these emerging nanotechnologies Quantum dot Cellular Automata (QCA) [2] is one of the most studied. To represent logic values in QCA, different charge configurations stored on identical cells [3] are used instead of voltage levels as it happens in CMOS. Currently, two are the types of QCA implementations that attract most the attention of researchers: Magnetic QCA or NanoMagnet Logic (NML) [4] and Molecular QCA [5] [6] (MQCA). NML technology is interesting for its very low power consumption [7] and the intrinsic memory ability [8], while molecular QCA provides very high clock frequencies and extremely reduced feature sizes [9].

In our work we focus mainly on NML technology, because it is the only QCA implementation which has an extensive experimental validation [11] [12] [7], though attention to faults in MQCA implementation has been recently assured as well [13]. The digital information is represented using single domain magnets with a rectangular shape. If magnets size is sufficiently small they can assume only two possible stable states: "0" and "1" (Fig. 1 (b)) [14] [15]. Signal propagation is obtained placing magnets one nearby the other, exploiting magnetic interaction among neighbor cells. Since the magnetic field generated by a single magnet in not sufficient to alter the state of its neighbor, a clocking mechanism must be used [16]. This field forces magnets in an unstable state ("RESET" case, see Fig. 1 (b)). When the magnetic field is removed, magnets realign themselves following the input element in an anti-ferromagnetic sequence. Due to the influence of thermal noise the maximum number of magnets that can be cascaded without incurring in errors during the signals propagation is limited [17]. In order to design real magnetic circuits a multiphase clock system is therefore necessary, as, for example, we proposed in [18]. Circuits are divided in areas (clock zones) made by a limited number of magnets. At every clock zone a different clock signal is applied. The behavior is shown in Fig. 1 (c), where three clock signal are applied to the circuit. Thanks to this mechanism when magnets of a clock zone are switching (SWITCH in Fig. 1 (c)), magnets on the left clock zone are in the HOLD state and act as inputs while magnets on the right clock zone are in the RESET state and have no influence on switching magnets. The sequence of RESET, SWITCH and HOLD phases guarantees a correct signal propagation as can be understood from Fig. 1 (c) observing the temporal sequence (1), (2) and (3). Logic computation is obtained using elementary gates, such as majority voters and cross-wires, depicted in Fig. 1 (a), where an example of gates we fabricated is shown.

Since NML technology is still in the research phase nanomagnets are normally fabricated using electron beam lithography (EBL), but it is possible to achieve the required resolution also with ultra violet optical lithography [19]. The magnetic material is deposited on the substrate through sputtering or evaporation, the magnetic layer is patterned with lithography and then the geometry is obtained through the selective removal of material with an etching process. Regardless of the lithographic technique used, the fabrication process will introduce some variations that may affect the functionality of the final circuit. Possible causes of defects can be: 1) The presence of defects on the substrate, 2) micro-movements of the substrate during the lithography phase, 3) over-exposure or under-exposure in the etching phase or 4) electrons scattering that can cause exposure of the resist outside the desired region. All these variations can alter the relative position of magnets and therefore the magnetic interaction among them, causing possible malfunctioning.

In order to reliably study and evaluate the competitiveness of this technology, it is necessary to design and to examine circuits of a reasonable complexity keeping into account the effects of process variations. The effect of process variations can be evaluated using low level physical simulators, as shown in [10] and [20]. However only small circuits can be analyzed with such simulators due to extreme requirement in terms of computational power. We developed a new algorithm to analyze the faults derived by process variations in complex circuits and we have integrated this algorithm in our design and simulation tool for emerging nanotechnologies, ToPoliNano [21] [22]. The algorithm is based on the results of physical level simulations we already executed and discussed in [20]. It allows the estimation of the effects of faults generated by displacements in the relative magnets position. Both output-error-rate and yield of circuits implemented and simulated in presence of faults are the outcome of the simulations.

Our contribution allows to understand the reliability of NML and to give feedbacks to the technologists for in terms of both qualitative and quantitative directions toward which it is preferable to improve the fabrication process. The work here proposed, then, remarkably helps the future development of this emerging technology.

II. NML Fault Analysis

Since magnetic interaction strongly depends on the distance among neighbor magnets and on their sizes, it is important to better underline how the process variations affect the logical behavior of circuits. The approach we adopted is as follows: 1) starting from an already synthesized, placed an routed NML circuits based on nanomagnets we associate to magnets position a certain variability as discussed in the following and according to information obtained by the technological processes; 2) we run simulations using the algorithm implemented in ToPoliNano for NML enriched with the capability to take into account the new positions and introducing proper criteria and decision mechanisms to define whether the information is correctly propagated or not; 3) we compare the simulation results to defect-free simulation outputs and detect the presence of possible errors. In the following we describe in details this method.

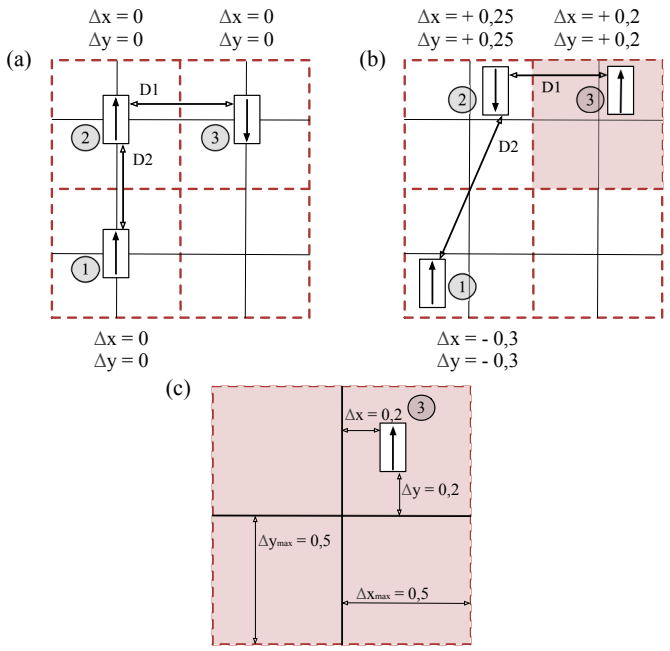

Figure 2: (a) Ideal behavior of a sample circuit, magnets are placed evenly across the plane with regular spacing. (b) Example of circuit affected by process variations; near each quadrant are specified the Δx and Δy shifts. In this non-ideal case the signal is not propagated correctly starting from the second magnet. (c) Zoom of a quadrant in which are marked the maximum allowed shifting values.

In our design approach circuits are seen as matrix in which each node is occupied by a single magnet, in order to obtain very regular structures. We want to evaluate the effect of non-uniform distances among magnets, so we introduced in ToPoliNano the possibility to inject irregularities in the final circuit layout. Fig. 2 (a) shows an example of an ideal NML circuit, where each magnet is evenly spaced among its neighbors. Horizontal and vertical distances are equal to 20 nm according to the technological reference we have [10]. In this ideal case the magnetization of each magnet evaluated with ToPoliNano corresponds to the exact physical behavior.

Fig. 2 (b) and (c) show part of a circuit matrix where magnets are shifted from their original position. Details of the model are represented in Fig. 2 (c) in which the Δx and Δy shifts from the central node are highlighted. The shift values Δx and Δy represent the relative displacements respect to the reference node. The maximum possible shift is the absolute value of 0.5 (both in vertical and in horizontal), this means that each magnet can moves with a displacement of ± 50% w.r.t. the reference coordinate. As an example in the case of Fig. 2 (c) magnets can move within the horizontal coordinates $1,5 < x < 2,5$ and the vertical coordinates $0,5 < y < 1,5$.

Fig. 2 (b) shows different possible combinations of Δx and Δy. For each quadrant containing magnets the relative displacements are reported. Values of $D1$ and $D2$ are different with respect to the previous ideal case (Fig. 2 (a)), in particular $D2$ proves to be higher than the maximum distance achievable for

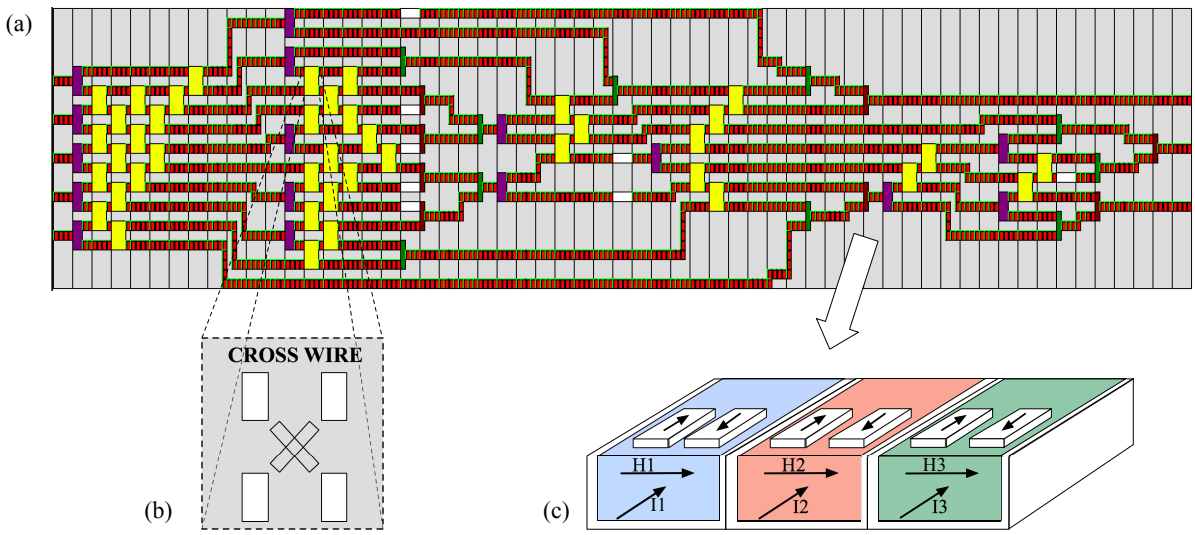

Figure 3: (a) Layout of a 2 bits Ripple Carry Adder in which are highlighted clock zones. (b) Enlargement of a sample block: the CrossWire component is largely employed in NML technology and it is used in order to realize interconnections. (c) Example of clock zone structures: magnets are placed on a wire on propagates information horizontally.

the correct signal propagation. By performing several micromagnetic simulations in [10] [20] we obtained the threshold distance values that guarantee a correct magnetization both horizontally and vertically. Our tool uses this parameters to establish the logic state of each device; thus, in case $D2$ is greater than the threshold value, then the ferromagnetic interaction between magnet 1 and magnet 2 is not correct and an error is generated.

At the time of writing, the two values defining a magnet displacement are loaded by an external file which contains a pair of Δx and Δy randomly generated for each node of the circuit. In an extension of this work we plan to be able to include displacements maps derived by real physical implementations, even though, from a methodological point of view nothing would be changed. Once the position is updated for all the magnets in the circuit, ToPoliNano calculates the magnetization of each magnet according to its simulation algorithm (referring to Fig. 2): I) The logic state of magnet 1 is calculated II) before evaluating the state of the second magnet, D2 must be calculated: if this value is greater than the fixed threshold the final state will be the same of the previous ideal case. Otherwise, if the distance is too high, a probability exists that the information will not be propagated correctly. In this case it is possible to notice from Fig. 2 (b) that vertical ferromagnetic interaction between the first two magnets is not respected. III) The same approach is repeated in order to evaluate the magnetization of the third cell, in this case, since D1 is lower than the fixed threshold the information is propagated correctly, so the antiferromagnetic horizontal interaction happens correctly.
Since displacement values are loaded from an external file, different distributions of distances and their effects on the circuit behavior can be analyzed: thus real data from defects due to fabrication steps associated to specific zones of the circuit can be imported in the analysis.

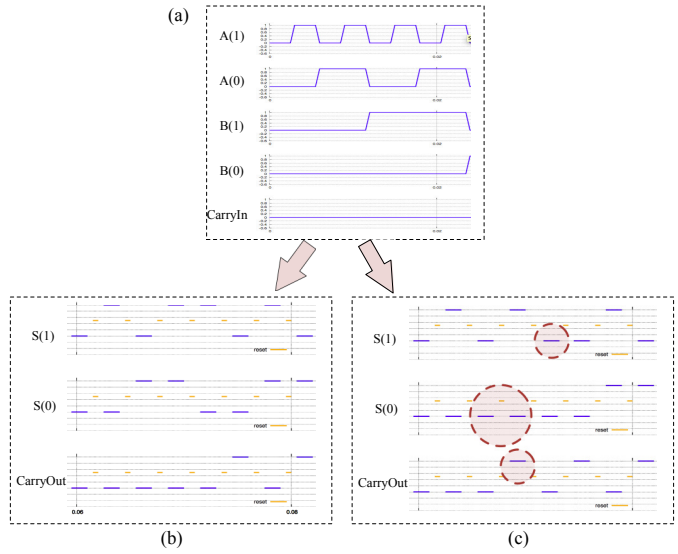

Figure 4: (a) Input signals for the RCA2 circuit. (b) Output signals obtained performing the ideal logic simulation. (c) Output signals obtained performing the logical simulation which takes into account faults derived from process variations.

III. Results

The layout shown in Fig. 3 (a) depicts a two bits Ripple Carry Adder (RCA 2) automatically generated by ToPoliNano, starting from a VHDL description (for a detailed explanation on how this result is achieved refer to [21] [22]). From an architectural point of view the circuit is implemented with few basic blocks. As an example Fig. 3 (b) shows a zoom of the crosswire [12], a particular block that allows to cross

Δx	Δy	$OER_{avg_{1000}}$	*Yield*
± 0.12	0.12	0.8728	0
± 0.1	0.1	0.1364	0.604
± 0.07	0.07	0	1
± 0.05	0.05	0	1
± 0.1	0	0	1
± 0	0.1	0	1
± 0.2	0	0.8703	0
± 0	0.2	0 .8625	0

Table I: Simulation results of Output Error Rate and Yield considering different nanomagnets shift

two wires on the same plane without interferences. Fig. 3 (c) shows the working principle of the clock mechanism: magnets are placed over a wire where a current run through generating the magnetic field. This layout is chosen accordingly to the theoretical and technological constraints related to the fabrication process, which was demonstrated experimentally in [11]. The RCA2 circuit was therefore simulated considering firstly the ideal magnets positions and then taking into account also faults derived from process variations. The obtained waveform in the ideal case is depicted in Fig. 4 (b). The adder was then tested applying the fault analysis algorithm and changing the magnets positions. As an example, Fig. 4 (c) shows that, for example, with an input configuration of A = 11, B = 00, Input Carry = 0 the resulting output is incorrect (S = 10 and Output Carry = 1). The circuit has been tested varying Δx and Δy within different ranges according to Table I. For each combination 1000 iterations were performed exploiting a MonteCarlo-like approach. These results are used to obtain the mean value of Output Error Rate $OER_{Ave_{1000}}$ and the number of fully working circuits (Yield). As an overall consideration, we notice that, with shift values smaller than 0.1, the mean yield is 1. This means that the lithographic process permits to tolerate variations in the magnets position around 10%.

IV. Conclusions

We studied how process variations due to non-uniform spacing between magnets may introduce faults which affect the logical behavior of NML based circuits. We also demonstrate that this analysis can be performed even on complex circuits exploiting our algorithms integrated in the ToPoliNano CAD tool. This work represents a remarkably innovative approach in the study of emerging nanotechnologies since it allows a systematic design and analysis similar to what can be obtained with CMOS technology.

As future works we are extending the analysis to more complex distribution of faults. We will also introduce in ToPoliNano a physical level simulation algorithm based on a simplified version of the LLG equation which rules the micromagnetic dynamics. Thanks to this new algorithm it will be possible to obtain more accurate results without the need to use external computationally intensive low level simulations to evaluate the error probability.

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