A K-band GaAs MMIC Doherty power amplifier for point-to-point microwave backhaul applications

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***Abstract*—This work reports the design of a GaAs monolithic K-band Doherty power amplifier for point-to-point microwave backhaul applications. The design of the module is described, from the choice of the architecture based on power budget and gain requirements, to the analysis of the solutions adopted. The MMIC is expected to achieve 32.5 dBm output power in the 20.8-24 GHz band, PAE higher than 32% at saturation (20% at 6 dB output back-off) and gain higher than 10 dB.**

***Index Terms*—Doherty power amplifiers, Gallium arsenide, K-band, microwave backhaul, MMICs.**

I. Introduction

Microwave point-to-point connections cover half of the backhaul deployments worldwide. The trend is to increase the working frequency, for capacity improvement and apparatus size reduction: frequency bands span nowadays the entire microwave frequency spectrum from 7 to 42 GHz [1], [2]. The increasing usage of high peak-to-average modulated signals asks for advanced solutions to enhance the average Power Added Efficiency (PAE) of the power amplifier (PA).

To this aim, the present work explores the Doherty scheme as an alternative to conventional class AB PAs for K-band (20.8 to 24 GHz) microwave backhaul. A GaAs MMIC Doherty Power Amplifier (DPA) with gain higher than 10 dB and 32.5 dBm of output power is presented. The design is based on the 0.15-μm PWR pHEMT MMIC process of TriQuint Semiconductors [3]. This is one of the first examples of K-band DPAs [4], [5] and implements in GaAs a complex driver architecture able to increase the inherent low gain of DPAs. This cell is conceived as the building block of a 4-way combined PA, able to reach the 4 W output power typically required by commercial products for backhaul.

II. Design

A. Power combining architecture

Reaching the 4 W (36 dBm) output power target, at an assumed 3 dB compression, with GaAs technology requires combining several devices. An estimated 2 dB loss in the output combining networks yields a required output power of 38 dBm at the drain plane. To minimize the layout complexity, the final PA will combine eight $12\times85\,\mu$m pHEMTs, each of them delivering 29 dBm. A foundry non-linear model is available for this device size. The relatively large bandwidth (20.8-24 GHz) imposes accurate design of the matching networks together with careful selection of the architecture.

Fig. 1 illustrates the possible configuration choices for combining 8 power devices in a DPA. Option (a) relies on a single DPA, where the main and auxiliary stages are composed by 4 devices; option (b) combines 2 DPAs, where each main/auxiliary is composed by 2 devices; in (c), 4 small DPAs are combined, and each main/auxiliary stage has a single power device. The latter option, exploited in this work, allows to design, test, and optimize the single-cell building-block DPA. Moreover, each DPA will work on a higher impedance with respect to the other options, thus helping to improve the matching bandwidth. On the other hand, options (a) and (b) present advantages in terms of routing and compactness.

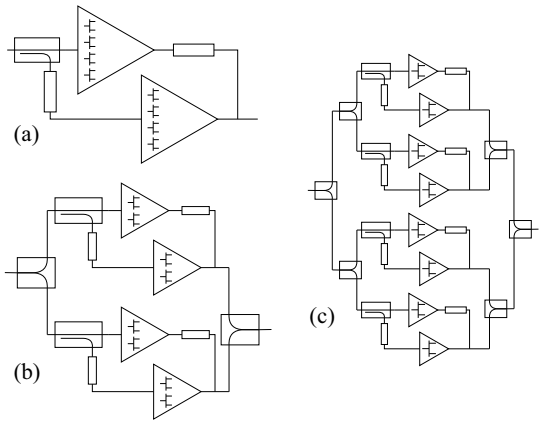

Fig. 1. Possible architectures for DPA power combining.

B. Doherty gain enhancement

From preliminary simulations, the power gain of a single stage DPA using the $12\times85\,\mu$m pHEMT is limited to 5-6 dB, with 31% PAE at 6 dB back-off. To overcome this problem, we included a driver stage in the architecture. We focused on the two "driver strategies" of Fig. 2, comparing them in terms of performance and complexity. While both strategies give the same advantages in terms of gain, the resulting PAE can be different. Fig. 3 shows a comparison of the two strategiest: the total PAE is evaluated starting from the simulated values of gain and PAE of the $12\times85\,\mu$m pHEMT and of the single stage DPA at back-off. At same driver efficiency (x-axis in Fig. 3), solution (b) always offers a higher PAE, for every considered driver gain (different coloured curves in Fig. 3).

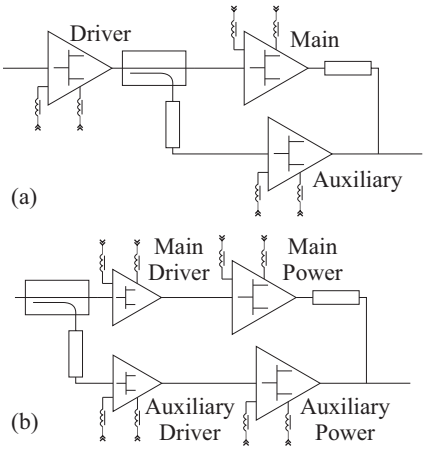

Fig. 2. Comparison between driver strategies for DPA.

Also, if we consider as a target the reference PAE obtained by the non-driven DPA at 6 dB back-off (purple solid line in Fig. 3), solution (b) is advantageous, because the driver efficiency specifications can be relaxed.

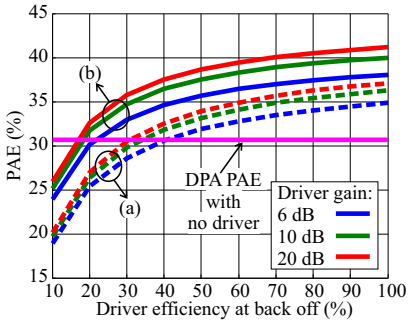

Fig. 3. Total PAE of DPA with driver vs. driver efficiency, for different driver gain. Strategy (a): dashed lines. Strategy (b): solid lines. Ideal DPA PAE without driver: solid purple line.

Moreover, in the scheme of Fig. 2(b), the auxiliary power device can be biased in class B/AB, improving the DPA behaviour in terms of output power and linearity, while the auxiliary driver is biased in class C for the correct turning-on of the branch [6]. The drawbacks of solution (b) are related to the complex structure and the large number of different bias voltages. An $8\times50\,\mu$m device has been chosen for the driver amplifier, since it is able to deliver, before compression, the input power needed to fully drive the $12\times85\,\mu$m power device.

C. Matching strategy

The power device intrinsic drain optimal load, extracted from simulated load-pull on the non-linear model, resulted in $R_{\rm opt} = 20\,\Omega$, a value adopted also as the characteristic impedance of the Doherty impedance inverter Z_0. The common load $Z_{\rm L} = 10\,\Omega$ requires a final output matching to reach the external $50\,\Omega$. To design the output matching networks, the output equivalent circuit has been approximated in the operative frequency band by the network shown in Fig. 4, extracted from load-pull analysis.

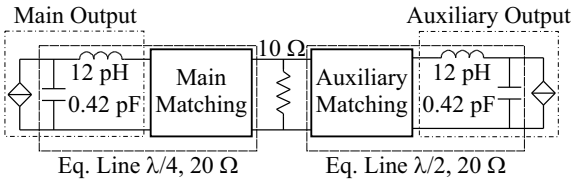

Fig. 4. Output equivalent reactive network of the $12\times85\,\mu$m device and DPA output matching strategy.

The device output capacitance of the main device has been absorbed in the impedance inverter (see Fig. 4). No explicit harmonic control has been inserted, but the second harmonic termination has been monitored to avoid detrimental effects on the efficiency. The auxiliary output network has been designed to provide power matching at saturation and to maximize the impedance seen from the output port when the device is turned off (i.e. $S_{22} \simeq 1$). Simple compensation of the device output capacitance with an inductive stub is not compatible with bandwidth constraints. Thus, the matching network, that absorbs the output capacitance, has been realized as a $\lambda/2$ $20\,\Omega$ equivalent line (see Fig. 4).

The interstage matching networks topology has been designed adopting a simplified procedure. The input of the power device and the output of the driver device have been represented, in the band of interest, by linear equivalent circuits extracted from simulated load-pull, as reported in Fig. 5. The matching has been realized according to [7], see Fig. 6.

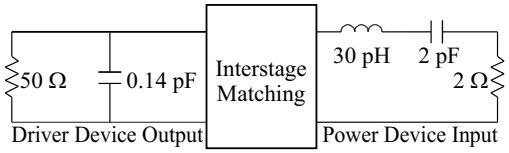

Fig. 5. Equivalent circuits adopted for interstage matching design.

Regarding the input of the power device, the equivalent circuit elements strongly depend on the bias point and output power level. To preserve symmetry the same equivalent circuit is adopted for main and auxiliary sections, thus leading to advantages in terms of stability and robustness. The input matching network has been designed considering the large-signal input reflection of the driver device for a class AB and C bias. The networks implementation at layout level has been

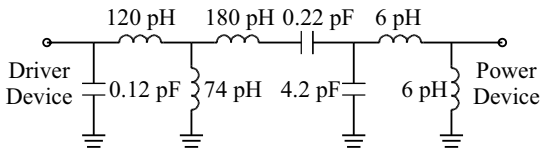

Fig. 6. Interstage matching network: lumped equivalent circuit.

carried out first by substituting the capacitances with library MIM capacitors, then replacing the inductances with short transmission lines, finally tuning length and width to optimize the frequency response. The input branch-line divider has been

designed in a semi-lumped form with each branch realized as a capacitive-loaded transmission line.

D. Stability, robustness, EM simulations

Broadband loop stability has been analyzed adopting linear models at suitable bias points, accounting for the device self-biasing in nonlinear operation. Crucial device parameters have been swept to evaluate the effect of process deviations and model inaccuracies. Pad/bond-wires/external bias-tee models have been added to simulate low-frequency behaviour. The power stages evidenced two critical frequency bands around 7-8 GHz and 0.8-1 GHz. A solution has been found properly dimensioning the drain stub lengths and inserting, at gate and drain DC by-pass, a shunt resistor with a DC-block to ground. For the driver stages, sufficient stability margin is reached with a series resistor on the gate, before the by-pass capacitor.

Regarding robustness to process variations, Monte Carlo simulations of the building blocks and of the DPA have been carried out. To minimize dispersion, it has been important to maintain symmetry, employing identical structures for the main and auxiliary stages. This solution ensures a really improved robustness and better average performances, even if it doesn't optimize the DPA behaviour in the nominal case.

Electro-Magnetic (EM) simulations have been extensively employed, in particular for the design of the output combiner, where the coupling at the junction of the main and auxiliary branches has to be carefully assessed.

III. Performance Evaluation

The MMIC layout of the single cell DPA now under fabrication is shown in Fig. 7.

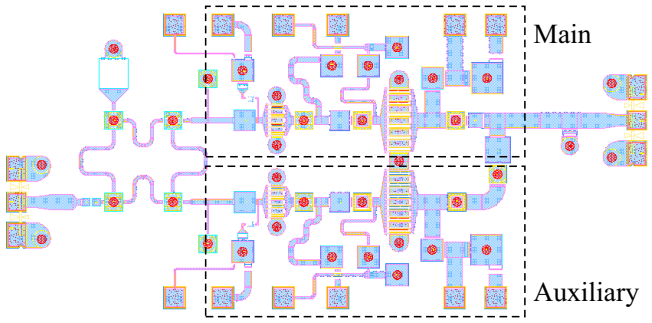

Fig. 7. Layout of the MMIC DPA. Mask area is $3000 \times 1430\,\mu\text{m}^2$.

The devices are biased at 6 V drain voltage; in the main branch, the bias current is 20 mA for the driver and 100 mA for the power device; in the auxiliary branch, power device is biased with 30 mA while the driver is in class C, with -1.9 V gate voltage. The small signal gain resulted almost flat around 10.5 dB in the entire band 20.8-24 GHz (Fig. 8, right), thanks to input mismatch at low frequency (Fig. 8, left). We expect that the insertion loss will improve over the entire bandwidth with the adoption of Lange couplers for DPA combination.

Harmonic balance simulations have been carried in CW and in the band 20.8-24 GHz. The DPA provides around 32.5 dBm

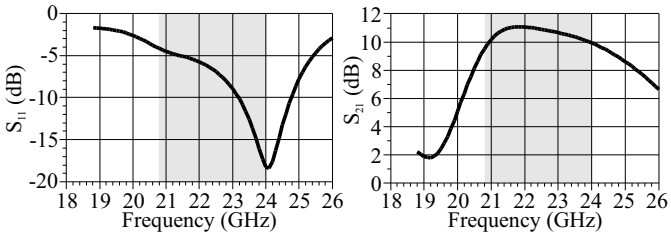

Fig. 8. Small signal simulations of the realized MMIC. S_{11}: left; S_{21}: right.

of output power on the design band, and can be used as a building block of the combined structure of Sec. 1 for the final 4 W module. The power gain as a function of the frequency is shown in Fig. 9 left and the PAE in Fig. 9 right. For the same bias point in the entire band, the power gain ripple stays lower than 1.5 dB (9.5-11 dB), with a corresponding PAE higher than 32% at saturation (20% at 6 dB output back-off).

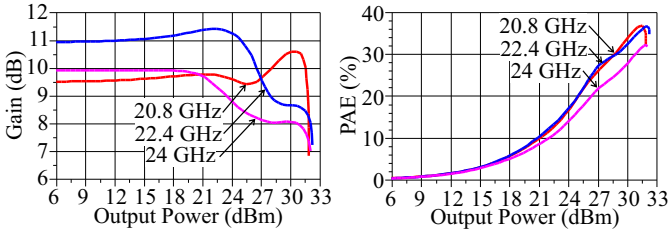

Fig. 9. Single tone simulations of the realized MMIC. Gain: left; PAE: right.

Performance optimization can be further achieved by tuning the gate bias for a specific frequency sub-band.

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