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Compact Parameterized Macromodels for Signal and Power Integrity analysis of RF and Mixed Signal Systems

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Abstract—Linear macromodeling techniques are well established for compact dynamical modeling of complex signal and power distribution networks. In this work, we extend applicability of such reduced-order behavioral models to small-signal descriptions of complex circuit blocks typically found in RF or Analog and Mixed/Signal designs. In addition, we include in the models the explicit dependence on one or more design parameters, such as temperature, bias or gain, thus obtaining a multivariate small-signal behavioral macromodeling approach. The main outcome is a major reduction in the runtime required for transient system-level verification, which can be performed directly by simulating the surrogate macromodels rather than full transistor-level circuits. We demonstrate this approach through an Operational Amplifier circuit block of a commercial 3G transceiver design.

I. INTRODUCTION

The system-level verification of signal and power integrity of integrated Radio Frequency (RF) and Analog-Mixed-Signal (AMS) Systems on Chip (SoC) for compact portable electronic applications such as smartphones and tablets is very challenging and time-consuming [1]–[3]. Due to miniaturization and aggressive integration, complex nonlinear circuit blocks coexist in close proximity. Although suitable countermeasures can be taken for the isolation of sensitive analog blocks from noisy digital parts, several parasitic local and global coupling effects may affect the overall system, possibly leading to interference and causing system malfunctioning. Therefore, fast and accurate solutions for system-level simulation under different operation conditions must be performed, in order to qualify the system for signal and power integrity.

In recent years, the so-called “macromodeling” techniques have gained a lot of popularity for fast modeling and simulation of signal and power distribution networks. Such interconnects, being intrinsically linear, are first characterized through their multiport scattering responses in the frequency domain by full-wave electromagnetic solvers. Then, the scattering responses are subjected to curve fitting schemes [4], [5] with passivity constraints [6]–[9], which extract reduced-order behavioral models of the interconnect network in state-space form. The latter is readily synthesized in a SPICE netlist, thus allowing global transient simulation. This process is now standard in commercial tools and in industrial design flows.

The above procedure falls short when nonlinear circuit

blocks or devices are present. Due to their nonlinearity, such elements must be removed from the overall interconnect structure, which is macromodeled separately. The nonlinear devices are then reassembled to the reduced-order interconnect, resulting in a still large nonlinear network, whose numerical simulation remains challenging.

In this work, we consider a special class of nonlinear circuit blocks, namely those subsystems that, although very complex in their internal structure, are intentionally designed to have an almost linear input-output response when suitably biased around a prescribed DC operation point. Examples can be Low Noise Amplifiers (LNA’s), Operational Amplifiers (OPA’s), or programmable active filters in RF transceivers for wireless applications. We show that reduced-complexity small-signal linear macromodels are easily extracted for these subsystems [10], [11], possibly including the effect of external design parameters such as bias voltage, gain (for amplifiers), temperature, etc. As a result, system-level signal and power integrity verification can be achieved through parametric analysis in standard circuit solvers, with an overall runtime that is orders of magnitude less than for the original transistor-level description of the system. The proposed technique is demonstrated on a complex Operational Amplifier (OPA) circuit block from a commercial design.

II. SMALL-SIGNAL MULTIVARIATE BLACK-BOX MACROMODELING

We start with a general description of a large-scale P -port nonlinear circuit described by finite-order state equations

$$\dot{\mathbf{x}}(t; \lambda) = \mathbf{F}(\mathbf{x}(t; \lambda), \mathbf{u}(t; \lambda); \lambda) \quad (1)$$

$$\mathbf{y}(t; \lambda) = \mathbf{G}(\mathbf{x}(t; \lambda), \mathbf{u}(t; \lambda); \lambda) \quad (2)$$

where $\mathbf{u}, \mathbf{y} \in \mathbb{R}^P$ collect input and output variables, respectively, $\mathbf{x} \in \mathbb{R}^N$ collects state variables, and \mathbf{F}, \mathbf{G} are nonlinear multivariate functions, and $\lambda \in \mathbb{R}^\mu$ is a vector collecting μ external parameters.

Assume that small-signal conditions apply, so that

$$\begin{aligned} \mathbf{u}(t) &= \mathbf{U}_0(\lambda) + \tilde{\mathbf{u}}(t), \\ \mathbf{x}(t; \lambda) &= \mathbf{X}_0(\lambda) + \tilde{\mathbf{x}}(t; \lambda), \\ \mathbf{y}(t; \lambda) &= \mathbf{Y}_0(\lambda) + \tilde{\mathbf{y}}(t; \lambda), \end{aligned} \quad (3)$$

where $\{U_0(\lambda), X_0(\lambda), Y_0(\lambda)\}$ represent the constant (bias) input, state and output vectors arising from nominal DC operation, and $\{\tilde{u}(t), \tilde{x}(t; \lambda), \tilde{y}(t; \lambda)\}$ denote small signal variations of input, state, and output around the bias point. Inserting (3) into (1)-(2) and computing a first-order Taylor expansion of the nonlinear maps F, G around the operation point, leads to the following linearized state-space equations

$$\dot{\tilde{x}}(t; \lambda) \approx \tilde{A}(\lambda)\tilde{x}(t; \lambda) + \tilde{B}(\lambda)\tilde{u}(t), \quad (4)$$

$$\tilde{y}(t; \lambda) \approx \tilde{C}(\lambda)\tilde{x}(t; \lambda) + \tilde{D}(\lambda)\tilde{u}(t), \quad (5)$$

where the parameter-dependent state-space matrices $\tilde{A}(\lambda) \in \mathbb{R}^{N \times N}$, $\tilde{B}(\lambda) \in \mathbb{R}^{N \times P}$, $\tilde{C}(\lambda) \in \mathbb{R}^{P \times N}$, $\tilde{D}(\lambda) \in \mathbb{R}^{P \times P}$ collect the partial derivatives of F, G with respect to states and inputs, evaluated at the operation point. System (4)-(5) represents a small-signal linear transfer function model, with small-signal transfer function

$$\tilde{H}(s; \lambda) = \tilde{C}(\lambda)(sI - \tilde{A}(\lambda))^{-1}\tilde{B}(\lambda) + \tilde{D}(\lambda). \quad (6)$$

The number N of states in (4)-(5) can be very large, especially when the model includes the effects of all parasitics due to capacitive, inductive or resistive/substrate couplings. Therefore, some complexity reduction is highly desired before using the model for system-level simulations aimed at functional as well as signal/power integrity verification. In order to obtain such reduced-order model, the full nonlinear circuit block is run within the available CAD environment for a set of discrete frequency/parameter grid points $(\omega_k; \lambda_\nu)$. Then, the resulting multiple sets of frequency- and parameter-dependent scattering data $\tilde{H}(j\omega_k; \lambda_\nu)$ are processed by a parametric rational fitting engine, in order to obtain a low-order rational macromodel which takes the form

$$\dot{\tilde{x}}_q(t; \lambda) \approx \tilde{A}_q(\lambda)\tilde{x}_q(t; \lambda) + \tilde{B}_q(\lambda)\tilde{u}(t), \quad (7)$$

$$\tilde{y}_q(t; \lambda) \approx \tilde{C}_q(\lambda)\tilde{x}_q(t; \lambda) + \tilde{D}_q(\lambda)\tilde{u}(t), \quad (8)$$

with a number of states $q \ll N$, and such that

$$\tilde{H}(s; \lambda) \approx \tilde{H}_q(s; \lambda) = \tilde{C}_q(\lambda)(sI - \tilde{A}_q(\lambda))^{-1}\tilde{B}_q(\lambda) + \tilde{D}_q(\lambda) \quad (9)$$

for $s = j\omega$ and each component $\lambda^{(i)}$ of the parameter vector within user-defined fitting bandwidth $[\omega_{\min}, \omega_{\max}]$ and parameter range $[\lambda_{\min}^{(i)}, \lambda_{\max}^{(i)}]$. The macromodel is obtained by a number of steps, itemized below.

1) *Model structure and fitting*: We consider the following representation [12], [13] for the parameterized small-signal macromodel

$$\tilde{H}_q(s; \lambda) = \frac{\mathbf{N}_q(s, \lambda)}{d_q(s, \lambda)} = \frac{\sum_{m=0}^q \mathbf{R}_m(\lambda)\phi_m(s)}{\sum_{m=0}^q r_m(\lambda)\phi_m(s)} \quad (10)$$

where the frequency-dependent basis functions are partial fractions associated to a set of distinct prescribed poles a_m

$$\phi_0(s) = 1, \quad \phi_m(s) = \frac{1}{s - a_m} \quad (11)$$

and where the parameter-dependent coefficients are expressed as a superposition of multivariate basis functions $\xi_\ell(\lambda)$ as

$$\mathbf{R}_m(\lambda) = \sum_{\ell=1}^L \mathbf{R}_{m,\ell} \xi_\ell(\lambda), \quad r_m(\lambda) = \sum_{\ell=1}^L r_{m,\ell} \xi_\ell(\lambda) \quad (12)$$

with constant and unknown coefficients $\mathbf{R}_{m,\ell}$ and $r_{m,\ell}$. In this work, we use entire-domain multivariate polynomials as $\xi_\ell(\lambda)$, which are sufficient due to the low order that is required for our application. The coefficients in (10) are identified by performing a weighted least-squares fit of the data $\tilde{H}(j\omega_k; \lambda_\nu)$ within a Sanathanan-Koerner framework. More details about this process are found in [12], [13], [17], where it is also shown how to construct the state-space realization (9).

2) *Parameterized DC correction*: The above macromodel is almost ready for system-level simulation. In fact, a brute-force replacement of the nonlinear state equations (1)-(2) with the macromodel (7)-(8) will not lead to correct results, since the latter captures only small-signal variations and lacks information on the operation point. This is readily seen by computing the DC response of the macromodel under nominal bias conditions,

$$\mathbf{Y}_{q,0}(\lambda) = \left(\tilde{D}_q(\lambda) - \tilde{C}_q(\lambda)\tilde{A}_q^{-1}(\lambda)\tilde{B}_q(\lambda) \right) \mathbf{U}_0(\lambda) \quad (13)$$

which in general is not equal to the correct DC output $\mathbf{Y}_0(\lambda)$. A correct implementation is obtained by complementing the macromodel realization with suitable constant correction sources defined as

$$\Delta \mathbf{Y}_{q,0}(\lambda) = \mathbf{Y}_0(\lambda) - \mathbf{Y}_{q,0}(\lambda), \quad (14)$$

to be connected at the interface ports of the macromodel [11]. The actual values of these sources are obtained by evaluating (14) for each value of the parameter grid points λ_ν , and by interpolating/fitting these values with a low order polynomials using the basis functions $\xi_\ell(\lambda)$ of (12). A SPICE implementation is straightforward through polynomial controlled sources, a basic component that is available for practically all SPICE engines.

3) *Discussion*: The proposed macromodel is equivalent to standard small-signal analyses available in any circuit solver, but with the added value of intrinsic model order reduction. The full-size small-signal circuit with N states is replaced by its macromodel having only $q \ll N$ states. The main ‘‘order reduction’’ approach that we use is based on black-box curve fitting with external parameters. This technique has already been discussed in [12]–[16] for modeling of linear structures only. This paper extends this technique proving its applicability to biased nonlinear circuit blocks, provided that proper care is taken in the enforcement of the (parameter-dependent) DC macromodel behavior.

III. RESULTS

The proposed macromodeling procedure is illustrated on a circuit block composed by a single OPERational Amplifier whose voltage source is provided by a Low-DropOut (LDO) voltage regulator, see Fig. 1. Both components were extracted

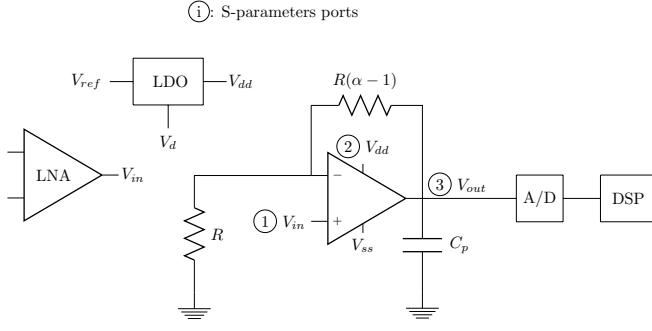


Fig. 1. Subset of high-level circuit blocks inside a base-band receiver chain.

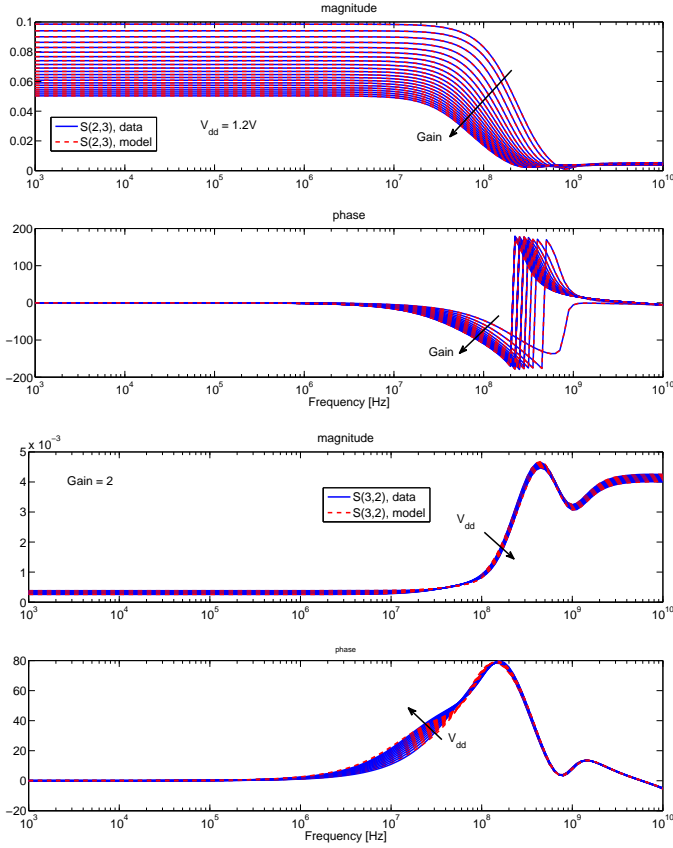


Fig. 2. Top: comparison between parameterized macromodel (red dashed lines) and small-signal S-parameter $S_{2,3}$ responses of the OPA circuit block for fixed supply voltage $V_{dd} = 1.2$ V and variable gain. Bottom, same comparison but for $S_{3,2}$ with fixed gain $\alpha = 2$ and variable V_{dd} .

from a commercial 3G transceiver design. The OPA circuit block is parameterized by a supply voltage $V_{dd} \in [1.1, 1.3]$ V with 20 mV steps and a gain $\alpha \in [1, 2]$ with steps 0.05, which are ranges of practical interest. Linearity and closed-loop stability were verified in practice by means of Spice simulations. The LDO model is parameterized by a $V_d \in [1.2, 1.7]$ V using a nominal voltage reference $V_{ref} = 0.6$ V, see also [18].

Figures 2-3 compare the computed macromodel responses to the original small-signal scattering responses for various

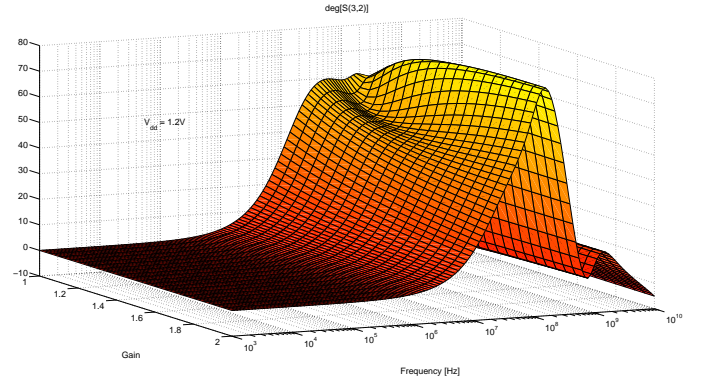


Fig. 3. Illustration of the variability of a sample scattering response $S_{3,2}$ (phase) of the parameterized OPA macromodel with respect to gain.

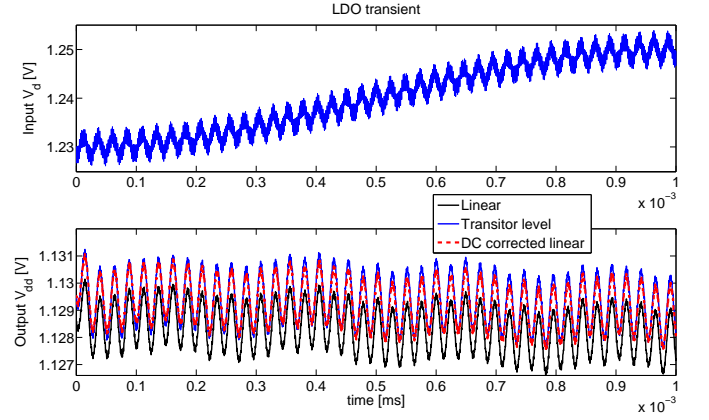


Fig. 4. Bottom panel: detail of the transient analysis of the LDO transistor-level circuit block (blue continuous line) and parameterized macromodel, with (red dashed line) and without (black line) DC correction sources. The LDO input affected by noise is depicted in the top panel. As expected, the output from the LDO is always close to the nominal value of 1.13 V.

combinations of the parameters. The accuracy is excellent. These figures show that the variability induced by supply voltage variations is very small, whereas the sensitivity to a gain variation is larger.

The same macromodeling process was also applied to the LDO (not shown here). Then, the parameterized macromodels of OPA and LDO were synthesized in SPICE, and a transient analysis was performed to validate the macromodel vs the full transistor level circuits. For illustration, we address a common signal-integrity scenario: the output from a differential LNA in a base-band receiver chain is amplified and filtered using an OPA. Signal quality and noise rejection are of paramount importance since the analog output from the OPA is then processed by an A/D converter and provided to a Digital Processing Block. Disturbances on the voltage input V_d , due to cross-talk or external noise sources must be handled by the LDO resulting in a stable V_{dd} for the OPA. Therefore a multi-tone (1 GHz–567 MHz–40MHz) multi-amplitude distortion is added to a 10 kHz square wave used as disturbance on the V_d input of the LDO, while the input for the OPA is a 4 MHz

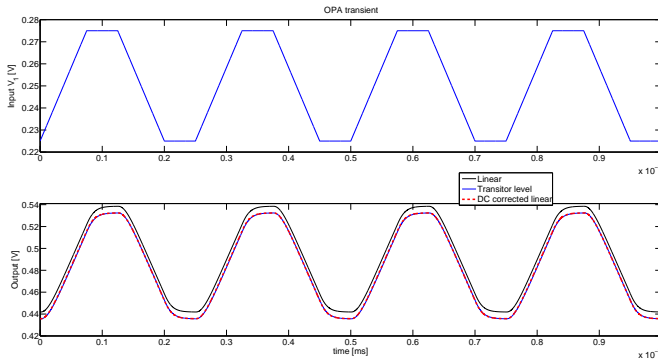


Fig. 5. Bottom panel: detail of the transient analysis of the OPA transistor-level circuit block (blue continuous line) and parameterized macromodel, with (red dashed line) and without (black line) DC correction sources.

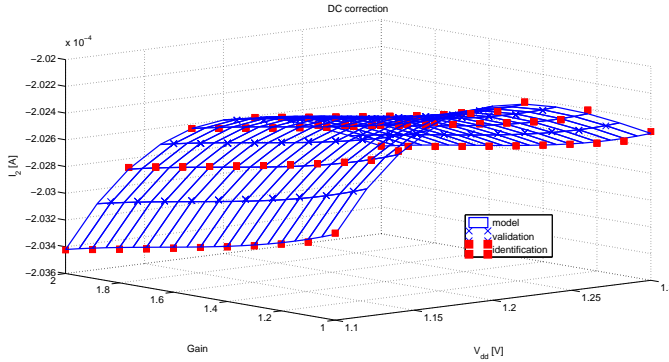


Fig. 6. OPA current correction source I_2 depicted as a function of V_{dd} and gain α . The 2D polynomial model (blue continuous line grid, degree 4 in both variables) attains a RMS error of 10^{-5} .

square wave.

A small part of the input signal and the corresponding outputs are depicted in Fig. 5 for the OPA and in Fig. 4 for the LDO. A 200 μ s transient simulation is required in order to properly assess the effect of the disturbances on the LDO input V_d . The transistor level simulation required 10 h. Such large simulation time is quite common and basically due to: the complexity of the transistor level models, involving 600 transistors, 100 diodes and 600 dynamical elements, and the complexity of the multi-tone disturbance on the LDO. The linear macromodel completed the simulation in only 8 minutes leveraging on the synthesized low order model: order 11 for the OPA and 16 for the LDO. As can be seen in Figures 4 and 5, such a tremendous speedup can be achieved with no compromise on accuracy. The figures further demonstrate the necessity of including DC correction sources, since the results without such sources present a clear DC offset. Dealing with two parameters, i.e. V_{dd} and α , the DC correction current sources were modeled using two-dimensional polynomials; results are depicted in Figure 6.

IV. CONCLUSIONS

In summary, we have presented a parameterized macromodeling procedure that is able to produce accurate and efficient

small-signal macromodels of nonlinear circuit blocks that are designed to operate linearly under specific bias conditions. The obtained macromodels provide an implicit model order reduction, thus reducing transient simulation runtime. Therefore, such macromodels can be used as elementary building blocks, replacing the actual design schematics, and suitably combined with signal and power distribution network reduced models within a full system-level simulation, leading to a drastic reduction in overall runtime.

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