Compact Model for Multiple Independent Gates Ambipolar Devices

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Compact Model for Multiple Independent Gates
Ambipolar Devices
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Motivation: Ambipolarity is often suppressed by processing steps; It can be exploited to enhance logic functionality. Natural evolution of FinFET
Novel approach is needed to tackle complex structures

Multiple Gates vs Multi-Gates
In this context, Multiple Gates ≠ Multi-Gate
GAA are Multi-Gate devices, but do not necessarily feature MultiGates.
Present work is about Multiple Independent Multi-Gate devices.
Nanoarray-based structures can benefit, as well, of this approach.

The approach: a collective strategy.
Device is seen as composed by a series of Sections.
How to decompose it:
Define appropriate sections (S_i) in the overall structure.
Sections need not feature the same parameter set
The study of the complete device is reduced to the study of simpler parts.

Device section modeling

I_{th} can be calculated independently in each Section S_i provided we know V_{th} and V_{os} of all sections: V_{os} = V_{th} + I_{ds} / L_{ds}
Potential charge density
Charge density current

The method

\[ I_{d1} = \frac{2e^{-L_{ox}q\phi_{bs}}}{q} \int_{V_{th}}^{V_{os}} q(V) dV \]

Q_{QI} and Q_{Q2} are linked with V_{s} and V_{os} through the charge control equation:

\[ V_{s} = \int V_{os} dV - \int V_{th} dV = \frac{Q_{Q1} + Q_{Q2}}{2 \varepsilon_{ox} L_{ox}} \]

Q_{Q1} and Q_{Q2} can be neglected in calculating

\[ I_{d1} = \frac{2e^{-L_{ox}q\phi_{bs}}}{q} \int_{V_{th}}^{V_{os}} q(V) dV \]

V_{s} can be calculated substituting Q_{QI} in the charge control equation:

\[ V_{s} = \int V_{os} dV - \int V_{th} dV = \frac{Q_{Q1} + Q_{Q2}}{2 \varepsilon_{ox} L_{ox}} \]

Knowing Q_{Q1} it is possible to calculate the current:

\[ I_{d1} = \frac{2e^{-L_{ox}q\phi_{bs}}}{q} \int_{V_{th}}^{V_{os}} q(V) dV \]

V_{s} can now be calculated through the charge control equation:

\[ V_{s} = \int V_{os} dV - \int V_{th} dV = \frac{Q_{Q1} + Q_{Q2}}{2 \varepsilon_{ox} L_{ox}} \]

If requirements are not met it is possible to iterate the process. As a rule of thumb, the more the gates, the more iterations.
Up to three gates one iteration is enough, as will be shown in the results section. Else the process ends.

Single section modeling

Charge-based model is used at Single Section level to obtain current information . Drain current calculated as:

\[ I_{ds} = \frac{2 \pi R^2}{L} \int_{V_{th}}^{V_{os}} q(V) dV \]

Extensions

Same nature of the problem, same approach, slight modifications.

Gateless section

\[ V_{i} = V_{t1} - R \frac{dV}{dt} \]

\[ Q_{Q} = Q_{o} \]

Doped channel

\[ \delta = \frac{V_{th}}{V_{os}} \delta_{V_{th}} \]

\[ V_{os} - \frac{K_{t1}}{K_{n1}} \frac{dV}{dt} = \frac{K_{t1}}{K_{n1}} \frac{V_{os} - \frac{K_{t1}}{K_{n1}} \frac{dV}{dt}}{V_{th}} \]

\[ V_{i} = V_{o} = V_{th} - R \frac{dV}{dt} \]

Arbitrary Num. of gates

Q_{Q} can be determined as positive root of:

\[ Q_{Q} = \frac{K_{t1}K_{t2}}{K_{n1}K_{n2}} \left( \frac{V_{os} - \frac{K_{t2}}{K_{n2}} \frac{dV}{dt}}{V_{th}} - 1 \right)^{2} + \frac{dV}{dt} \log \left( \frac{Q_{Q1} + Q_{Q2}}{Q_{Q1}} \right) \]

Validation

Theoretical: numerical simulations: TCAD (Silvaco Atlas)
Experimental: at this stage of development, we still did not perform this kind of verification.

Conclusions

Fast (second vs. hours) and accurate (max err negligible) simulation.

Results: single section

Results: double section

Results: triple section, one gateless

Results: triple section

\[ L_{1}, L_{2}, L_{3} \] (different length of the sections)

\[ V_{G1}, V_{G2}, V_{G3} \] (different applied voltages to the gates)

R (radius of the nanowire) tox (oxide thickness)

I_{th} independently calculated in sections S exploiting a charge-based model.

Hypothesis: no voltage drop at Si and S_{i+1} contacts.