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***Abstract*—The interesting expectations on nanoarray based circuits are counterbalanced by critical issues related to reliability. Nanowires and active devices currently cannot rely on a mature technology and high rates of defects are still to be expected. Our approach to evaluate the effects on nanoarray based circuits behavior consists in simulating at switch level the precise behavior of the circuit considering a statistical distribution of faults throughout the tile area. We are able to reckon the output error rate of nanoarray circuits as a function of defective rates and defect distribution giving to both technologists and architects directions to find possible solutions.**

I. Introduction

The trend of scaling the critical dimension of CMOS has started to show its limits, both from physical and economical point of view. Nanoscaled array based technologies are, among the emerging technologies, one of the possible CMOS next substitute. Literature scenario shows a large number of nano-structures proposal, one of these is based on nanowire arrays [1] organized in matrices called tiles. In such a structure the circuit is represented through blocks connected together. Each block is composed by a grid of Nano Wires or Carbon Nano Tubes. Moreover, crosspoints are called sub-tiles and they can be programmed with FET, diodes or can be disconnected.
As mentioned before, circuits based on nanarrays allow for denser designs with respect to conventional CMOS technology, however defect rates due to nanoscale manufacturing are the main concern.
Most of the existing techniques, developed for CMOS technologies and used to deal with defect-tolerance problems cannot be applied on nanoscale circuits These techniques are not aimed to be employed with very high defect rates. Moreover, the proposed solutions require complex and aperiodic structures within circuits and this is not achievable with very regular structures such as nanoarray architectures. From literature it is known that fault sources can be classified into three main groups: permanent faults, transient faults and process variations.
The aim of the work presented in this paper is to analyze the main sources of permanent faults and to present a new approach to overcome them.

II. Faults analysis method

The two main fault can be identified in: I) Disconnected crosspoints instead of active devices and II) Broken nanowires. In these cases we can assume that no information can be further propagated. Different approaches can be used in order to solve the problem of defect-tolerance, many of these techniques are based on reconfigurability principle; in this case once faults are located it is necessary to be able to access every node of the circuit in order to reprogram it.
It is widely recognized that in order to allow this, circuit

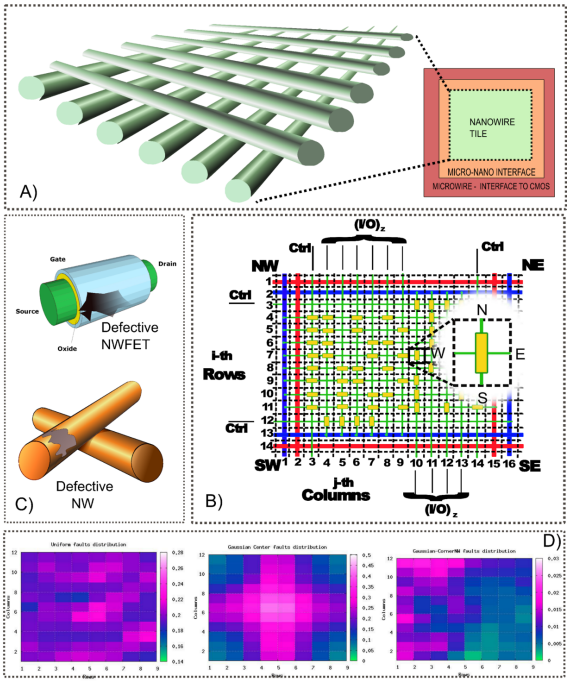

Fig. 1. A) Nanowire array general structure; B) Detailed example of a NASIC Full Adder; C) Details of a NWFET and of a WIRE with defects; D) Maps of defects distribution (Uniform on the left, Gaussian in the center, Gaussian corner in the right).

interface must be very complex and the effective device density should be downgraded. For these reasons we choose to investigate a completely different approach based on the insertion of structural redundancies.
In order to provide an effective assessment of the circuit's yield, we can separate the contributions of the internal signals $P_{(I/O)_z}$ (where z is the index of the I/O lines) from the contributions of the control signals P_{CTRL}. Considering a uniform probability of faults we can express the yield as $Y = \left[1 - \left(\prod_z P_{I/O_z}\right) P_{CTRL}\right]$ [3]. Since it would be difficult to analytically express these terms, also considering this simplification, we decided to develop our simulation tool exploiting the Monte Carlo simulation approach. In this way a large number of input patterns is generated in order to test different defect probabilities distributions.
The simulator can handle different kind of distributions; starting from this, a fault map can be generated for each tile of the circuit. These maps were represented in matrix form in which each node constitutes a sub-tile of the circuit. In such a way users can decide to load defect maps and the simulator checks in each node of the circuit if the information can be

propagated or not. This approach makes it possible to evaluate the impact of high error rates.

III. RESULTS

Our multilevel simulator has been developed in C++, with the support of a custom XML-based language for all input and configuration information, and of Perl scripting for faults sets generation. The whole software is compatible with different operating systems: Linux, UNIX, Mac OS X and Windows are currently supported.

The simulator has been tested for faults with few logic functions based on NASIC fabric [4]. In particular we used a NAND-NAND nanoarray structure. In this paper we report the impact of defects for the two inputs AND port and for a 1-bit Full Adder (FA).

The impact of defects previously described is based on a set of files which include fault information statistically generated in a Monte Carlo style (5000 trials for each faults set). During the assembly process NWs could break along their axes, so defects could have a not uniform distribution along the wire. We carried out multiple simulations to show the impact on the output error rate of different fault distributions in both wires and devices. In each simulation step we used both Uniform (U) and Gaussian (G) distributions on the plane. In the latter case the peak of the distribution can be positioned where necessary to better describe the real defects occurrences due to fabrication processes. Here we consider a centered Gaussian (G-Ct) and a corner case (G-Cn) in the four different corners (NE, NW, SE, SW).

Figure 2.top shows the output error rate for the AND port due to faults distributed along both horizontal and vertical NWs. The graph shows an increase of the output error rate as a function of nanowire defect rate. The slope of the linear curve is unexpectedly high: 2% of nanowire defects causes a $\approx 30\%$ output error rate, whilst 10% causes a $\approx 40\%$ to $\approx 50\%$ as output error. These results are dependent on the distribution type. In particular the G-Cn-NE and G-Cn-NW are the worst case, due to the presence in those zones of direct connections to input signals.

The output error rate for a 1-bit Full Adder (FA) under the same condition is shown in Figure 2.center. A similar trend is observed in this graph, but with a lower ratio ($\approx 5\%$ for 2% nanowire defects) at the lowest values of defect rate. However, even if both graphs start at a quite different output error rates for low defect rates, both FA and the AND port reach a $\approx 70\%$ of output error rate for a 20% nanowire defect rate in the worst case. When both nanowire and device defects are taken into account, Figure 2.bottom, the different behavior of the AND port and FA is more evident. The impact of device error rate is lower compared with nanowire defects which affect larger parts of the circuit. The difference between the AND port and FA relies on the fact that the AND port is smaller and denser with respect the FA circuit.

Hence, it is very important to have a simulator which performs a fine grade analysis the behavior of the circuit at sub-tile level, in order to extract information useful for all the design phases. Given a fault-rate there is a notable difference in the output error rate of the behavior depending on the actual distribution of the faults in the structure. Therefore, the tool helps designers to evaluate the distribution of faults, very precisely, for whatever such distribution since it is very difficult do find it analytically. In this way, we can evaluate the effectiveness of fault tolerant techniques proposed in literature.

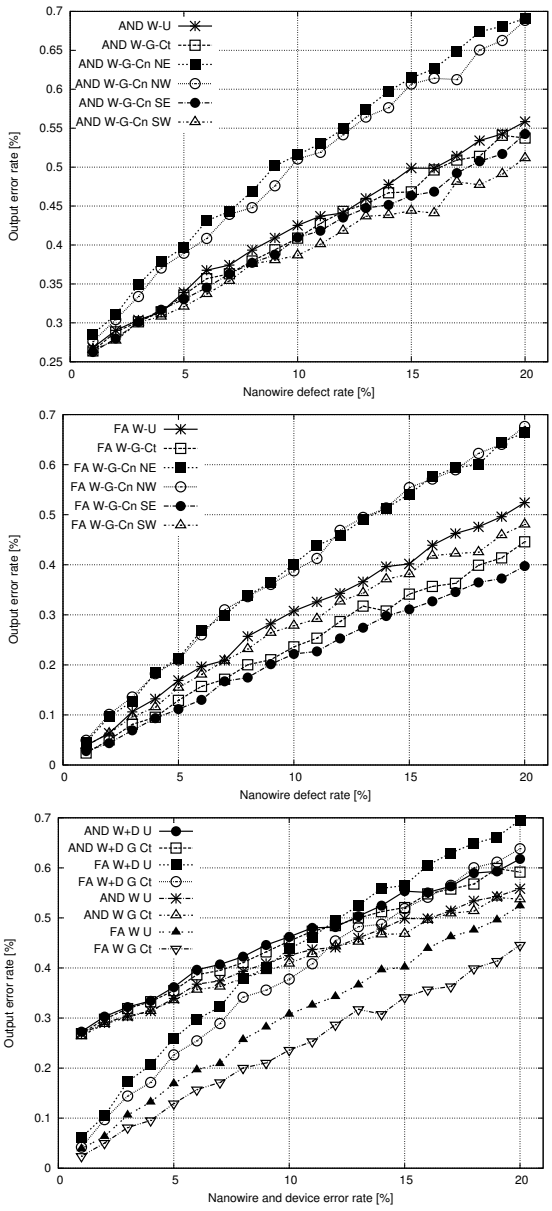

Fig. 2. Output error rate for AND port (top), Full Adder (center) as a function of nanowire defect rate and for both AND port and FA (bottom) when device and nanowire faults are superposed

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