Prediction of Stochastic Eye Diagrams via IC Equivalents and Lagrange Polynomials

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ABSTRACT

This paper addresses the prediction of eye diagrams in high-speed data links with the inclusion of manufacturing tolerances. The statistical assessment of the system performance is done via the combined application of accurate and efficient IC models and of the stochastic collocation method with Lagrange interpolating polynomials. Numerical results on the computation of the eye opening profile for a realistic PCB interconnect with the inclusion of the effects of parameters uncertainties conclude the paper.

I. INTRODUCTION

The shrinking of the physical size of electronic devices, along with the increase of their speed, is leading to a non-negligible impact of the manufacturing process on the system performance. In this framework, designers demand the availability of simulation techniques and tools for the stochastic analysis of high-speed interconnects and circuits in the early design phase. The typical resource for the assessment of parameters variability effects on system responses is based on the application of the brute-force Monte Carlo method, or possible enhanced tools allowing to select the optimal subset of model parameters in the whole design space [1]. These methods, however, are inefficient and prevent their application to the analysis of complex realistic structures, such as the data link of Fig. 1.

A well-known example is provided by the generation of eye diagrams from the voltage responses received at the far-end side of the interconnect (e.g., the IC on the right of Fig. 1). The prediction of the eye features, like the width or opening, is currently one of the tools for the assessment of data link reliability. In this specific application, a large number of bits as well as a dense exploration of the design space, aimed at collecting some quantitative information on the statistical properties of the eye features, must be considered. The above requirements lead to prohibitive simulation times, especially when the computational cost of a single simulation is large, as in the case where transistor-level models are employed to mimic the behavior of the I/O ports of ICs. Although accurate, this approach is extremely inefficient, and cleverer solutions are therefore highly desirable.

To overcome the previous limitations, in this paper, a simulation strategy aimed at improving the efficiency of both the simulation of the data link and the assessment of the impact of its uncertainties on the eye diagram is proposed. The contribution in the paper is twofold. Firstly, state-of-the-art models of IC buffers are used in place of transistor-level description of devices. IC models have already been proven to provide accurate results with large efficiency improvements [2]. This makes the Monte Carlo analysis feasible, but still time consuming. Secondly, the stochastic collocation method (SCM), combined with Lagrange interpolation [3], is used to further speed up the transient simulation. The SCM has already been successfully used for the statistical analysis of high-speed interconnects [4], [5], and is here conveniently applied to the SPICE simulation of realistic printed circuit board (PCB) structures with nonlinear dynamical components, like the one of Fig. 1.

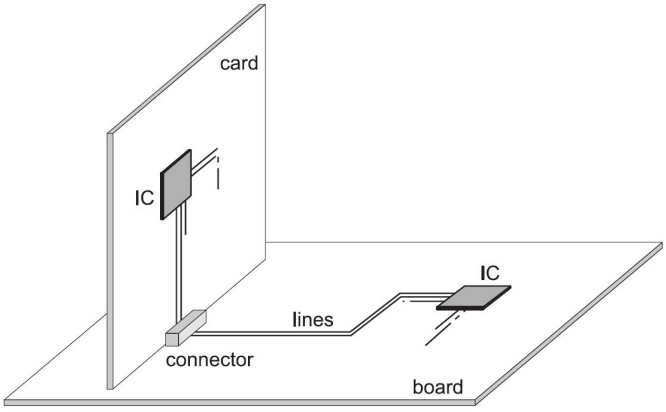

Fig. 1. Example of a high-speed data link consisting of a long propagation path between two digital integrated circuits.

II. APPLICATION TEST CASE

In the scheme of Fig. 1, a single point-to-point interconnect is considered, where the output port of the IC on the card communicates with another IC on the board, which acts as a receiver circuit. The intermediate connector and the receiver are represented by an LC circuit ($L = 2\,\text{nH}$, $C = 2\,\text{nF}$) and a simplified equivalent composed by clamp diodes and a $10\,\text{pF}$ ideal capacitor accounting for the dominant behavior of the IC input ports, respectively. The two interconnects in Fig. 1, one on the card and one on the board, are both copper microstrips with the following nominal parameters: width $w = 150\,\mu\text{m}$, copper thickness $t = 30\,\mu\text{m}$, substrate thickness $h = 100\,\mu\text{m}$, relative dielectric permittivity $\epsilon_r = 4.1$.

The above assumptions are made for simplifying the structure and thus concentrating on the effects of the variation

of the parameters defining the IC output ports and the PCB interconnect on the performance of the data link. Specifically, the variability is provided by the strength of the driver, the width of the PCB microstrip, and the relative permittivity of the dielectric substrate, which are modeled as independent random variables with Gaussian distribution (additional details will be provided hereafter, in Section V). A Texas Instruments transceiver (model name SN74ALVCH16973, power supply voltage $V_{DD} = 2.5\,\mathrm{V}$), whose HSPICE transistor-level description is available from the vendor official website, is used in place of the IC on the left. The data pattern used for this study is a 200-bit long sequence with a bit time of 3 ns and Gaussian jitter error (zero mean and $0.15\,\mathrm{ns}$ standard deviation).

III. Determnistic IC (buffer) modeling

Different approaches are currently in use for generating IC models. The standard solution is offered by the Input/Output Buffer Information Specification (IBIS) [6], which assumes simplified equivalent circuits of typical buffer structures and provides guidelines for collecting the key features of devices, like the static characteristics of the output port of a buffer, the equivalent capacitance of the silicon die, the parameters of the equivalent circuit of the package, etc. Recently, other approaches that complement IBIS and provide improved accuracy for recent device technologies have been proposed [2], [7], [8]. In this study, the modeling methodology presented in [2] is considered.

In the case of the output ports of IC buffers, the relation involving the port electric variables can be expressed as

$$i(t) = w_H(t) i_H(v(t), t) + w_L i_L(v(t), t), \tag{1}$$

where $v(t)$ and $i(t)$ are the voltage at output port of the IC buffer and $i(t)$ is the associated current flowing out of the buffer output terminal. In the above equation, w_H and w_L are suitable weighting functions which play the role of the input signal driving the buffer state, whilst i_H and i_L are suitable parametric relations accounting for the device behavior in the fixed high and low state, respectively. The parameters defining equation (1), i.e., the weighting functions $w_{H,L}$, and the coefficients in the parametric relations $i_{H,L}$, can be computed via a well-established procedure from port voltage and current responses to a predefined set of stimuli (see [2] for additional details).

It is relevant to remark that the proposed model for IC buffers has been proven to provide accurate results in the prediction of the eye diagram, with speed-up on the order of 10-100×. Specifically, timing errors computed as the maximum delay between the reference transistor-level model and the proposed model responses at the $V_{DD}/2$ level, turn out to be on the order of 1% of the bit time. Also, for the same comparison, the relative error obtained in the prediction of the openings of eye diagrams is 2%.

IV. The stochastic collocation method

This section provides an overview of the SCM, with a brief discussion of the three main features of the Lagrange interpolation, i.e., the interpolating polynomials, the clever choice of the collocation points, and the extension to account for multiple random variables.

Lagrange interpolation. The basic idea of the SCM and Lagrange interpolation is to sample the stochastic system response at (few) clever points and to reconstruct the overall response in the whole random space by interpolation [3]. For a time-domain response $y(t, \xi)$ depending on a single random variable ξ, the interpolation is

$$y(t, \xi) \approx \sum_{i=0}^{P} y(t, \xi_i) \Phi_i(\xi), \tag{2}$$

where $\{\Phi_i\}$ are the Pth-order Lagrange polynomials associated to the collocation points ξ_i. They are built as

$$\Phi_i(\xi) = \prod_{\substack{0 \le j \le P \\ j \neq i}} \frac{\xi - \xi_j}{\xi_i - \xi_j}, \tag{3}$$

and the following property holds:

$$\Phi_i(\xi_j) = \delta_{ij}, \tag{4}$$

with δ_{ij} the Kronecker's delta.

It is worthwhile noting that (2) turns out to be an analytical function, where a limited set of responses $y(t, \xi_i)$, evaluated for predefined samples ξ_i of the random variable ξ, are used to reconstruct the continuous behavior by means of Lagrange polynomials. Such an analytical expression can be used as a computationally-cheap model for a fast sampling of the random response and extraction of statistical information.

Choice of the collocation points. One key issue of the solution consists in finding a good set of collocation points for which to evaluate the random response. Although different choices are available, the analogy with Gaussian quadratures suggests to use the roots of the polynomials which are orthogonal to the distribution of the random variable ξ. For standard distributions, such as uniform or Gaussian, these polynomials are well-known and correspond to the Legendre and the probabilists' Hermite polynomials, respectively. Hence, in the case of Gaussian variability, for a given value of P in (2), the points ξ_i are given by the roots of the $(P+1)$th-order Hermite polynomial. For instance, if $P = 3$, we have four evaluation points at $\xi_{0,1} = \pm 2.334$ and $\xi_{2,3} = \pm 0.742$.

Extension to multiple random variables. A straightforward generalization to the case of multiple random variables is to use a multivariate interpolation where the collocation points are represented by a tensor product grid obtained from the one-dimensional case. In turn, the multivariate Lagrange polynomials are built as products of univariate polynomials. For example, given two random variables ξ and η, the two-dimensional collocation grid is represented by all the possible points $\boldsymbol{\xi}_i = (\xi_m, \eta_n)$, with $0 \le m \le P_1$ and $0 \le n \le P_2$. It should be noted that a square grid (i.e., $P_1 = P_2 = P$) is usually employed, but this is not mandatory. The bivariate Lagrange polynomials are then obtained as

$$\Phi_i(\boldsymbol{\xi}) = \Phi_i(\xi, \eta) = \Phi_m(\xi) \Phi_n(\eta), \quad \forall m, n. \tag{5}$$

The total number of response samples to be computed is thus

$$Q = \prod_{k=1}^{n} (P_k + 1), \tag{6}$$

where n is the number of random variables. For large values of P_k and/or n, sparse grids allow to mitigate the growth in the number of collocation points [3].

V. Numerical results

This section collects the numerical results on the stochastic simulation of the test case discussed in Section II. As briefly outlined above, among the different sources of variations, we select and focus on the following three parameters: (i) the strength of the output buffer of the IC driver, (ii) the width of the PCB microstrip interconnects, and (iii) the permittivity of the dielectric substrate. This choice is relevant because it allows to model typical variations in the output current of IC buffers, as well as the uncertainties introduced by the etching process and by the impurities in the substrate materials. The buffer strength is varied by applying a Gaussian random weight with unitary mean and 10% relative standard deviation to the simplified model (1). The remaining parameters are considered as two additional independent Gaussian random variables having the nominal parameters given in Section II, i.e. $w = 150\,\mu$m and $\epsilon_r = 4.1$, and relative standard deviations of 10% and 5%, respectively.

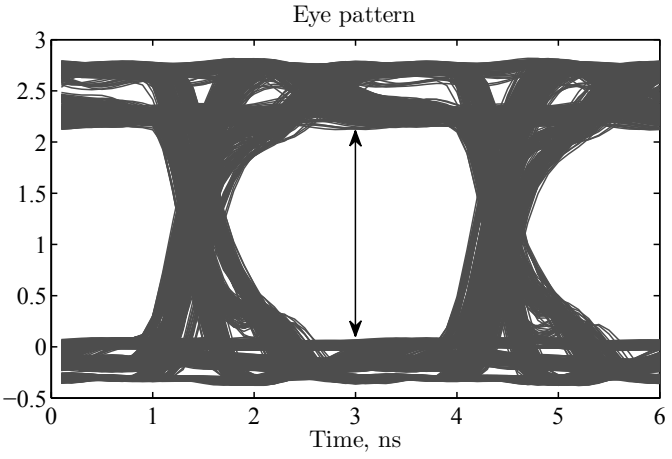

Fig. 2. Eye diagram arising from the voltage signal received at the right-hand side of the data link of Fig. 1. The double arrow identifies the eye opening.

In order to quantify the effects of parameters variability on the system response, the eye diagram derived from the voltage waveforms at the receiver side of the PCB link of Fig. 1 is computed. Fig. 2 shows for example the eye pattern obtained by means of a Monte Carlo analysis, carried out by means of the pertinent feature available in HSPICE and by using the IC output port model (1). This eye diagram is from now on assumed as the reference. It is relevant to remark that the use of the equivalent model (1) allows to reduce the Monte Carlo simulation time to 5 h and 6 min for a 10000-run analysis, whereas the predicted time for a transistor-level simulation is more than one day and a half. However, this computational burden is still rather heavy for a circuit designer , and can be further reduced thanks to the SCM, as shown in the following.

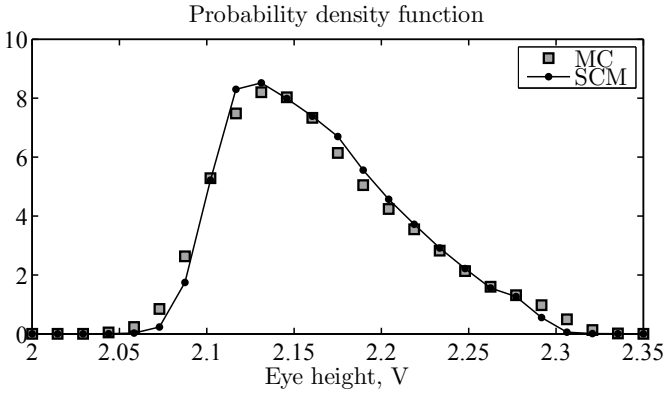

Fig. 3. Probability density function of the eye aperture for 10000 samples of the random parameters. The curve labeled "MC" refers to the Monte Carlo simulation, while the distribution marked "SCM" refers to the response obtained via the SCM and a third-order Lagrange interpolation.

In fact, the stochastic link response can be alternatively obtained by interpolating, according to the SCM, a reduced set of simulated responses. For example, having three random variables ($n = 3$) and using a third-order interpolation ($P_{1,2,3} = 3$), only 64 simulation runs are required. A 64-term Lagrange interpolation is then obtained according to (2). The fast random sampling of such an interpolation enables an alternative and convenient construction of the eye pattern. For a thorough comparison between the two approaches, a quantitative information is extracted from the eye diagrams, i.e. the probability density function (PDF) of the height, indicated by the double arrow in Fig. 2. Fig. 3 shows the PDF of the eye aperture computed from the Monte Carlo- and the SCM-based eye diagrams, both obtained by considering 10000 samples of the random parameters. A remarkable accuracy can be appreciated.

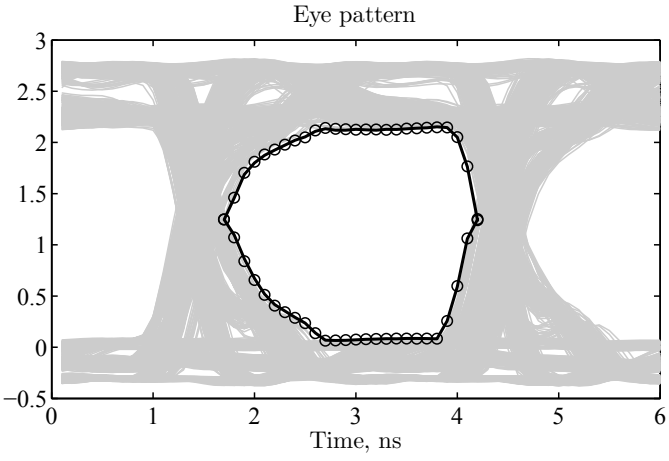

Fig. 4. Eye diagram of Fig. 2, with the inclusion of the profile of the eye opening computed with a confidence level of 99% and based on 10000 samples of the random parameters. Solid line: prediction via the proposed technique; circles: profile obtained via Monte Carlo simulation.

As an additional comparison, Fig. 4 shows the profile of

the eye opening computed by considering a 99% confidence level. Briefly speaking, this means there is a 1% probability that the stochastic link response lies inside the black mask in Fig. 4. Also for this case, the prediction obtained with the SCM excellently compare with the result provided by the Monte Carlo analysis. As far as the efficiency is concerned, the SCM-based approach requires only 64 circuit simulations, which take 1 min and 35 s, whilst a negligible additional time of 1 s is needed to sample the interpolating polynomial. An impressive speed-up of about $200\times$ is thence obtained.

VI. Conclusions

The simulation of eye patterns including the effects of parameters uncertainties in high-speed data links is addressed in this paper. The proposed approach is based on the available deterministic models of distributed interconnects and on state-of-the-art models of the I/O ports of devices. Furthermore, the variability on the link responses is taken into account via Lagrange interpolating polynomials, whose coefficients are computed in accordance with the SCM, i.e. via a small number of SPICE simulations at predefined points in the design space. The combination of equivalent circuit models for nonlinear devices and of the SCM allows a considerable reduction in the computational cost compared to the Monte Carlo analysis at transistor level.

The proposed method has been applied to a realistic PCB interconnected structure, leading to accurate results and a remarkable efficiency improvement in the statistical assessment of eye-diagram parameters.

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