A high precision power supply meter*

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This paper describes an efficient implementation of a power supply meter. The implementation is based on the Fourier series decomposition algorithm, using CORDIC algorithm for complex mathematical computations. It is able to calculate RMS and peak values, phase shift, power factor, and complex, active, and reactive power for two periodic waveforms up to the 25^{th} harmonic.

Several implementation alternatives are compared pointing out the advantages and the disadvantages of each one. Then the circuit structure at block level is described with emphasis on the advantages resulted from the use of CORDIC algorithm, followed by some considerations over precision issues.

1 INTRODUCTION

Since the discovery of the electricity by Volta and up to our days, the electric power faced a constantly growing utilization. The electric consumers diversify more and more and, at the same time, they change their interaction with the power supply. Although the rational utilization of the power distribution network becamed an issue long before the electromagnetic compatibility was an acute problem, now they have to be faced together by the electric power end user.

The need to watch constantly the way that large power consumers are interacting with the supply is a must in our days. This is accomplished by special equipments capable of performing accurate measurements of power supply parameters and signal or initiate corrective actions when necessary.

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We described in this paper a circuit that can be used to perform the electric measurements needed for such an equipment. This circuit will be the result of a project we do in the framework of SUMIS action for DTA s.r.l., an SME located in Milan, Italy.

2 DESIGN CHOICES

The goal of the project is to build a measurement instrument for AC values. It should be able to measure RMS values and harmonic peak values for each of its two analog inputs, and phase shift, active and reactive power, and power factor individually for each harmonic up to the 25^{th}.

First choice to be made was if an analog or a digital implementation is appropriated.

The analog solution would consist mainly in putting together several switched capacitor filters. These filters should comply to very tight specifications in terms of low order harmonics rejection and phase distorsion for the passband. Such filters had to be designed by hand, with a very accurate layout. Long and extensive electric simulations in transient mode and the layout complexity would made the design last too long and would give very few guaranties for a first time working product. Moreover, this solution would rise the problem of finding an available technology providing SC filters for very low frequencies (as low as 50Hz).

Moving the analog solution to a digital implementation leads mainly to a DSP machine acting very much as the analog filters. This solution is not less expensive in terms of area but the design flow is much more simplified allowing a VHDL description and synthesis approach.

Given that we had to do a harmonic analysis, we looked toward the FFT (DFT) algorithm as an optimized DSP approach for this task. We noted that a RAM buffer is required to store the input samples for processing and that a lot of multiplications are to be done in the DFT algorithm. We noted also that DFT works for any kind of input signals.

As we had to measure only periodic waves, we decided to implement a particularization of the Fourier transform, the Fourier series development, only for the harmonics of interest. This solution has the following main advantages over the DFT:

- the computation effort is much lower;
- real time processing can be done avoiding input samples storage on board;
- the algorithm is simpler to implement resulting in a smaller area;
- the resulting DSP machine is more observable and easier to debug.

In general, all digital implementations offer larger flexibility in postprocessing the results for obtaining derived values from the direct measured ones, that are the harmonic peak value and phase. They can also be interfaced with a microprocessor system and can be much easier integrated into a remote measurement or control equipment.

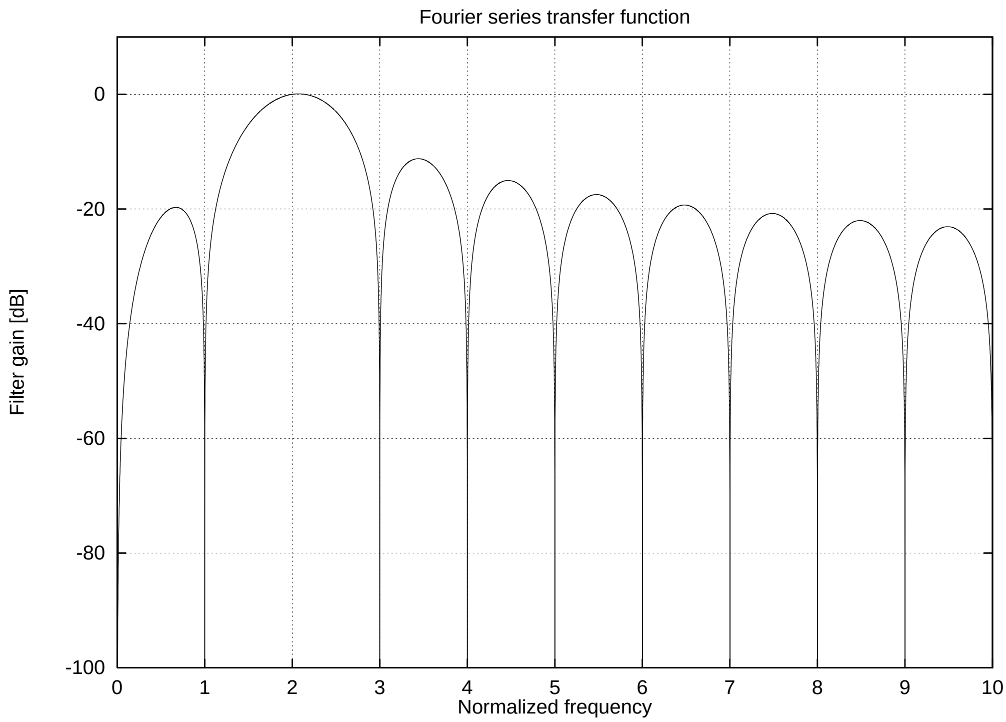

Figure 1: Fourier series transfer characteristic

The DFT and Fourier series implementations are by far more accurate and efficient than the analog or the digital implementation of general purpose filters. The Fourier series algorithm in fact acts like a passband filter for the selected harmonic while having transmission zeroes for all other harmonics of the fundamental. In figure 1 is shown the theoretical transfer characteristic of a Fourier series that selects the second harmonic.

3 CIRCUIT STRUCTURE

Our aim was to keep the circuit structure as simple and small as possible while avoiding timing problems.

The block schematic we choose is presented in figure 2. For sake of simplicity we decided that a microprogrammed machine is the most suited. This way we keep the *Control* block simple and small. A part of the ROM is used for storing the microcode and is in tight interaction with the *Control* block.

In order to avoid timing problems due to the high clock frequency required by the real time processing, we used two separate real time processing paths, one for current samples and one for voltage samples. For this purpose, there are two distinct A/D converters that sample synchronously the voltage and current lines for one fundamental period. Real time processing is no more required in the postprocessing part, so this part uses only one bus.

The computational part of the circuit is done using two implementations of the CORDIC algo-

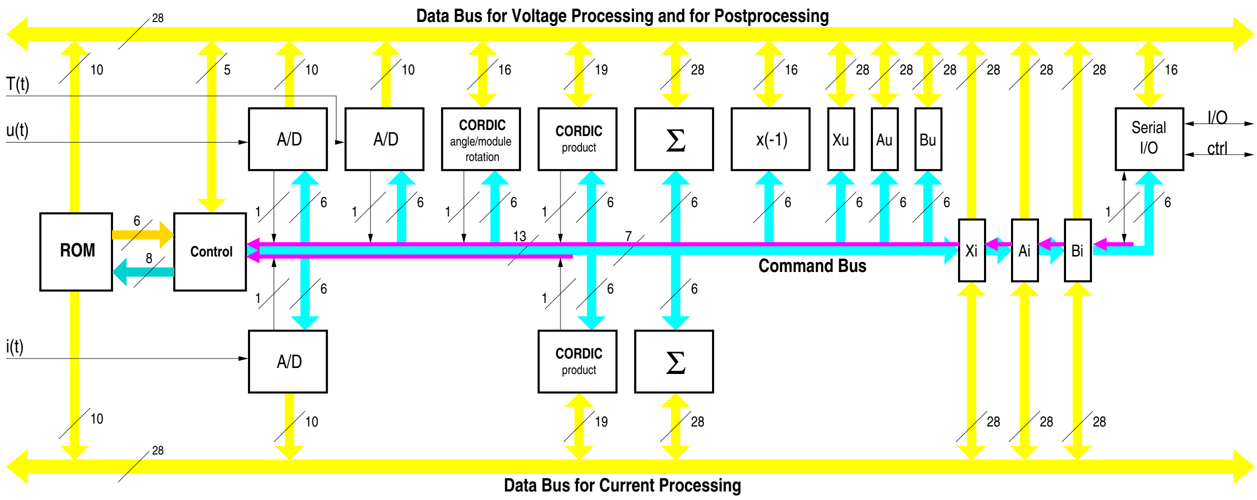

Figure 2: Block schematic

rithm: *CORDIC angle/module/rotation* and *CORDIC product*.

The first implementation performs essentially vector rotations. Thus, with slight algorithm changes it is able to compute in one step the vector module and the vector angle using vector X and Y components as input. In another operation mode, the same block is able to rotate a vector with a given angle, returning vector X and Y components for the new position. This operation mode is used to compute the *cosine* trigonometric function for a given angle for power factor measurement or to compute the active and reactive powers as X and Y components for the complex power.

The second CORDIC implementation, *CORDIC product*, is optimized for real time product calculation. There are two such blocks, one for the current processing path and one for the voltage path.

The *Control bus* is used in common by the two paths in the processing phase. It will carry mainly microcode instructions that are peeked by the *Control* block from the ROM and that will be decoded by each block in part. The same bus carries also busy/ready feedbacks from the blocks that need several clock cycles for completing their task.

The *Serial I/O* interface will implement a slave I^{2}C protocol and will be used to read commands from an external digital system and to output measurement results.

A third A/D converter is provided for temperature measuring. This is a customer's request.

4 PRECISION CONSIDERATIONS

All mathematical operations are done using integers represented in 2 complement. By using this fixed point representation we considerably simplified the operation of the mathematical blocks.

The drawback with respect to using a floating point representation is that more attention should be paid to overflows and underflows.

To dimension the internal busses, ROM words, and recursive algorithms iteration count we used the precision specifications and the maximum allowable precision on output. In fact, system constraints imposed an output size of 16 bits for measurement results that limits the results precision. Thus we start dimensioning backward, evaluating the output truncation error and following all data flows in the algorithm up to the inputs. We imposed that all intermediate errors be at most a tenth of the largest allowable error on output for that measurement.

We have done also a theoretical worst case error estimation by cumulating in the algorithm the effects of the maximum input quantization error, internal operands truncation error, recursive algorithms truncation error, etc. These error estimations are very pessimistic and may never happen in real measurements. Moreover, when operating with real input waveforms, several errors may compensate each other during the same measurement, leading to a much smaller error on output results.

On the other hand, even in the worst case estimations described above we still did not take into account several important error sources as: integral approximation using a finite term sum, A/D converter errors, A/D signal conditioning errors (noise, phase shift, DC offset), that may heavily influence the overall precision of the measurements.

In order to validate the algorithm and the precision performance we developed a C language program that emulates most part of the hardware behavior as: operands truncations, input samples quantization approximation, controller operation, etc. The standard test consisting in $2 \cdot 8^6 = 524288$ distinct input waves and calculating all the output values for the fundamental and each harmonic up to the 25^{th} needs about 2 weeks to complete on a SUN SPARCstation 20 workstation.

5 CONCLUSIONS

We found that using the Fourier series decomposition and the CORDIC algorithm for the task of harmonic analysis for periodic waveforms is very effective both as computational effort and circuit size. The estimated precision class of the instrument is better than 0.5 for full scale input waves using 10 bit A/D converters, without taking into account the analog part errors.

The microprogrammed architecture we chosed is very flexible allowing easy algorithm change to add or eliminate postprocessing operations, to change the number of input samples per fundamental period, bus size scaling for improving precision, etc.

The circuit size may be further reduced by eliminating the second processing path. The current and voltage samples may be processed in sequence using the same blocks and the same bus by doubling the clock frequency and changing accordingly the microcode sequencing.

The circuit is designed using SYNOPSYS VHDL synthesis for the AMS 0.8μm digital CMOS technology.

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