Electric clock for Nano-magnet Logic Circuits

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***Abstract*—Among the Field-Coupled technologies NanoMagnet Logic is one of the most promising. The low power consumption coupled with the possibility to combine memory and logic in the same device, makes this technology the ideal candidate for low power and portable applications. However, the necessity to use an external magnetic field to locally control the circuit represents the weakest point of this technology. The high power losses in the clock generation system wipes out most of the advantages of this technology.**

**In this work we propose a clock system based on a piezoelectric actuator that allows to electrically control NanoMagnet Logic circuits. The low power consumption coupled with the fact that electric fields are easier to generate at nanoscale makes this clock system a competitive candidate as final clocking mechanism for this technology. Moreover the solution here proposed is feasible with current technology, and this represents a strong key point of the proposed solution.**

## I. Introduction

In recent years the interest in Field-Coupled devices, like NanoMagnet Logic, is rapidly increasing [1]. In this logic single domain nanomagnets are used as base cell. Due to particular magnetic properties, like shape or magnetocrystalline anisotropy, magnets can have only two stable states that are used to represent the logic values '0' and '1' [2]. Circuits are built placing many cells near each others, and information propagates through magnetostatic coupling of neighbor cells. A clock mechanism is required to correctly propagate information through the circuit [3]. Magnets are forced in an intermediate unstable state applying an external magnetic field. When this magnetic field is removed magnets realign themselves following the input element. Since the number of magnets that can be cascaded is limited [4], a multiphase clock system is necessary to build working circuits. Three clock signals (Figure 1.A) with a phase difference of 120 degrees are applied to small areas of the circuits called clock zones composed by a limited number of elements. With this system in every instant when magnets of a clock zone are in the SWITCH state (Figure 1.B), magnets on their left are in the HOLD state and act like an input and magnets on their right are in the RESET state and have no influence. In this way signals propagate in a specific direction [5].

Magnetic field is generated through a wire placed under the magnets plane [6], however the required value of current is quite high and the associated power consumption wipes out the major advantage of this technology. Other solutions uses multilayered magnets clocked using spin-torque coupling

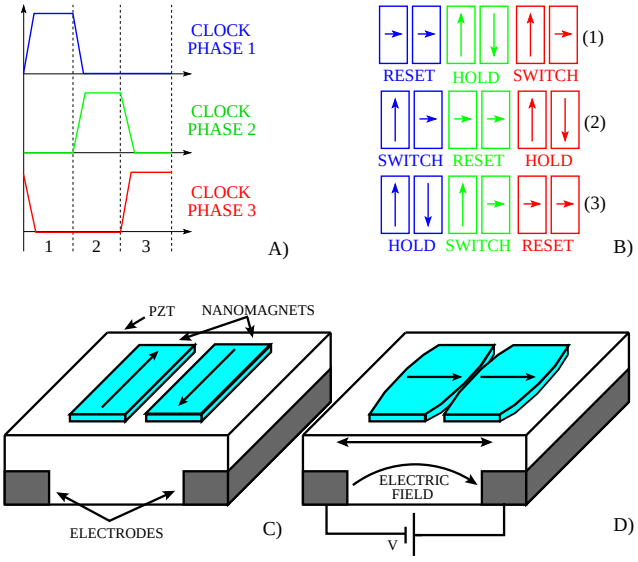


Fig. 1. A) 3-phase clock signals. B) Signal propagation during the clock period. C) Electric clock mechanism, when an electric field is applied the strain induced by the piezoelectric layer rotates the magnetization vector of 90 degrees.

through a current that flows through the magnets [7] or multiferroic structure where the magnets is composed by a piezoelectric layer and a magnetostrictive magnetic layer that can be clocked through an electric field [8]. Both solutions show remarkably low power consumption compared to the classic approach. We propose a solution similar to [8], with the difference that magnets do not have a multilayered structure: They are made by only one magnetic material and are deposited directly on a piezoelectric layer (Figure 1.C). When an electric field is applied magnets are forced in the RESET state by the strain induced by the piezoelectric layer (Figure 1.D). While renouncing at some performance compared to [8], this structure as the advantage that can be fabricated with available technology.

## II. Results

The proposed circuit structure is shown in Figure 3. Single logic gates on mechanically separated islands, obtained by patterning with optical lithography a piezoelectric layer (PZT), are used to build circuits. The basic logic gate is a 3-magnets AND/OR gate obtained changing the shape of the

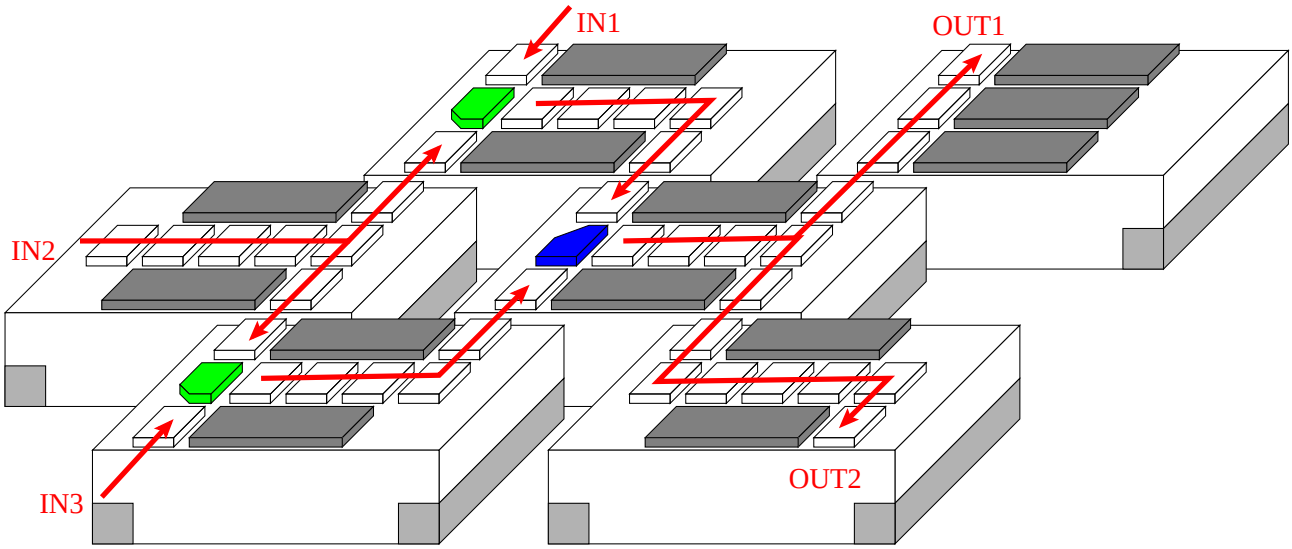


Fig. 2. Example of circuit layout using the proposed clock.

central (darker) element [9]. Since the horizontal coupling in a chain of magnets is antiferromagnetic, every magnet has the inverted value with respect to its neighbors. As a consequence, if there is an odd number of magnets in a clock zone the logic function is inverted and NAND/NOR gates are obtained. NAND/NOR are universal gates that can be used to build any circuit. Magnets can be made by IronTerbium with sizes of 65x50x10 $nm^3$ or Nichel with sizes of 55x50x10 $nm^3$. Electrodes are buried under the PZT which can have a thickness in the range of 70-600nm. Magnets cannot be placed directly above the electrodes because in those areas the electric field is near 0. Shielding blocks are used to avoid errors in the vertical signal propagation [10]. Every NAND/NOR is in an independent clock zone, and can have a width of 3 or 5 magnets. The smaller the structure is the lower energy is required to reset the magnets, as can be seen from Figure 3, where the switch energy of a gate for different gate sizes, composition and oxide thickness is shown. Circuits are simulated using the free tool Magpar [11]. Simulation shows that the energy consumption, considering all the source losses, is 1000 times lower than the classic magnetic field approach.

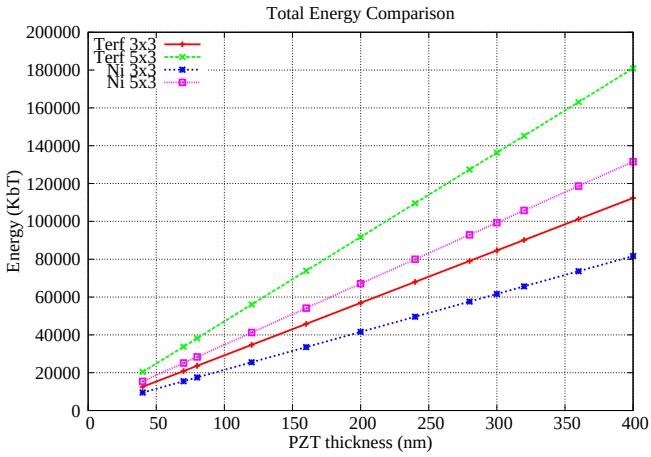


Fig. 3. Energy comparison with different material and sizes.

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