# Modeling and Characterization of Metal/SiC Interface for Power Device Application

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*Dedicated to my parents...*

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**Abstract**

Silicon carbide is a wide band-gap semiconductor widely considered to be an excellent material for the fabrication of power devices able to operate in extreme environmental conditions. Its superior properties such as wide energy bandgap, high hardness, chemical inertness, high electrical field breakdown strength and high thermal conductivity enable electronic devices, based on it, to operate at high temperatures, high voltages and high frequencies and make it an attractive semiconducting material for the power electronics industry. Since 1999 a number of electronic devices based on silicon carbide are commercially available such as Schottky barrier diodes with voltage rating of 300 - 1700 V (as of 2011) which often show non-ideal electrical behavior.

Non-ideal electrical behavior is manifested in the abnormal current—voltage characteristics and greater than unity ideality factors. Various theories exist as to the origin of these non-idealities some attribute them to different conduction mechanisms such as generation-recombination and edge-related currents and others to the inhomogeneous Schottky barrier. We have considered the approach, taken by Tung, which can explain all the non-ideal behaviors with thermionic emission theory alone by assuming the Schottky barrier height to be inhomogeneous. Inhomogeneous Schottky barrier implies spatially varying isolated low barrier height regions existing alongside a homogeneous high Schottky barrier. These regions are supposed to interact, in case of being situated together, resulting in the region with low barrier height to be pinched-off. If the pinch-off occurs the low barrier height region (or patch depending on the shape) has a Schottky barrier height equal to the 'saddle point potential' in front of that patch or low barrier region. Whole Schottky barrier is assumed to be composed of numerous such low barrier height patches. These patches are considered to be embedded into the high background Schottky barrier and define the overall current transport through the Schottky barrier diode. A similar model is the parallel conduction model presented by D. Defives et al. which instead of considering the Schottky barrier to be composed of various small patches, divides the Schottky barrier into two major parts each with different Schottky barrier height and both existing simultaneously within one Schottky barrier diode. Though accurate to some extent, this model considers the two Schottky barrier heights to be electrically independent of each other; which is not true in all

situations. After applying Tung's theoretical model it was possible to extract nearly correct value of Richardson constant for the Schottky diodes with titanium and molybdenum Schottky contacts on 4H silicon carbide. It was also possible to fit the experimental data correctly with Tung's theoretical model. Note: The diodes used in this research work were fabricated during a research project involving Vishay and Politecnico di Torino.

# Chapter 1

# Introduction

Power electronic devices based on silicon carbide (SiC) are gaining importance and popularity, among researchers, because of their superiority over their silicon counterparts. Devices based on SiC exhibit better performance than the conventional electronic devices, are less expensive and may help to reduce energy losses [1]. Silicon carbide comes with material properties that enable devices based on it to operate at high temperature, high power and high frequencies. The first power electronic devices based on SiC were Schottky barrier diodes followed by other devices such as the introduction of JFETs in 2008 and MOSFETs in 2011 with a voltage rating of 1200 V [2]. Though superior in some qualities these devices often show non-ideal electrical behavior due to inhomogeneous Schottky barrier height. The non-ideal behavior of electronic devices implies non-ideal electrical parameters which are characterized by inhomogeneous Schottky barrier height with excess device current at low applied bias, temperature dependence of the ideality factor and reverse leakage currents.

Scope of this work is to address the Schottky barrier height inhomogeneity problem and to propose an explanation for the origin of abnormal electrical behavior of the Schottky barrier diodes. For this purpose the author has electrically characterized a number of Schottky barrier diodes with molybdenum and titanium Schottky contacts in order to achieve the best fit to the experimental data and to extract correct value of a universal constant known as Richardson constant. The model applied falls within the perimeter of thermionic emission theory with slight modifications proposed by R. T. Tung (who treats Schottky barrier height as composed of very small low barrier height patches embedded in the high background Schottky barrier). According to this model these low barrier height patches

play very important role in defining the current transport through the Schottky barrier diode. We have applied this model to a number of Schottky barrier diodes (SBDs) and have tried to assess its accuracy in predicting the electrical behavior of the Schottky barrier diodes[3, 4, 5].

In this thesis mathematical modeling and electrical characterization of SiC based Schottky barrier diodes is presented. In chapter 2 a general overview of SiC with material properties, applications and brief history will be given. In chapter 3, metal-semiconductor contacts in general and metal-SiC contacts in specific are covered and in chapter 4 process technology for the fabrication of SiC based Schottky diodes will be presented followed by different characterization techniques in chapter 5 and results and discussion in chapter 6. Finally the thesis will be concluded.

# Chapter 2

# An Overview of Silicon Carbide

Silicon carbide (SiC) is a wide band-gap semiconductor with a number of good properties which make it a favorable material for the fabrication of high power electronic devices able to operate at high temperature and high frequencies. Properties like its energy band-gap, thermal conductivity and electric field breakdown strength are among those which will be discussed in detail in this chapter after a brief mention of the history of SiC from its discovery to its use in the electronics industry [6, 7, 8, 9].

## 2.1 History

Silicon carbide was first discovered by Jöns Jacob Berzelius in 1824. Later it was Acheson who produced SiC by heating coke and silica together, in a furnace—a method still known as Acheson process. He called the new compound "carborundum" which was to be used for abrasion and cutting due to its hardness. First use of SiC in electronics was the invention of SiC LEDs in 1907. But the use of SiC in electronics was not to last longer because of difficulties in producing high quality SiC crystals due to unavailability of any controlled crystal growth technique [2, 10].

In 1955 an important crystal growth technique was invented by J. A. Lely which made controlled crystal growth possible. This resulted in huge research activity on SiC for a short time and first academic event on SiC was held in 1958, a conference at Boston. After this event no considerable technological activity can be seen

mainly because no high quality SiC substrates were available at that time [10].

It was in 1970s when two Russian scientists Tairov and Tsvetkov discovered a new method for SiC crystal growth known as seeded sublimation growth which made possible, for the first time, the production of SiC wafers. This was followed by the discovery of yet another technique called 'step controlled epitaxy' in 1987 which made possible epitaxial growth of SiC and resulted in the commercialization of first power electronic devices based on SiC such as the Schottky diodes and MESFETs produced by Cree Inc. and Infineon [10].

## 2.2 Physical and Chemical Properties

Silicon carbide is a colorless solid substance with a hardness of 9 on Mohs scale and a Young's modulus of 424 GPa [11]. It rarely involves in chemical reaction at room temperature and is not found in liquid form but sublimes to Si, $Si_2C$ and $SiC_2$ vapors at more than 1800 $^oC$ temperature. Doping of the wafers is normally achieved through ion implantation or direct growth of ions into the silicon carbide [10].

### 2.2.1 Energy Bandgap

Energy bandgap of any solid is the difference between top of the valence band and the bottom of the conduction band. It represents those energy states which cannot be occupied by electrons. If an electron in the outer most shell of an atom is supplied with energy equal to energy bandgap it will become a free electron. Energy bandgap is important in understanding whether the solid is good electrical conductor or bad electrical conductor. Bad conductors or insulators have large energy bandgaps while good conductors have very small energy bandgaps or no energy bandgaps at all because they have continuous conduction band and valence band [12].

There are some solids which have energy bandgaps in between conductors and insulators known as semiconductors. In semiconductors we have a narrow energy gap between conduction band and valence band e.g. silicon has an energy bandgap of 1.1 eV and germanium has 0.67 eV [13]. Some semiconductors have energy bandgaps much larger than these semiconductors, these are called "wide bandgap semiconductors" such as GaN with energy bandgap of 3.4 eV and silicon carbide which comes with a bandgap of 3.39 eV for 3C-SiC polytype, 3.33 eV for 2H-SiC and 3.265 eV for 4H

SiC polytype (which is normally preferred more over other polytypes of silicon carbide). The wide bandgap of SiC is important for SiC based devices to operate at high temperatures where Si based devices normally fail to perform [10].

### 2.2.2 Breakdown Electric Field Strength

The magnitude of electric field which results in the total breakdown of the material to which the field is applied is called the breakdown electric field strength ($E_{max}$) of that material. It is different for different materials and also depends on doping concentration of the semiconductor. The $E_{max}$ of SiC is 2.49 MV/cm and that of Si is 0.401 MV/cm for the equal doping levels [10].

### 2.2.3 Saturation Drift Velocity

Charge carriers in a semiconductor have drift velocities which under normal circumstances are proportional to the magnitude of applied electric field. Drift velocity of a charge carrier increases with increasing electric field, inside a semiconductor, until a certain limit is reached after which the charge carriers cannot move faster no matter how strong is the electric field; this velocity is known as saturation drift velocity or simply saturation velocity. Apart from applied electric field saturation velocity also depends on a constant called carrier mobility. Every material has a constant and characteristic carrier mobility which is different for different semiconductors. A semiconductor with large carrier mobility will demonstrate high charge carrier velocity than the one with low carrier mobility value at same magnitude of electric field [14]. Silicon carbide has a very high saturation drift velocity making SiC a suitable material for the fabrication of high frequency electronic devices. The saturation drift velocity of SiC is 2 x $10^7$ cm/sec which is almost double that of silicon's and is one of the advantages of SiC as semiconductor material because it allows SiC based devices to achieve high channel currents and high gains [10].

### 2.2.4 Thermal Conductivity

Doped silicon carbide has thermal conductivity values of above 4 $W.cm^{-1}.K^{-1}$ and pure SiC has a thermal conductivity value of 4.9 $W.cm^{-1}.K^{-1}$ while silicon has a thermal conductivity value of 149 $W.cm^{-1}.K^{-1}$ almost thirty times as large as that of silicon carbide.

Thermal conductivity is the measure of material's ability to conduct heat and must be as less as possible (for the fabrication of power electronic devices) because large thermal conductivity affects the carrier mobility of devices at high temperatures and leads to the overall decreased performance of the device [10].

### 2.2.5 Crystal Structure

Silicon carbide is a crystalline solid with four atoms of carbon covalently bonded (with $sp^3$ hybrid orbital) to a silicon atom, at the center, forming a tetrahedron. The distance between two carbon atoms is 3.08 Å and the distance between a carbon and silicon atom is 1.89 Å as shown in Fig. 2.1[10, 15].

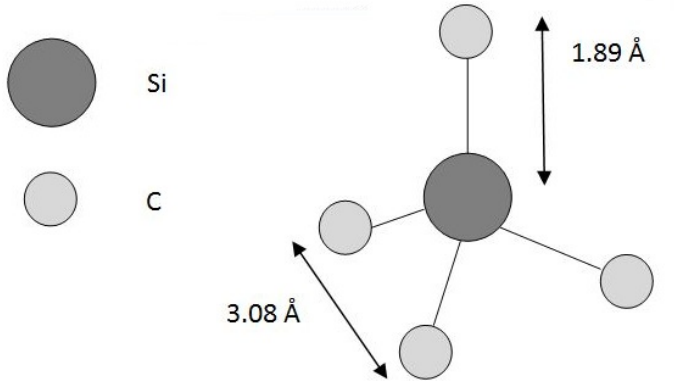


Figure 2.1: Silicon carbide basic unit [not to scale]. Source [10]

Silicon carbide exhibits polarity along c-axis and it is possible to achieve a SiC wafer with only Si atoms on the surface or only C atoms on the surface on the other side with different chemical properties as shown in Fig. 2.2 [10, 15].

### 2.2.6 Polytypes of SiC

Silicon carbide occurs in nature with more than 300 polytypes [1]. 6H-SiC and 4H-SiC are the ones mostly used for the fabrication of high frequency and high power electronic devices. Other polytypes include 3C-SiC, 2H-SiC and 15R-SiC according to Ramsdell notation in which the number in the beginning stands for the number of hexagonal Si-C bilayers (or planes) after which the same stacking sequence is repeated. Each polytype has a number of Si-C bilayers stacked on top of each other and occupying different positions

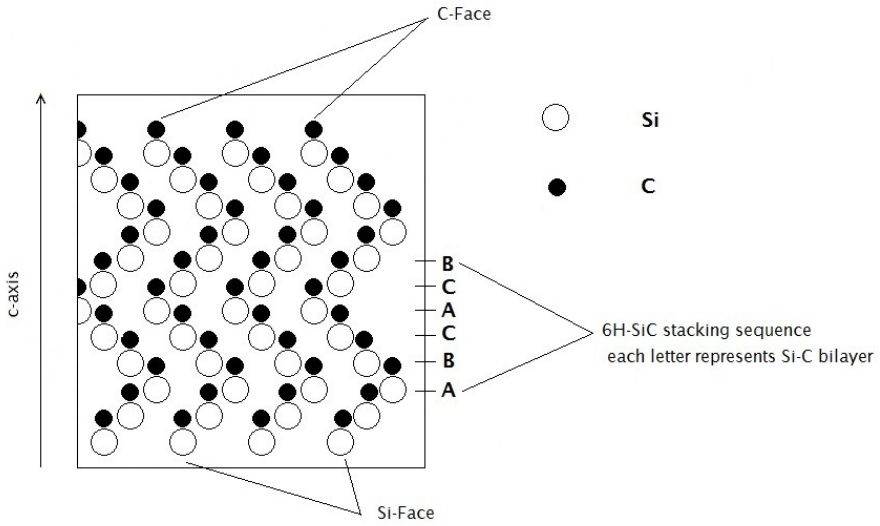


Figure 2.2: SiC polarity and 6H-SiC stacking order [not to scale].Source [15]

(denoted by letters: A, B and C) as shown in Fig. 2.3. These different positions can be achieved by a mutual rotation of 60 or $180^o$ of the bilayers. The letter in Ramsdell notation indicates the resulting crystal structure e.g. H for hexagonal, C for cubic and R for rhombohedral. Recognizable by naked eyes because of its color

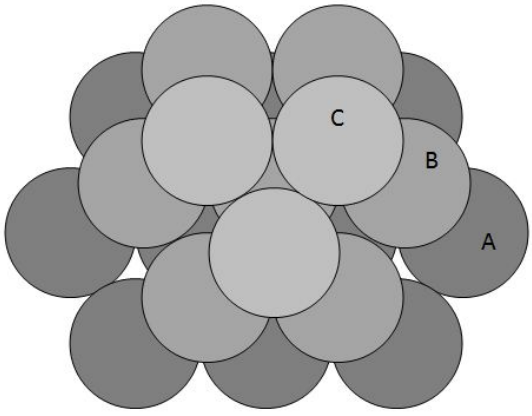


Figure 2.3: Stacking order of 3C-SiC. Source [10]

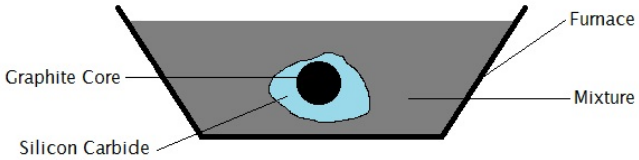


Figure 2.4: Acheson furnace [16].

(depending on the dopant species) each polytype of SiC comes with different carrier mobility and bandgap [10, 15].

## 2.3 SiC Bulk Growth Techniques

### 2.3.1 Acheson Process

Discovered by Edward Goodrich Acheson in 1885 for bulk production of SiC, to be used for abrasive and cutting applications, this process uses a mixture of silica, coke, small amounts of salt and saw dust to be heated in a furnace at very high temperatures for 7-10 days. After this time SiC crystals with areas of the order of 1 $cm^2$ are produced [10]. Acheson got patents of this process in 1896 and later designed a special furnace which used resistive heating. The cross-section of Acheson's furnace is shown in Fig. 2.4. In the center of the furnace there is a graphite core which can be heated by passing electric current. The graphite core is buried in the mixture of silica and coke with other ingredients. The hot graphite core initiates chemical reaction in the mixture and silicon carbide is produced in the form of layers over the graphite core alongside carbon monoxide as a by-product. There are four chemical reactions that take place during the Acheson process [16]:

- $C + SiO_2 \longrightarrow SiO + CO$
- $SiO_2 + CO \longrightarrow SiO + CO_2$
- $C + CO_2 \longrightarrow 2\,CO$

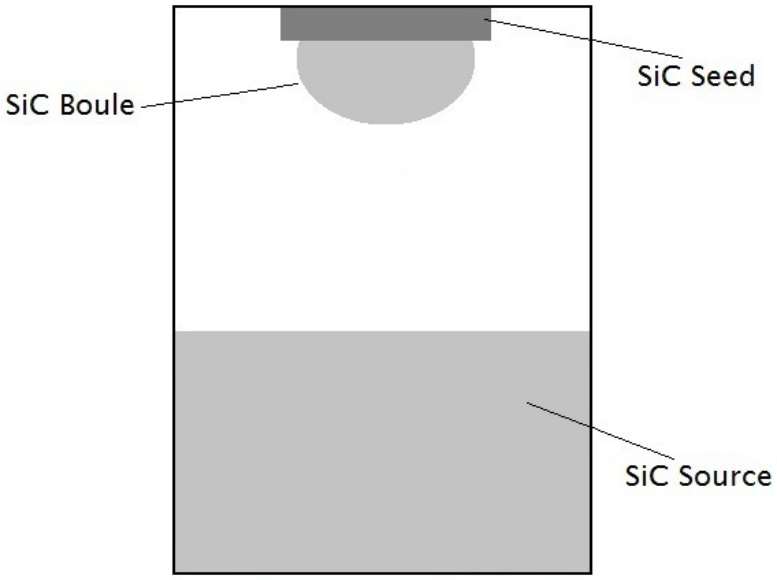


Figure 2.5: Seeded sublimation growth reactor. Source[15]

- $2\,C + SiO \longrightarrow SiC + CO$

### 2.3.2 Seeded Sublimation Growth Technique

Discovered by two Russian scientists Tairov and Tsvetkov in 1978 this technique is still used for the growth of SiC crystals and is also called modified Lely process. In this technique SiC powder is poured into a graphite crucible with a high quality seed connected to the lid of the crucible. The crucible is heated in an inert argon atmosphere up to 2200 $^oC$ temperature while the seed is kept at relatively low temperature so that after sublimation the vapors will condense at reaching the seed which should be at a distance from the SiC powder. The vapors found in the crucible include Si, $Si_2C$, $SiC_2$ and $Si_2$ [10, 15].

### 2.3.3 Liquid Phase Epitaxy

Liquid phase epitaxy (LPE) is a method to achieve SiC crystals from the Si and C melt. In LPE a high purity SiC seed crystal and Si-C melt are brought into contact inside a movable graphite crucible immersed into an argon filled reactor with high pressure lid

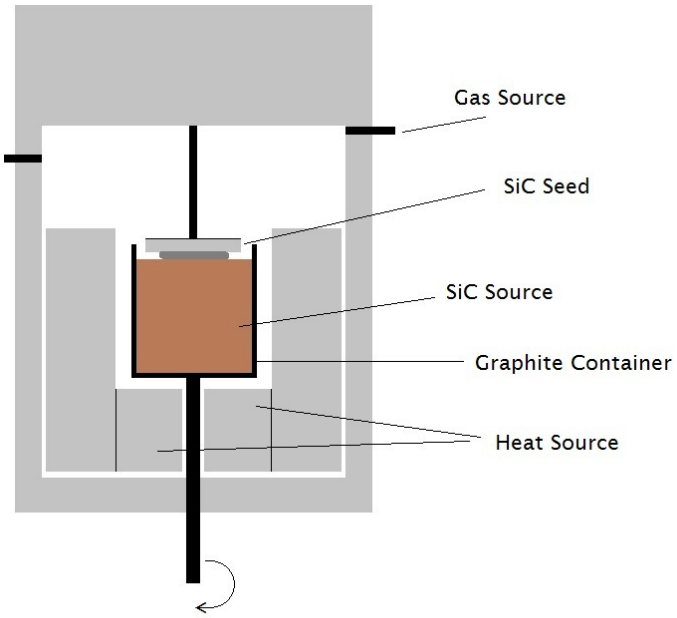


Figure 2.6: Liquid phase epitaxy reactor. Source[15]

and resistance heater. The crucible is rotated and SiC crystals can be achieved on the seed due to the cooling of the melt[15].

### 2.3.4 HTCVD

Discovered in 1995 HTCVD (high temperature chemical vapor deposition) is a three step process which uses gases (as silicon carbide source) which are injected into a vertical graphite reactor with seed resting at the top of the reactor interior. The gases containing C and Si such as silane and ethylene are first decomposed under high temperature into Si and $S_xC_y$ microparticles (Si may also form droplets depending on the temperature) which then are transported into the sublimation chamber filled with inert helium gas as a carrier. Here all the microparticles would sublime to Si, $SiC_2$ and $Si_2C$ vapors which would eventually condense on the relatively colder seed crystal [10, 15].

### 2.3.5 Comparison of SiC Bulk Growth Techniques

Of all the techniques discussed above seeded sublimation growth technique is the best because it is less expensive and faster (in terms of growth rate) than LPE or HTCVD. It gives a bigger SiC boule which can be cut into bigger SiC wafers after performing XRD analysis—for determining the crystallographic orientation[15].

## 2.4 SiC Epitaxial Growth

### 2.4.1 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a method which can be used for the growth of epitaxial layers over the semiconductor substrate due to its ability to grow high purity thin films. In CVD precursor gases are decomposed at high temperature and the required material is deposited over the wafer surface while unwanted by-products are pumped out of the CVD chamber [17]. For epitaxial growth of silicon carbide a mixture of precursor gases such as silane and hydrocarbons are heated to first decompose and then grow on the SiC substrate in the presence of hydrogen as a carrier gas. The precursor gases are heated (up to 1700 $^{o}$C) by means of a SiC coated graphite susceptor which is thermally insulated from the reactor and can be RF heated. For the homogeneity of epitaxial layer the substrate can be rotated and argon is normally added as another carrier gas. Many types of CVD reactors exist such as cold wall, hot wall and chimney-type reactors or horizontal, planetary and vertical reactors depending on the materials transport method used [10, 15].

### 2.4.2 SiC Epilayer Doping

Epilayer doping can be achieved by mixing nitrogen (for n-type doping) and trimethylaluminum (for p-type doping) with precursor gases during epitaxy for the most common dopant species i.e. nitrogen and aluminum. Phosphine ($PH_3$) and diborane ($B_2H_6$) can be used for less common dopant species such as phosphorus and boron. The doping concentration can be controlled by changing the silicon-carbon ratio (Si:C). This can easily be done by adjusting the amount of precursor gases [10, 15].

## 2.5 SiC Crystal Defects

### 2.5.1 Micropipes

Micropipes are hollow hexagonal cavities passing through silicon carbide wafers along c-axis. Their size may range from 1 to 100 $\mu$m and they can easily be observed under a microscope. Micropipes are the most intriguing of all the defects found in SiC, they can be formed when a large number of screw dislocations add up to form a big screw dislocation that can penetrate the wafer or during crystal growth when other particles come inside a growing crystal. A device fabricated over a micropipe cannot work and will result in failure [10, 15].

### 2.5.2 Comets

Comets or carrots are comet shaped objects penetrating whole epilayer. They are called comets because they resemble in shape to celestial objects also called comets with a head and diffuse tail. Comets can be formed when a microparticle moves during crystal growth over the growing surface [15].

### 2.5.3 Etch Pits

Etch pits have depths of a few hundred nanometers and diameters between 1 and 10 $\mu$m they can be formed when hydrogen ($H_2$) etches the SiC surface during epitaxial growth [15].

## 2.6 Applications of SiC Based Devices

Electronic devices based on SiC are suitable for high power and high frequency operations and due to better performance in power conversion and high switching speeds find applications in military, avionics, modern hybrid automobile power systems, uninterruptible power supplies, microwave and so on. Some of the major applications are discussed below.

### 2.6.1 Power Conversion

Major applications of SiC based electronic devices can be found in power conversion from DC-DC or from DC-AC. For switched mode DC-DC conversion, Schottky diodes are combined with inductors or

capacitors in a circuit to either step up the input power or to step it down. Inductor transfers its stored energy through Schottky diodes during power conversion. DC-DC conversion finds widespread applications in industrial and consumer electronics. DC-AC conversion, on the other hand, uses multiple diodes coupled with inductors which transfer their stored energy through these diodes. DC-AC power conversion finds applications mostly in uninterruptible power supplies and motor speed control [10].

### 2.6.2 SiC Devices As Gas Sensors

Schottky barrier diodes (SBD) and FETs based on SiC can detect some important gases such as oxygen, hydrogen, carbon monoxide and hydrocarbons. When thin metal film of SiC Schottky contact is exposed to gases e.g. hydrogen the current-voltage characteristics of the SBD are affected within a few milliseconds of the exposure. This occurs due to the fact that the Schottky barrier height of the SBD changes when the device comes in contact with some of the gases to which the SiC SBDs are sensitive. SiC gas sensors find applications in automobiles and aircrafts for detecting the fuel leakage and for detecting fires [18].

### 2.6.3 UV Detection

Silicon carbide Schottky barrier diodes (SBD) are able to detect ultra-violet radiation (UV) in a better way than Si based UV detectors because of SiCs wide bandgap. Because of wide bandgap SiC based SBDs are insensitive to radiation with frequencies below UV and can detect exclusively ultraviolet light even in the presence of visible and infrared light. Silicon based gas sensors however, are sensitive to visible and infrared light too and show poor performance in their presence unless additional radiation filtering is provided [18].

### 2.6.4 Microwave Applications

Superior material properties of silicon carbide are also exploited for microwave applications. Due to better RF and dc performance SiC based electronic devices are preferred over devices based on conventional semiconductors such as silicon or gallium-arsenide. Devices based on SiC exhibit much better microwave power at room temperature than their Si and GaAs counterparts [19]. Use of 4H-SiC in microwave technology can result in low cost, high power and smaller

sized devices with greater bandwidth control. For these reasons SiC MESFETs are being designed for continuous wave applications through X band and SiC static induction transistors (SIT), for high power pulsed transmitter technology, through L band operation [20].

## 2.7 Summary

This chapter was intended to be a brief introduction of the interesting world of silicon carbide as a semiconducting material so that, the reader may get some idea of the importance and potential of silicon carbide in power electronics. For further reading more detailed material should be referred (some links are provided in the end of this thesis[21, 22]). In the next chapter we will discuss metal and silicon carbide contacts together with their operation.

# Chapter 3

# Metal-Semiconductor Contacts

In this chapter metal-semiconductor contact formation mechanism and physics is covered. In the beginning a discussion is given about metal-semiconductor contacts in general followed by a discussion on metal-SiC contacts in the latter half of the chapter.

## 3.1 Metal - Semiconductor Contacts

When a metal and a semiconductor are brought into contact a depletion region forms between them. The width of this depletion region depends on the semiconductor doping level and determines the type of the contact that has formed. If the depletion region is narrow an ohmic contact has formed and if the depletion region is wide a Schottky contact has formed. Both metal and semiconductor are carefully chosen keeping in mind their work-functions. If the metal work-function $\phi_m$ is greater than the work-function of semiconductor ($\phi_s$), electrons will flow from semiconductor to metal giving rise to space charge or depletion region over a width W in case of n-type semiconductor—energy band diagram can be seen in Fig. 3.1. Electrons will stop flowing once the metal and semiconductor are at thermodynamic equilibrium and both have reached the same Fermi level. After the establishment of depletion region electrons in the metal will experience a barrier in traveling to semiconductor [23]. This barrier is known as Schottky barrier ($\Phi_B^0$) and is given by:

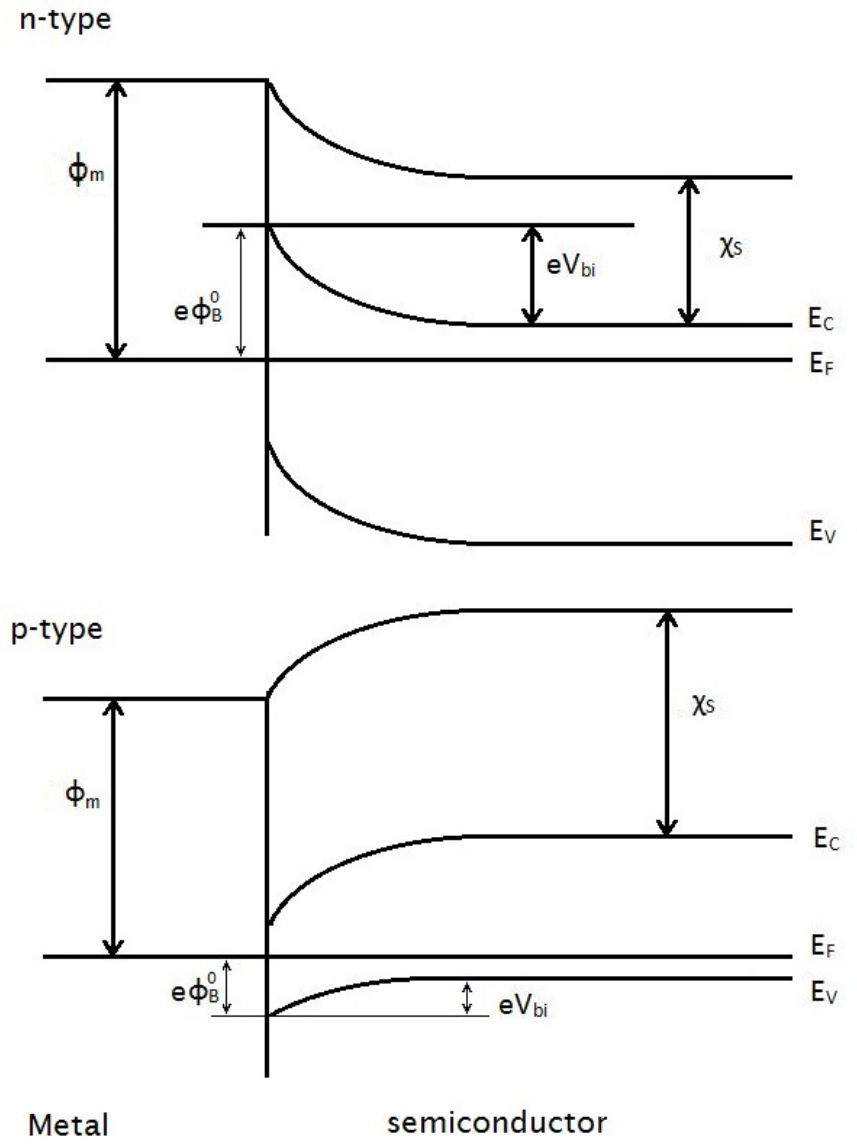


Figure 3.1: Energy band diagram of metal-semiconductor contact. Source [18]

$$e\Phi_B^0 = \phi_m - \chi_s \tag{3.1}$$

$\chi_s$ in equation 3.1 is known as electron affinity of the semiconductor. The barrier for electrons traveling from semiconductor to metal is called built-in potential ($V_{bi}$) and in the absence of applied bias is given by [3]:

$$eV_{bi} = e\Phi_B^0 - eV_N \tag{3.2}$$

in Eq. 3.2 $V_N$ is known as conduction band minimum and $e$ is the elementary charge. The amount of current passing through Schottky contact can be calculated by thermionic emission theory which relates the current I to applied voltage $V_a$ as follows:

$$I = AA^* exp\left(\frac{-e\Phi_B}{k_B T}\right)\left[exp\left(\frac{eV_a}{k_B T}\right) - 1\right] \tag{3.3}$$

$k_B$ in Eq. 3.3 represents Boltzmann's constant, T applied temperature, A area of the contact and $A^*$ Richardson's constant and $\Phi_B$ is the Schottky barrier height after considering the image force lowering of the Schottky barrier height[23]. In an ideal situation an ohmic contact can be formed if $\phi_m < \phi_s$ and electrons flow from metal to (n-type) semiconductor leaving behind lowered energy levels at the metal-semiconductor interface. But practically this seems impossible because almost all the metals have work-function values higher than those of the semiconductor work-functions' (especially for wide bandgap semiconductors). In this situation an ohmic contact can be achieved by increasing the doping level of the semiconductor ($N_D > 10^{19}$ cm$^{-3}$) so that the width of depletion region can be decreased making possible for electrons to tunnel through the relatively narrow barrier. This type of ohmic contact is known as tunnel ohmic contact and the tunneling mechanism is governed by field emission—not to be confused with *thermionic field emission* which occurs when charge carriers do not have sufficient thermal energy to surmount the barrier and they tunnel through the barrier where it is narrow enough. Thermionic field emission occurs at relatively light doping ($10^{17}$ - $10^{19}$ cm$^{-3}$) and is intermediate between field emission and thermionic emission [23].

## 3.2 Specific Contact Resistance

Before discussing metal-SiC contacts a very important quantity need be mentioned which will often be quoted in the rest of the thesis and that is specific contact resistance $\rho_c$. Specific contact resistance is the measure of the resistivity of a metal-semiconductor contact. It is very useful when comparison (in terms of contact resistance) between two contacts of unequal sizes is required because it is independent of the dimensions of the contact. Specific contact resistance is equal to the product of contact resistance and the surface area of the contact. The contact resistance is not independent of the area of the contact and its value can be influenced by metal barrier height and the processing techniques [23]. Specific contact resistance can be expressed in many ways depending on the dominant current transport mechanism but in general it is given by [23]:

$$\rho_c = \left(\frac{\partial J}{\partial V_a}\right)^{-1}_{V_a=0} \tag{3.4}$$

J in Eq. 3.4 represents current density and $V_a$ is the applied voltage. If thermionic emission is the dominant current transport mechanism, $\rho_c$ can be expressed as follows:

$$\rho_c = \frac{k_B}{eA^*T} exp\left(\frac{e\Phi_B}{k_BT}\right) \tag{3.5}$$

Due to light doping required for thermionic emission $\rho_c$ is independent of the doping density unlike tunneling current transport which occurs when the semiconductor is heavily doped and $\rho_c$ is dependent on doping density N as given below:

$$\rho_c \propto exp\left(\frac{\Phi_B}{\sqrt{N}}\right) \tag{3.6}$$

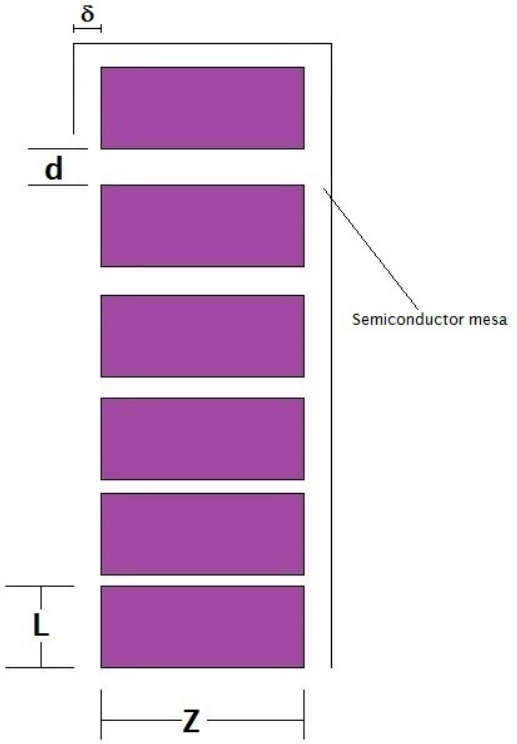


Figure 3.2: Configuration of contacts according to TLM method—not to scale. Source[23, 24].

and for thermionic field emission specific contact resistance is given by:

$$\rho_c \propto exp \frac{\Phi_B}{E_{00} \coth\left(\frac{E_{00}}{k_B T}\right)} \tag{3.7}$$

The measurement of contact resistance can be done through transmission line model (TLM) which uses a number of rectangular pads with similar dimensions. These pads are achieved by metal deposition over the semiconductor as shown in Fig. 3.2 [24]. If the pads have length $L$ and width $Z$ with $d$ representing spacing between two adjacent pads then the resistance $R_T$ between two adjacent pads is given by:

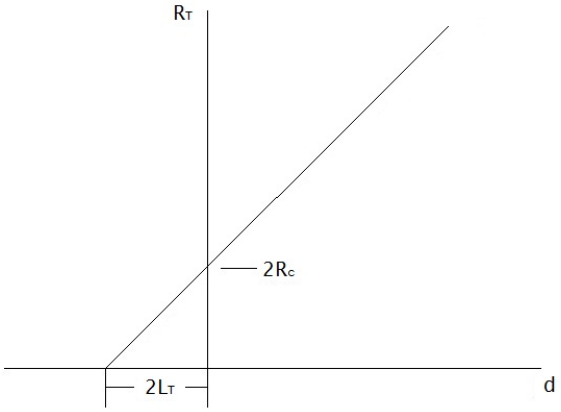


Figure 3.3: Typical $R_T$ versus d plot. Source [25]

$$R_T = 2R_c + \left(\frac{R_{SH}}{Z}\right) d \tag{3.8}$$

$R_{SH}$ in Eq. 3.8 is the semiconductor sheet resistance; $R_c$ is the contact resistance of the pads. The pads are deposited on a semiconductor mesa with $Z + 2\delta$ width. It is important to note that Eq. 3.8 considers $\delta << Z$. The specific contact resistance $\rho_c$ can be obtained from $R_c$ as:

$$\rho_c = R_c Z L_T \tanh\left(\frac{L}{L_T}\right) \tag{3.9}$$

$L_T$ in Eq. 3.9 is the transfer length which means the distance from contact edge to where the current density becomes equal to 1/e of the original value. Transfer length can be extracted from x-intercept of $R_T$ vs. $d$ plot as shown in Fig. 3.3 [25].

## 3.3 Metal-SiC Contacts

Various metals are used for the formation of Schottky as well as ohmic contacts to silicon carbide. Normally different metals are chosen for n-type and p-type silicon carbide. Schottky contacts with

high values of Schottky barrier height and low values of ideality factor are preferred while ohmic contacts with low *specific contact resistance* values are preferred. Achieving low *specific contact resistance* ohmic contacts to SiC has been a challenge throughout the history of SiC in electronics. In the beginning ohmic contacts were formed and tested on 6H-SiC due to its low cost but as SiC growth technology advanced and high carrier mobility 4H-SiC wafers became available it is now common to see works reporting on fabrication of ohmic contacts on 4H-SiC with considerably low specific contact resistance values ($\rho_c$). Nowadays achieving low $\rho_c$ ohmic contacts to SiC is an active area of research and many materials are being tested for low cost and better performance [23].

### 3.3.1 Ohmic Contacts to n-type SiC

Chromium and tungsten were among the earliest materials used for ohmic contact fabrication to n-type 6H-SiC. These days a range of materials is used to fabricate low $\rho_c$ ohmic contacts to n-type SiC. Some of the materials are listed in Table 3.1. Aluminum and molybdenum can also form low $\rho_c$ ohmic contacts to n-type SiC without the need of annealing treatment after the deposition and, at some time, were considered fit for the fabrication of devices based on SiC but soon after the realization that Mo and Al show negative reaction to wet etching they were replaced with Ni and Ti [23].

Titanium forms high $\rho_c$ ohmic contacts to n-type SiC without post deposition annealing and forms low $\rho_c$ ohmic contacts after annealing at temperature exceeding 900 $^o$C. Annealing done at temperatures below 900 $^o$C results in a Schottky contact probably because of the absence of $Ti_3SiC_2$ which is commonly found after annealing at temperatures exceeding 900 $^o$C. The specific contact resistance values reported for annealing treatment performed at 950 $^o$C and 1000 $^o$C are 1 x $10^{-4}$ $\Omega$ cm$^2$ and 6.7 x $10^{-5}$ $\Omega$ cm$^2$ respectively [23].

Nickel has been studied more than any other metal for ohmic contacts to n-type SiC. Just like titanium, Ni forms a Schottky contact on n-type SiC, if not annealed, with Schottky barrier height values depending on SiC surface treatment performed before depositing nickel. Ni shows Schottky behavior even after annealing at 600 $^o$C while annealing at 950 $^o$C results in the formation of ohmic contact with specific contact resistance of 3.9 x $10^{-5}$ $\Omega$ cm$^2$ (for intermediate doping density). Reaction of Ni with SiC is reported at annealing temperatures of 500 $^o$C and above. The most common phase detected after high temperature annealing treatment is $Ni_2Si$ [23].

| **Metal** | **Ann. T ($^o$C)** | **N$_D$** (cm$^{-3}$) | $\rho_c$ ($10^{-6}\Omega$ cm$^2$) | Ref. |
|---|---|---|---|---|
| Al | none | $>10^{20}$ | 0.54-1.2 | [26, 27] |
| Mo | none | $>10^{20}$ | 2 | [27] |
| Ti | none | $>10^{20}$ | 0.27 | [27] |
| Ni | none | $>10^{20}$ | 3 | [27] |
| Co/Si/Co | 500, 5 min + 800, 2 min. | 1.1 x $10^{18}$ | 1.8 | [28] |
| Ti/$TaSi_2$/Pt | 600, 30 min | 2 x $10^{17}$ | 470 | [29] |
| Si/Ni | 900, 10 min | 2 x $10^{19}$ | 1.9 | [30] |
| Ni | 950, 10 min | 1 x $10^{19}$ | 2.8 | [31] |
| TiC | 950, 2 min | 1.3 x $10^{19}$ | 40.1 | [32] |
| Ni/Si | 950, 10 min | 1 x $10^{19}$ | 27 | [31] |
| Al/Ni | 1000 | 2x$10^{20}$ | 48 | [33] |
| Ni | 1000, 1 min | 4.2 x $10^{15}$ | 28 | [34] |
| Ni | 1000, 2 min | $>10^{20}$ | 1.2 | [35] |
| Nb | 1100, 10 min | 1.3 x $10^{19}$ | <1 | [36] |
| NiCr | 1100, 3 min | 1.3 x $10^{19}$ | 12 | [37] |

Table 3.1: Ohmic contacts to n-type 4H-SiC. Source [23]

### 3.3.2 Ohmic Contacts to p-type SiC

A good number of materials is used for the formation of ohmic contacts to n-type SiC but the choice is limited for p-type SiC because large forbidden energy bandgap (2.8-3.2 eV) and electron affinity values around 4.0 eV combined with wide energy bandgap of SiC make it difficult to achieve low Schottky barrier height required for ohmic contact formation. The most common materials used for the formation of ohmic contact to p-type SiC is the double layer Al/Ti metallization. Al/Ti shows ohmic contact behavior after annealing treatment at temperatures exceeding 900 $^o$C. Low specific contact resistance (1.5 x $10^{-5}\Omega$ cm$^2$) ohmic contacts can be achieved after annealing at 1000 $^o$C as reported by Crofton et al. with doping level of 2 x $10^{19}$ cm$^{-3}$[47]. In case of Al/Ti ohmic contact some authors have reported dependence of specific contact resistance on doping level of SiC and structural composition of Al/Ti alloy. Table 3.2 shows some of the materials used for ohmic contacts to p-type 4H-SiC [23].

| **Metal** | **Ann. T ($^o$C)** | **N$_A$** ($10^{18}$cm$^{-3}$) | $\rho_c$ ($10^{-5}\Omega$ cm$^2$) | **Ref.** |
|---|---|---|---|---|
| Al | 1000, 2 min | 4.8 | 42 | [38, 39] |
| Al/Ni | 1000, 2 min | 700 | 52 | [33] |
| Al/Ti | 900, 3 min | 10 | 64 | [40] |
| CoAl | 900, 5 min | 9 | 40 | [41] |
| Ge/Ti/Al | 600 | 4.5 | 10 | [42] |
| Ni | 1000, 2 min | 200 | 7 | [35] |
| Ni/Al | 1000, 5-30 min | 3-9 | 9.5 | [43] |
| Ni/Ti/Al | 800, 5-30 min | 3-9 | 6.6 | [43] |
| Pd | 700,5-40 min | 50 | 55 | [44] |
| Ti | None | 13 | 34.4 | [32] |
| Ti | 950, 2 min | 13 | 77 | [32] |
| Ti/Si/Co | 500,5 min+ 800, 1 min | 3.9 | 40 | [45] |
| TiC | 500,3 min | 20 | 2 | [46] |

Table 3.2: Ohmic contacts to p-type 4H-SiC. Source [23]

### 3.3.3 SiC Schottky Contacts

A lot of research has been done in order to understand the formation and behavior of Schottky contacts to silicon carbide using various metals. Schottky barrier heights of some metals for p-type SiC are given in Table 3.3 and for n-type SiC are given in Table 3.4. Schottky barrier height (SBH) value is different for different metals due to different metal work-functions. Moreover SBH value depends on a number of conditions such as chemical reactions taking place in metal-semiconductor interface may affect the SBH value. Semiconductor surface conditions can change the quality of the Schottky contact and the value of the SBH[18].

SBH is also sensitive to annealing temperature for example in the case of platinum Schottky contact to 6H-SiC, it is reported that the annealing treatment performed at temperatures exceeding 600 $^o$C raises the value of SBH . An increase from 0.45 eV to 1.35 eV was observed after annealing at 900 $^o$C. This occurs due to the presence of platinum silicide found after annealing treatments of above 600 $^o$C. The SBH is also found to depend on the doping level of SiC. For example it is reported that SBH is lowered if donor concentration reaches above 2 x $10^{17}$ cm$^{-3}$ and acceptor concentration reaches

| **Metal** | **SBH (eV)** | **Ideality Factor** | **Polytype** | **Ref.** |
|---|---|---|---|---|
| Al | 1.23 | 2.18 | 6H | [48] |
| Cu | 1.22 | 1.01 | 6H | [48] |
| Au | 1.18 | 1.51 | 6H | [48] |
| Ti | 1.94 | 1.07 | 4H | [49] |
| Au | 1.35 | 1.49 | 4H | [49] |
| Ni | 1.43 | 1.29 | 4H | [50] |

Table 3.3: Schottky contacts to p-type SiC. Source [18]

| **Metal** | **SBH (eV)** | **Ideality Factor** | **Polytype** | **Ref.** |
|---|---|---|---|---|
| Ti | 0.8 | 1.15 | 4H | [51] |
| Ti/Au/Pt/Ti | 1.17 | 1.09 | 4H | [52] |
| TiW | 1.22 | 1.05 | 4H | [53] |
| $Ni_2Si$ | 1.4 | <1.1 | 4H | [54] |
| Cu | 1.6 | <1.1 | 4H | [55] |
| Au | 1.73 | 1.02 | 4H | [56] |
| Ni | 1.59 | 1.05 | 4H | [57] |
| Ni | 1.63 | 1.1 | 4H | [58] |
| Pt | 1.39 | 1.01 | 4H | [57] |
| Mg | 0.69 | 1.3 | 6H | [59] |
| Mn | 0.79 | 0.96 | 6H | [60] |
| Al | 0.25 | 1.6 | 6H | [61] |
| Ti | 0.85 | <1.1 | 6H | [62] |
| Ti | 1.03 | 1.08 | 6H | [63] |
| Au | 1.12 | 1.15 | 6H | [64] |
| Ni | 1.39 | 1.02 | 6H | [65] |

Table 3.4: Schottky contacts to n-type SiC. Source [18]

above 1 x $10^{18}$ $cm^{-3}$. Dependence of SBH on temperature is reported in [66]. The SBH of n-type SiC tends to decrease and that of p-type SiC tends to increase as the temperature increases[18].

**Schottky Diode Operation**

At zero bias no current flows in the Schottky diode. The metal and semiconductor are at thermal equilibrium and depletion region exists between metal and semiconductor after the initial charge flow has stopped. The metal has negative charge and the (n-type) semiconductor has positive charge.

Under forward bias there is net current flowing through the diode due to electron transport from (n-type) semiconductor to metal because of the lowering of potential barrier. This current is given by:

$$I = I_S \left[ exp\left( \frac{eV_a - eIR_S}{nk_BT} \right) - 1 \right] \tag{3.10}$$

Where $Rs$ is the series resistance, n is the ideality factor which is usually between 1.0 and 2.0 and $I_S$ represents saturation current and is given by:

$$I_S = AA^*T^2 exp\left( \frac{-e\Phi_B}{k_BT} \right) \tag{3.11}$$

Where $\Phi_B$ is Schottky barrier height, A is the area of the diode, T is the temperature, $k_B$ is Boltzmann's constant and A* is the Richardson constant which can be calculated as follows:

$$A^* = \frac{4\pi e m^* k_B^2}{h^3} \tag{3.12}$$

$m^*$ is the effective mass[67]. Under reverse bias no electrons can flow from semiconductor to the metal due to the large difference between Fermi level of semiconductor and the top of the potential barrier. Electrons flow from metal to the semiconductor because Fermi level of the metal and the top of the potential barrier are at nearly the same height. The reverse saturation current of the diode is made up of such electrons whose number depends on the effective

density of states of the conduction band, $Nc$, which can be written as [68, 69]:

$$N_C = 2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{3/2} \tag{3.13}$$

Where $m_e^*$ is the effective mass for electrons[70].

## 3.4 Summary

In this chapter basic physics of metal-semiconductor contacts was discussed. Starting from a general discussion about metal and semiconductor contacts and their types in general the focus is moved to more specific metal-silicon carbide contacts. Two types of metal-SiC contacts were discussed: Schottky and ohmic. Generally accepted values of specific contact resistance and Schottky barrier height for both types of contacts are summarized in tables: 3.1, 3.2, 3.3 and 3.4. Specific contact resistance is also discussed briefly, with important results reported in the above mentioned tables. The value of specific contact resistance strongly depends on the processing techniques used for the device fabrication which will be discussed in the next chapter.

# Chapter 4

# SiC Process Technology

In this chapter we will describe the processing steps required to fabricate a Schottky barrier diode using 4H silicon carbide as a semiconductor material. SiC based Schottky barrier diode is the simplest structure to fabricate and serves as building block for more complicated structures such as MOSFETs, MESFETs, JFETs and etc.

## 4.1 Device Design

Named after a German scientist Walter H. Schottky, a Schottky barrier diode is a metal-semiconductor junction with highly rectifying properties unlike a p-n junction diode which is made up of semiconductor-semiconductor junction. It has a very low forward voltage drop as compared to a p-n junction diode and it is a unipolar device because it lacks minority charge carriers. Schottky diodes have been in use for a long time but in the last decade they have got much popularity and importance due to their better performance in power electronic applications [71].

Early Schottky barrier diodes were point-contact Schottky diodes which can be made by bringing a metal wire close to a semiconductor surface. Early cat's whisker detectors are good example of such Schottky diodes. These point contacts were replaced by metal deposited Schottky contacts because they couldn't continue operation until the wire would be placed at some other point on the semiconductor surface. Modern Schottky contacts are fabricated by metal-deposition on the semiconductor epilayer surface in vacuum. The epilayer is relatively thinner as compared to the bulk semiconductor substrate underneath; both the epilayer and the bulk have different

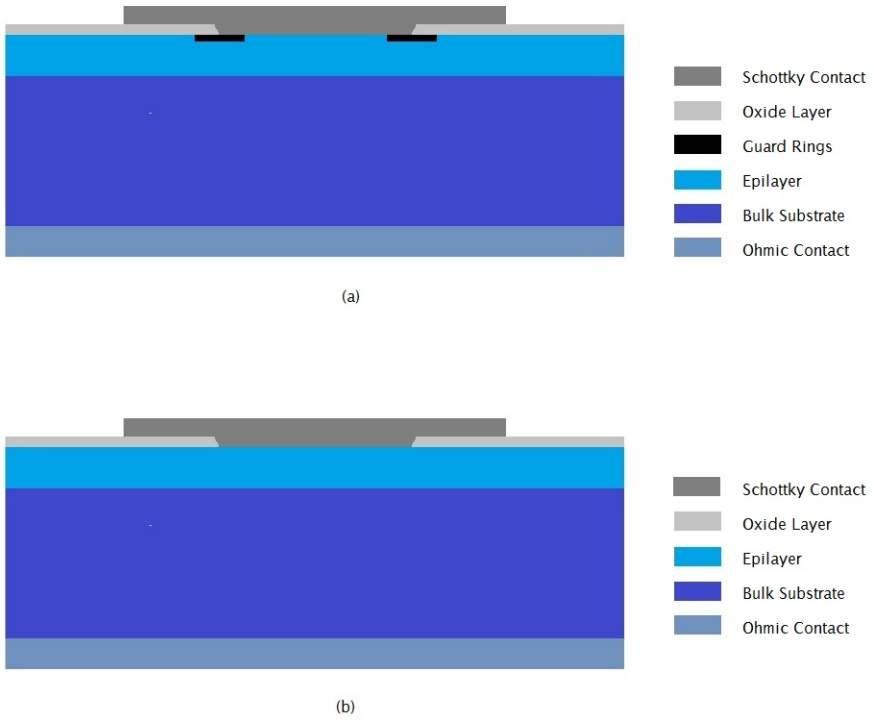


Figure 4.1: Schottky diode structure [not to scale]: (a) with guard rings (b) without guard rings. [15]

doping concentrations [71, 72].

Silicon carbide Schottky diode consists of a Schottky contact, ohmic contact, oxide layers and guard rings for minimizing the reverse leakage current. Schottky contact can be achieved on the front side of the SiC wafer and directly over the epilayer surface. Ohmic contact is deposited on the wafer's back side. An oxide layer is grown on the remaining epilayer surface and the guard ring is implanted underneath epilayer surface where the depletion region ends as shown in Fig. 4.1.

The semiconductor here is n-type with $p^+$-type guard ring structure which is needed to avoid Schottky diode breakdown around the edges of the Schottky contact, due to the presence of high electric fields. The guard ring can be fabricated by either diffusion or ion implantation of the metal ions along with an oxide layer near the Schottky contact edges. The guard ring is important because it can protect the Schottky contact from damage (due to the passage of large amounts of reverse current).

An ohmic contact is needed to transport device current out of the diode. Ohmic contact is achieved on the back side of the semiconductor wafer directly over bulk substrate by metal deposition often followed by annealing treatment. Different metals are used for Schottky and ohmic contacts depending upon the metal work-functions. A good ohmic contact must be non-rectifying having virtually no potential barrier between metal and semiconductor with contact resistance, as low as possible [68].

## 4.2 Process Techniques

### 4.2.1 Wafer Cleaning

Semiconductor wafer must be cleaned before starting the fabrication process. For thorough cleaning of the wafer surface a sacrificial oxide layer can be grown by either thermal oxidation or PECVD. Once grown oxide layer must be removed to get the neat semiconductor surface. For removing the oxide layer from the surface the SiC wafers are dipped into hydro-fluoric acid solution intermixed with water [15].

### 4.2.2 Thermal Oxidation

For thermal oxidation silicon carbide wafers are heated in a quartz tube filled with oxygen over a temperature range of 900—1200 $^{o}$C. The wafers must be inserted vertically into the center of the furnace. This type of oxidation is known as dry oxidation and is performed very often. Another thermal oxidation method also exists which is called wet oxidation because it uses water, as the source of oxygen, and argon or nitrogen as carrier gases. The temperature range for wet oxidation is the same as for dry oxidation and the time required to complete the oxidation depends on the temperature in the furnace and wafer orientation for both types of thermal oxidations [15, 73]. For controlled growth of oxide film over the semiconductor surface plasma enhanced chemical vapor deposition (PECVD) is used. In PECVD SiC wafers are inserted into the reactor chamber filled with reactive gases such as $SiH_4$, $CO_2$ or $H_2$. Remote PECVD is used to perform in situ plasma cleaning of the SiC wafer before metal deposition and thereby, avoiding thermal oxidation step altogether [74].

### 4.2.3 Photo-lithography

Photolithography is a process by which patterning of electronic devices is performed through a photo-mask placed over an ultraviolet-sensitive chemical photo-resist deposited upon a semiconductor substrate, in a clean-room environment. Through photolithography it is possible to shape the pattern on the substrate or to open areas for further treatment. Photolithography can create very sophisticated and small patterns cost-effectively [75].

Before performing photolithography the wafer must be cleaned in order to make sure that there are no any organic or inorganic contaminants over the wafer surface. This is done by RCA cleaning method which uses solutions such as:
$H_2O$:$H_2O_2$:$NH_4OH$ with 5:1:1 ratio and $H_2O$:$H_2O_2$:HCl with 6:1:1 ratio [15].

After cleaning the wafer a few drops of photo-resist are placed on the wafer surface (mounted on a spinner). High speed spinning is applied with 1200 to 4800 rpm for up to 1 minute time in order to achieve a uniform, flat and thin photo-resist layer with no any bumps on the surface. After that a hotplate prebake is applied with temperatures ranging from 90 to 100 $^oC$ for up to 1 minute time, to drive off solvents [73].

After the prebake the wafer is ready for exposure to ultraviolet light through a specially prepared photo-mask which blocks UV light to some regions and allows to other regions for creating a pattern. The pattern's shape would depend on the type of photo-resist applied before prebake. Two types of photo-resists exist: positive and negative. Positive photo-resist can be removed after exposure to UV light and the negative photo-resist can be removed on the regions where the ultra-violet light was not allowed to cause any chemical change in the photo-resist. The most commonly used photo-resist is the positive one due to the possibility of achieving small and better patterns by using it [75].

After that the wafer is applied a hard-bake to achieve a better adhesion of the remaining photo-resist at temperatures ranging from 120 to 140 $^oC$ for 20 to 30 minutes, if using an oven. After hard-bake is complete the chemical etch is applied in order to remove the uppermost layer over the areas which were not protected by the photo-resist. Finally the photo-resist is entirely removed from the wafer because it's no more needed. This step is performed by using chemical solutions that change the photo-resist so that it is stripped away. Photo-resist can also be removed by ashing which oxidizes the photo-resist by plasma (containing oxygen gas) [15, 73, 74, 75].

### 4.2.4 ICP Etching

Inductively coupled plasma (ICP) is used to remove small mass of silicon carbide wafer surface prior to performing ion implantation. It is a dry etch technique which uses a number of reactive gases for selective removal of regions from SiC substrate. ICP reactor consists of a plasma chamber (made of dielectric material) surrounded by an inductive coil and powered by an RF source. Plasma is generated by inducing magnetic field in the center of the chamber. The plasma moves towards the substrate in the presence of electric and magnetic fields at a pressure below 20 mTorr and ions are adsorbed on the wafer surface. As a result of chemical reaction between ions and SiC, gaseous by-products are formed which after desorption are pumped out of the chamber. This type of etching is known as reactive ion etching (RIE) and uses oscillating electric field to ionize gas molecules. The electrons absorbing in the chamber walls are fed to the ground in order to keep the system electrically stable. The DC isolated wafer platter gets positive charge by loosing electrons and the plasma develops negative charge (due to the presence of negative ions) resulting in ions' drift towards the wafer [15, 74, 76, 77, 78].

### 4.2.5 Ion Implantation

Silicon carbide selective doping is performed by ion implantation and diffusion. Due to good control over doping concentration and low temperature needed during doping process, ion implantation is widely used instead of diffusion which requires very high temperatures and has low diffusion coefficient. Selective doping of SiC can be done through ion implantation by masking areas over the wafer surface which need not be doped. The masking can be done by deposition of high mass metals such as gold or an oxide layer. The mask thickness must be carefully chosen, keeping in mind the range of ions to be implanted so that they should not reach the underlying areas and the mask must not be made of the element species which are used for silicon carbide doping[15, 73].

For implantation the ions are accelerated at energies ranging from 1 KeV to 1 MeV for achieving implant depths of 500 Å to 1 $\mu$m. Implanted ions occupy interstitial lattice positions in SiC together with Si and C atoms which are displaced from their respective lattice position due to ion implantation. Ion implantation does not change the electrical properties of SiC though; crystal structure may change depending on the doping level. For re-crystallization of material and activation of implanted ions the annealing is required. Annealing at

high temperature can induce a competition between implanted ions and the native species for vacant lattice sites. The atoms become active after occupying lattice sites [74].

The annealing temperature can be as high as 2000 $^{o}$C at atmospheric pressure in the presence of inert argon gas. High temperature used for post-implantation annealing can be harmful for the mask therefore; sometimes it's useful to perform ion implantation in hot environment with temperature ranging from 500 $^{o}$C to 1000 $^{o}$C. This can help immediate re-crystallization of the SiC crystals. Normally both techniques are combined to achieve fast crystal recovery and damage reduction [15, 73, 74].

### 4.2.6 Metal Deposition

Thin metal films are important for the fabrication of Schottky and ohmic contacts. The most commonly used metals are listed in table 4.1. There exist different methods for deposition of metals over the SiC wafer surface. The most common technique is the electron beam physical vapor deposition (EBPVD). In EBPVD a metal source is bombarded with electrons, traveling in beam (generated by heating tungsten filament in high vacuum), and is partially converted into gas phase (from the solid metal source). The atoms (in the gas phase) of the metal solidify after touching the colder wafer surface. The wafers are loaded into the vacuum chamber. The number of wafers that could be loaded into the chamber depends on the evaporator type for example it is possible to load 48 wafers at a time into an ULVAC EBX-14D E-beam evaporator placed in $\chi$-Lab. This particular evaporator comes with a cryogenic pump that can generate a pressure of $10^{-8}$ mTorr, with the possibility to perform four layer metallization without disturbing the vacuum [15, 73, 79].

### 4.2.7 Amorphous Si and Polyimide Deposition

While operating under reverse bias silicon carbide Schottky barrier diodes exhibit high leakage current. To avoid high leakage currents it is better to insulate the structures on the SiC wafer. For this purpose a passivation layer of amorphous silicon or polyimide is grown over the devices and annealed later on. Amorphous silicon growth could be done using a low pressure chemical vapor deposition (LPCVD) reactor[15].

Polyimide materials can also be used for insulation of the structures due to their ability to retain chemical resistance, tensile strength

| **Metal** | **Melting Point** ($^oC$) | **Deposition Rate** (nm/s) |
|---|---|---|
| Nickel | 1453 | 0.2-0.5 |
| Titanium | 1660 | 0.2-0.3 |
| Aluminum | 660.37 | 1-3 |
| Silver | 961.93 | 3-4 |
| Copper | 1083 | 1-2 |
| Molybdenum | 2617 | 0.1 |

Table 4.1: Various metals used for SiC based electronic devices. Source [15, 80]

and their good mechanical properties at high temperatures. Polyimide film deposition over the device structures results in better adhesion between metal and polyimide layers. The commonly used polyimide materials are PMDA,BPDA, and TFMOB[81, 82].

### 4.2.8 Wet Chemical Etching

Wet chemical etching is required to remove unwanted parts of the metal layers or amorphous silicon. Various chemical solutions are required for etching, the choice of etchant depends on the deposited material to be etched, some of the most commonly deposited materials such as Al, Cu, Ti, Ni, Si and their etchants are discussed below.

Aluminum and copper can be etched by heating in a mixture of nitric acid, phosphoric acid, acetic acid and de-ionized water at temperature ranging from 60 to 80 $^o$C. Oxidation occurs when nitric acid reacts with metals forming oxides which are then etched away by phosphoric acid. The time required to remove 1 $\mu$m thick layer of aluminum (deposited by EBPVD) is 2 minutes and for the copper less than a minute is required to etch. A commercially available E6 solution may also be used with the following composition : 80% $H_3PO_4$; 5% $HNO_3$; 5% $CH_3COOH$ and 10% de-ionized water[15].

Titanium can be etched at room temperature using a mixture of hydrogen peroxide and hydrofluoric acid in equal amounts with de-ionized water. Hydrogen peroxide ($H_2O_2$) can oxidize Ti by reacting and resulting in titanium oxide which is then etched away by hydrofluoric acid (HF). The exact composition of the etchant chemical solution is as follows: HF:$H_2O_2$:$H_2O$ with 1:1:100 ratio[15].

Nickel etching can be performed very rapidly (0.5 $\mu$m thick layer in 1 minute) in a mixture of copper sulphate, chloridic acid, methanol

and de-ionized water. Amorphous silicon is usually oxidized by reaction with nitric acid to form $SiO_2$ which can easily be etched by hydrofluoric acid [15].

### 4.2.9 Annealing

Annealing involves heating semiconductor wafers to a certain temperature for some time in controlled atmosphere and then allowing them to cool down. Annealing is often used to alter electrical properties of a semiconductor such as annealing performed after doping so that the dopant species can diffuse well and become active after re-crystallization of the semiconductor material. Annealing is also done after ohmic or Schottky contact deposition in order to improve some electrical properties [83].

## 4.3 Summary

In this chapter important process steps were discussed. Beginning from wafer cleaning and photolithography wet and dry etching techniques are also touched. Ion implantation and metal deposition are mentioned briefly and in the end a short description of annealing step is also given. All these steps are necessary to fabricate devices which after cutting and packaging are characterized for further analysis.

# Chapter 5

# Characterization Techniques for 4H-SiC

For the analysis of power electronic devices various characterization techniques are needed some of them are applied before fabrication and some after. Silicon carbide wafers must be analyzed thoroughly for any surface defects prior to device design so that the structures do not come over any defect and end in failure. After the fabrication, devices are analyzed for chemical and structural changes in order to understand the metal-semiconductor interface. Electrical characterization is performed to analyze and optimize the device performance. In this chapter a brief introduction will be presented, to some of the commonly used characterization techniques such as: X-ray diffraction, Raman spectroscopy and current-voltage measurement.

## 5.1 X-Ray Diffraction Spectroscopy

X-ray diffraction is used to investigate materials for chemical composition, physical properties and crystal structure. Almost 95% solids have well defined crystal structure with atoms arranged in planes at fixed lattice sites in the crystal (other 5% include amorphous solids like glasses). There is a fixed inter-planar distance $d$ between any two adjacent planes in the crystal called d-spacing. When x-rays are directed to any crystal both destructive and constructive interference occurs. Constructive interference occurs if the reflected rays are in phase and maximum beam intensity is observed. Incident x-ray beam makes an angle $\theta$ with lattice planes and the reflected rays make an angle $2\theta$ with lattice planes. Beam intensities can be

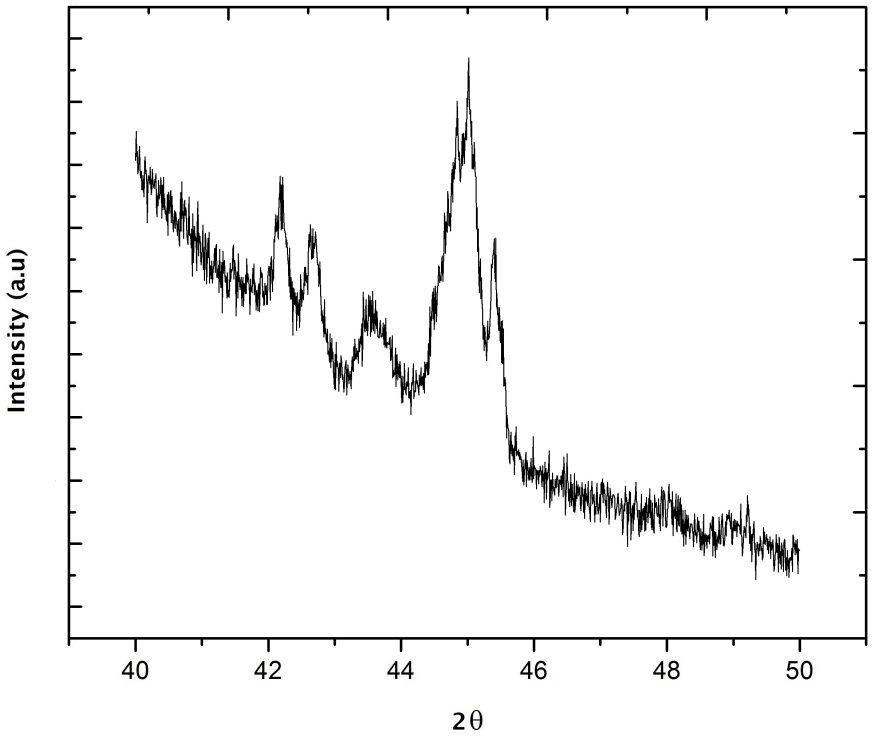


Figure 5.1: XRD Spectra of a Ni/Ti/Al/n-SiC Schottky barrier diode

recorded for specific angles and can be plotted in a graph as shown in Fig. 5.1 [84].

The pattern achieved for any particular material is unique and can be used to identify that material in any sample. Patterns for different materials add up and are recognizable like fingerprints. Commercially available databases can be used for matching or searching the spectra achieved by x-ray diffraction. These databases are also searchable through special computer software which can extract important information regarding the crystal structure or chemical composition of the sample used for investigation [84, 85].

## 5.2 Raman Spectroscopy

Raman spectroscopy is used to perform microscopic examination of materials for identification of molecules because Raman spectroscopy provides information about the vibrational modes in the material which are associated to the type of chemical bonding and

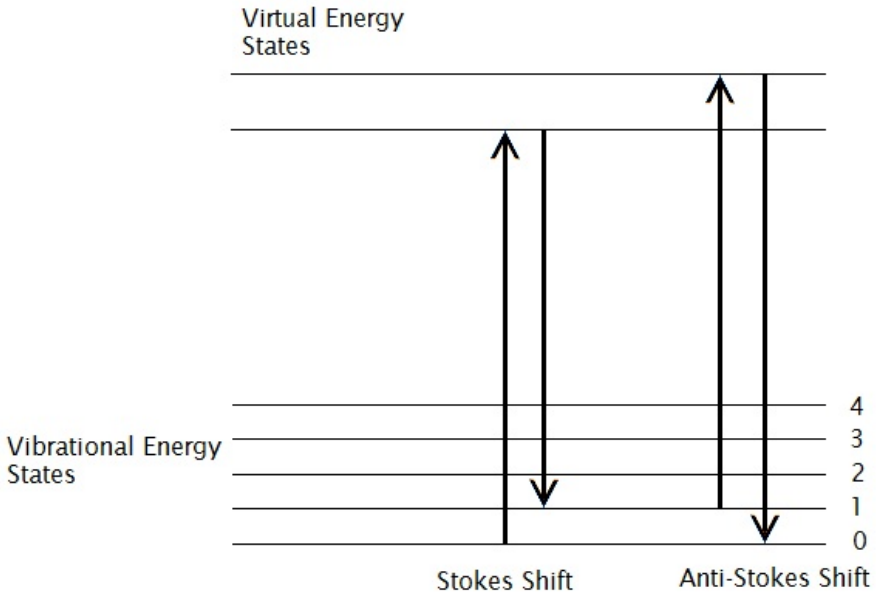


Figure 5.2: Energy states for Stokes and anti-Stokes shift. Source [86]

molecule symmetry; for the same reason it is also employed to study the changes in the chemical bonding. It is also helpful when it is necessary to know the crystallographic orientation of any solid by studying the polarization of scattered light and the polarization of incident light and the crystal itself. It is also possible, by using Raman spectroscopy, to know crystal quality[86]. Raman spectroscopy uses laser light from near infrared or near ultraviolet range of the visible spectrum to study phonons and molecular vibrations of the sample material. The sample is illuminated by laser light. The scattered light is detected, by band-stop filter for filtration, and studied for changes in energy[86].

When an incident photon hits a molecule (or atom) in the sample material, the energy of the molecule changes and the molecule comes in an excited virtual energy state. After some time the molecule emits a photon and goes back to a vibrational state different from its original vibrational state. This change in the vibrational state of the molecule results in a shift in the energy of emitted photon. If the energy of the emitted photon is more than that of incident photon then the shift in the energy is called anti-Stokes shift otherwise if the energy of the emitted photon is lowered and the molecule vibrates at

higher energy state then the shift is called Stokes shift as shown in Fig. 5.2 [86]. We did not use Raman spectroscopy for examination of the devices used in this research work but in future we will be using this technique together with BEEM for the examination of semiconductor material and devices based on it. BEEM is discussed in the following section.

## 5.3 Ballistic Electron Emission Microscopy

Ballistic electron emission microscopy (BEEM) is a technique in scanning tunneling microscope (STM). It is helpful in understanding the quality of metal-semiconductor interface because it can provide information about the local Schottky barrier height (SBH) at any particular location on the Schottky contact. Most of the times the SBH is not homogeneous and shows spatial variation which is also manifested in the abnormal current-voltage (I-V) characteristics. However, abnormal I-V characteristics can only provide information macroscopically while BEEM can detect microscopic changes in the SBH with great accuracy. The uncertainty in the measurement of SBH is around 0.01 eV. The experimental setup for BEEM is depicted in Fig. 5.3. BEEM involves three electrodes the Schottky metal is set at base voltage while the negatively biased STM tip is used to inject electrons into the sample and the ohmic metal serves as the collector where the ballistic electrons are collected. Normally it is performed with an additional in-vacuum current-voltage converter and preamplifier [87, 88, 89].

#### Measurement of SBH Through BEEM

For measurement of SBH at any point on the sample surface, electrons are injected into the Schottky metal surface (with the help of STM tip) which after passing through Schottky metal, metal-semiconductor interface and semiconductor substrate reach ohmic contact (collector). BEEM current is measured at the collector electrode and is plotted against tunnel voltage. Magnitude of tunnel voltage where the collector current is detected (we can call it threshold voltage) is measured as shown in Fig. 5.4. This voltage gives us the magnitude of Schottky barrier height. [88, 90].

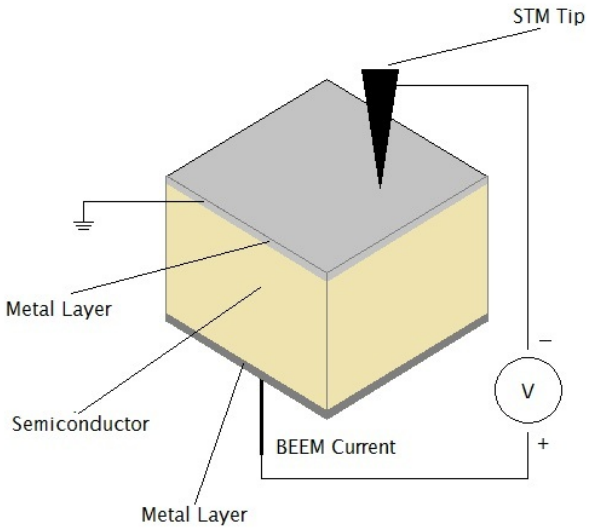


Figure 5.3: Ballistic electron emission microscopy setup. Source [87]

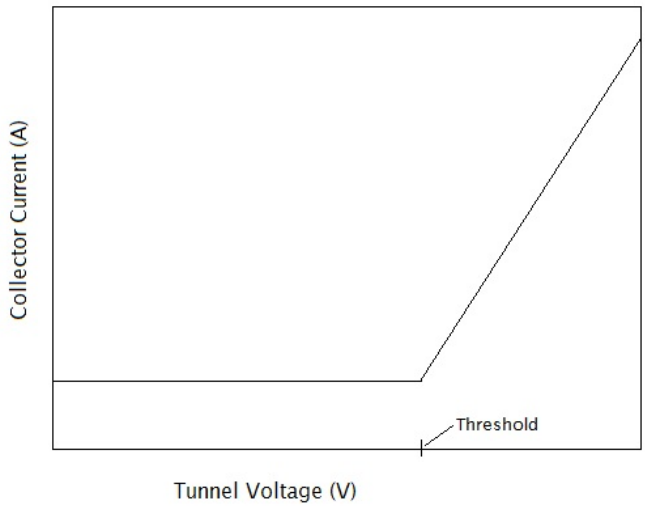


Figure 5.4: Typical BEEM plot. Source [88]

## 5.4 Electrical Characterization

Electronic devices must be characterized electrically in order to understand their electrical behavior. Silicon carbide based Schottky

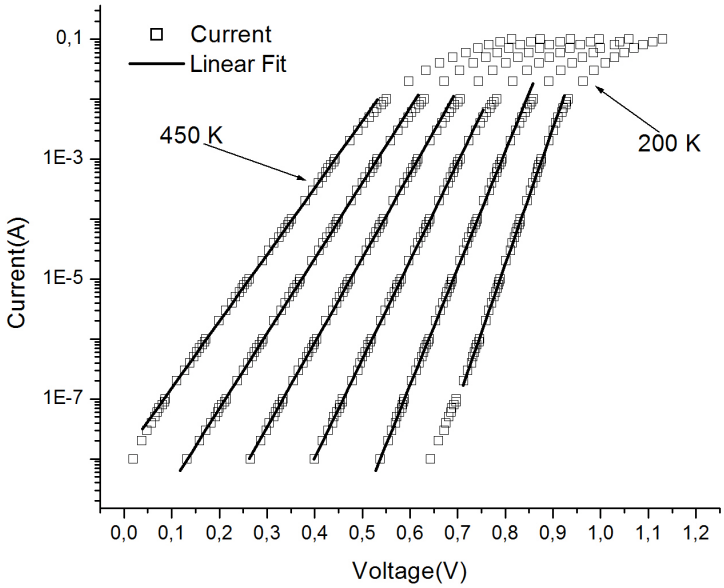


Figure 5.5: Forward Current-Voltage Characteristics ($lnI$ vs. $V$) of a Ti/4H-SiC SBD.

diodes can be characterized in two ways: by measuring current and voltage or by measuring capacitance and voltage. Automatic instruments are commercially available that can make such measurements and can provide current versus voltage or capacitance versus voltage values in electronic format, so that the data could be plotted for further analysis. Current and voltage measurements can be done with the help of Keithley 237 and 238 source measure units.

### 5.4.1 Current-Voltage Characteristics

Forward Current-voltage characteristics are used to measure Schottky barrier height and ideality factor of Schottky barrier diodes (SBDs). By measuring current and voltage at different temperatures it is possible to study the device performance. Schottky barrier height can be calculated from the current-voltage characteristics of any SBD. Typical I-V characteristics of a SiC Schottky barrier diode are shown in Fig. 5.5. I-V characteristics of a diode can be analyzed in the perspective of thermionic emission theory which predicts flow of current over a barrier $\Phi_A$ as given below[3]:

Figure 5.6: Keithley Source Measure Unit for I-V measurement

$$I = AA^*T^2exp\left(-\frac{e\Phi_A}{k_BT}\right) \tag{5.1}$$

Where A is the cross-sectional area of the barrier, A* is the Richardson constant, $\Phi_A$ is the barrier height, $k_B$ is the Boltzmann's constant and T is absolute temperature. Equation 5.1 is valid for thermionic emission of charge carriers in general. For thermionic emission in Schottky barrier diode we have to modify the equation because in the presence of forward bias lowering of SBH occurs and Eq. 5.1 can be written as follows:

$$I = A^*AT^2exp\left(-\frac{e\Phi_B - eV_a}{k_BT}\right) \tag{5.2}$$

where $e$ is elementary charge, $V_a$ is the applied voltage and $\Phi_B$ is the lowered SBH—due to image force lowering effect[3]. Its value is slightly lower than $\Phi_B^0$, the SBH which does not take into account the image force lowering effect:

$$\Phi_B = \Phi_B^0 - \delta\Phi_{image} \tag{5.3}$$

$$\Phi_B = \Phi_B^0 - \left[\frac{e^3N_DV_{bb}}{8\pi^2\varepsilon_s^3}\right]^{1/4} \tag{5.4}$$

Where $N_D$ is doping density of the semiconductor, $V_{bb}$ is the band-bending and $\varepsilon_s$ is the permittivity of semiconductor[3]. Equation 5.2 expresses current only in the forward direction while in fact the total current is a difference of the forward current and a current flowing in the opposite direction, which is equal to reverse saturation current and can be expressed as below:

$$I_S = A^* A T^2 exp\left(-\frac{e\Phi_B}{k_B T}\right) \tag{5.5}$$

and the total current is given by:

$$I = A^* A T^2 exp\left(-\frac{e\Phi_B}{k_B T}\right)\left[exp\left(\frac{eV_a}{k_B T}\right) - 1\right] \tag{5.6}$$

or

$$I = I_S\left[exp\left(\frac{eV_a}{k_B T}\right) - 1\right] \tag{5.7}$$

It is important to note that Eq. 5.7 does not take into account the resistance due to ohmic contact and the semiconductor substrate[3]. This resistance is called series resistance and if taken into consideration the net current can be written down as follows:

$$I = A^* A T^2 exp\left(-\frac{e\Phi_B}{k_B T}\right)\left[exp\left(\frac{eV_a - eIR_S}{k_B T}\right) - 1\right] \tag{5.8}$$

The SBH is found to lower due to tunneling effect which is very commonplace for semiconductors with high doping densities. Tunneling is also found in combination with thermionic emission; an

effect known as thermionic-field emission for which the current can be written in a slightly different way as given below[3]:

$$I = I_{S-TFE}\left[exp\left(\frac{eV_a}{E_0}\right) - 1\right] \tag{5.9}$$

where $I_{S-TFE}$ is the saturation current and $E_0$ is given by:

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{k_BT}\right) \tag{5.10}$$

and $E_{00}$ is given by:

$$E_{00} = \frac{e\hbar}{2}\left(\frac{N_D}{\varepsilon_s m^*}\right)^{1/2}. \tag{5.11}$$

Now it is possible to extract the value of SBH and ideality factor by plotting $ln(I)$ vs. $V_a$ (both $I$ and $V_a$ are experimentally measured). The slope of the linear region of the semi-logarithmic plot is calculated for extraction of ideality factor[3]. The ideality factor can be calculated by multiplying $e/k_BT$ with the inverse slope and SBH can be calculated from the intercept ($I_S$) as follows:

$$\Phi_B = -\left[ln\left(\frac{I_S}{AA^*T^2}\right)\right]\frac{k_BT}{e} \tag{5.12}$$

Equation 5.12 gives zero bias Schottky barrier height whose value is slightly lowered because of the image force lowering effect.

### 5.4.2 Capacitance-Voltage Characteristics

This technique was not used for the research presented in this thesis but a brief description of this method is worth reading. Capacitance-

Figure 5.7: HP Impedance Analyzer for C-V measurement

voltage (C-V) characteristics can be used to deduce the doping density and Schottky barrier height of the Schottky barrier diodes. For C-V characterization a HP4192AF impedance analyzer can be used (shown in Fig. 5.13). Capacitance is measured as a function of applied voltage and $1/C^2$ is plotted against applied reverse voltage (where $C$ stands for capacitance per unit area). The $1/C^2$ vs. $V$ plot is a straight line in case of uniform doping density. The slope of the straight line should be $-2/e\varepsilon_s N_D$ and the capacitance per unit area is given by:

$$C = \sqrt{\frac{e^2 \varepsilon_s N_D}{2(eV_{bb} - k_B T)}} \tag{5.13}$$

While x-axis intercept is equal to the built-in potential ($V_{bi}$) which can be used to extract the homogeneous SBH. The value of this SBH is slightly larger than the one extracted from I-V characteristics because it does not take into account the image force lowering of the SBH[3].

## 5.5 Summary

In this chapter some of the most important characterization techniques are discussed. X-ray diffraction and Raman spectroscopy are important when material characterization, for chemical composition or surface morphology, is required. Current-voltage and capacitance-voltage techniques are used for device characterization in order to understand the electrical behavior of the device and to

detect Schottky barrier inhomogeneity which will be discussed in the next chapter.

# Chapter 6

# Results and Discussion

This chapter is dedicated to the research done during whole PhD. Different anomalous device behaviors are described which indicate inhomogeneous Schottky barrier height. Electrical characterization of the Schottky barrier diodes is presented in the later part of the chapter with Tung's model used for the fitting of experimental data. The diodes used for this research work were fabricated on 3" n-type 4H-SiC wafers bought from Cree Inc. The doping concentration of the bulk substrate was $10^{18}$ cm$^{-3}$ with a thickness of 360 $\mu$m. The doping concentration of epitaxial layer was $10^{16}$ cm$^{-3}$ with a thickness of 5.5 $\mu$m. Aluminum ion implantation was used for the fabrication of P$^{+}$-type guard rings with mesa type structure. The first part of the chapter is dedicated to the Schottky barrier inhomogeneity and the latter part is dedicated to the electrical characterization of various Schottky barrier diodes.

## 6.1 Schottky Barrier Inhomogeneity

Inhomogeneity of the Schottky barrier height is an important problem and is a challenge for researchers who first did not pay proper attention to it until 1980s when it was microscopically proved through BEEM (ballistic electron emission microscopy) studies that in most of the cases the Schottky barrier height is not uniform and shows variation throughout the metal-semiconductor interface—which before this was considered to be uniform. Moreover, with the use of polycrystalline materials for the fabrication of modern semiconductor electronic devices it came more into focus. Devices based on silicon carbide also exhibit a number of behaviors characteristic of Schottky barrier inhomogeneity such as abnormal current-voltage

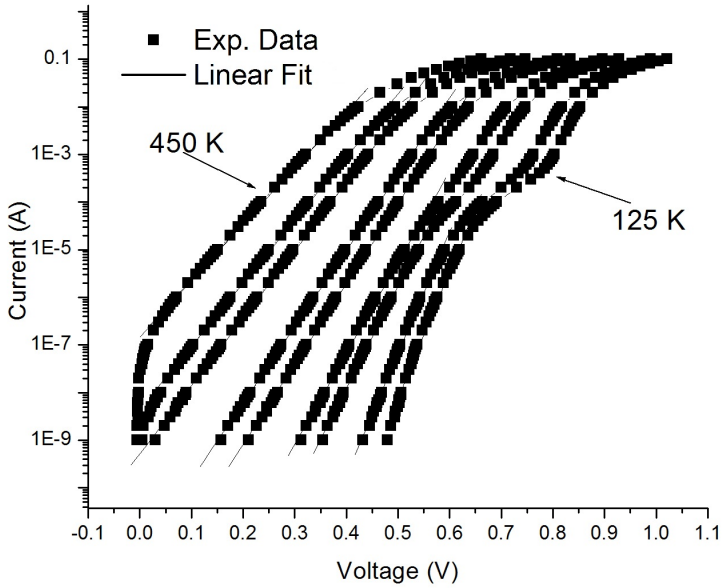


Figure 6.1: Forward I-V characteristics: $ln(I)$ vs. $V$ of Mo/4H-SiC SBD. Taken from [91]

characteristics, greater than unity ideality factor, temperature dependence of the ideality factor and reverse leakage current [3].

### 6.1.1 Abnormal I-V Characteristics

Schottky barrier diodes based on SiC often show abnormal current-voltage (I-V) characteristics with excess leakage current as shown in Fig. 6.1. This phenomenon is very common at low temperature. The ideality factor changes with the conduction mechanism, it is usually close to unity where the semi-logarithmic I-V plot is linear and its value deviates much from unity where the I-V plot shows curvature and small slope. The main conduction mechanism for linear portion of the plot is thought to be the thermionic emission while for the non-linear portion generation-recombination in the depletion region along with edge-related leakage currents are considered to be the reason for conduction. Sometimes only generation-recombination is responsible for the excess current and edge-related current is completely absent which means these both causes are not linked to each other. It has also been noticed that the excess

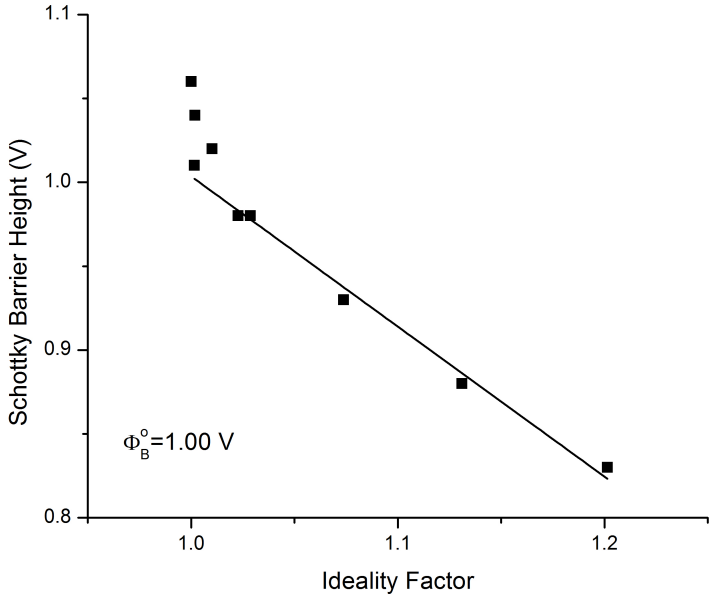


Figure 6.2: SBH vs. ideality factor plot of Mo/4H-SiC SBD.

current is present in some diodes while absent in other diodes fabricated on the same sample which indicates non-uniform distribution of generation-recombination centers [3].

According to R. T. Tung both excess current and edge-related current can be explained by linking them to the Schottky barrier inhomogeneity. Due to the spatial variation of the Schottky barrier height it is assumed that isolated low barrier height regions may exist with ideality factor values much larger than unity. Large values of ideality factor can explain the leakage current which is limited to the low forward biases because of series resistance. According to Tung the fact that the excess current is observed in some diodes and is missing in other diodes is in accordance with assumption that the isolated low SBH regions are causing excess current rather than generation-recombination centers in the depletion region. Leakage current is also dependent on the size of the diode and it is argued that low SBH patches exhibit better conduction when located near the edges rather than the middle of the contact possibly because the pinch off phenomenon is less effective near the edges as compared to the middle [3].

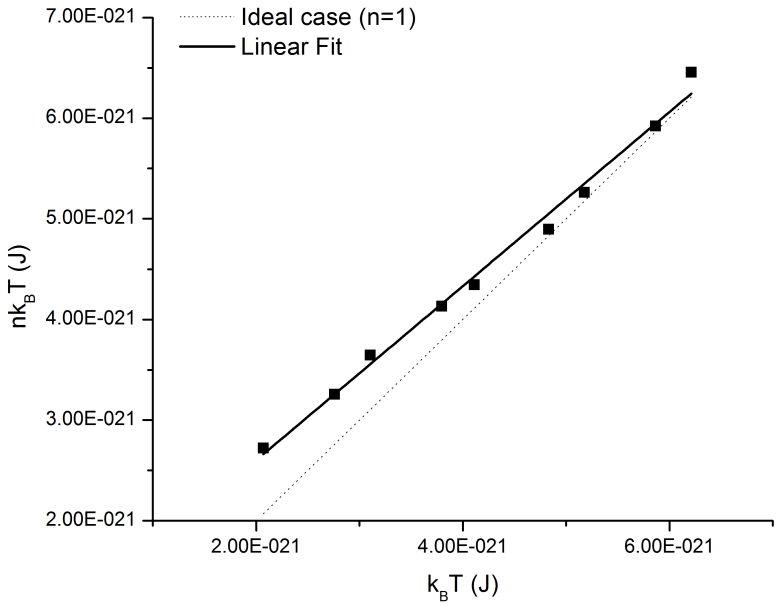


Figure 6.3: $T_o$ effect at low temperature for Mo/4H-SiC SBD. Taken from [91]

### 6.1.2 Greater Than Unity Ideality Factor

Ideality factor is the measure of Schottky contact quality whose value ranges from 1 to 2, if it is unity the Schottky contact is considered to be ideal and if its value is more than 1.0 the Schottky contact is considered to be of low quality[69]. Classical thermionic emission theory cannot explain an ideality factor greater than 1.03, therefore other conduction mechanisms or leakage currents and surface states are thought to be the causes of large ideality factor values. Moreover, ideality factors may have different values if different processing techniques were applied during the fabrication of the diodes and sometimes different ideality factors are reported for diodes fabricated on the same sample. Ideality factor often shows dependence on the experimentally calculated SBH as shown in Fig. 6.2. This behavior of ideality factor is attributed to the inhomogeneity of the SBH due to the fact that saddle point potential of inhomogeneous Schottky barrier depends on the applied bias. Correlation between SBH and ideality factor can be written mathematically as [3]:

$$\Phi_B^{eff} = \Phi_B^0 - (n_{eff} - 1)\, V_{bb}\xi^{-1} \tag{6.1}$$

Where $V_{bb}$ is band-bending, $\Phi_B^0$ is the homogeneous SBH, $n_{eff}$ is the ideality factor of low SBH region and $\xi$ is 2/3. Taking into consideration the bias dependence of the SBH the diode current can be re-written as follows [3]:

$$I = AA^*T^2 exp\left(-\frac{e\Phi_B(V_a)}{k_BT}\right)\left[exp\left(\frac{eV_a}{k_BT}\right) - 1\right] \tag{6.2}$$

the bias dependent SBH can be calculated as [3]:

$$\Phi_B(V_a) = \Phi_B(0) + \left(\frac{n-1}{n}\right)V_a \tag{6.3}$$

Where $\Phi_B(0)$ is the zero-bias SBH and is often quoted as the fundamental SBH of the system[3].

### 6.1.3 Temperature Dependence of Ideality Factor

Temperature dependence of ideality factor is observed very frequently by researchers working on SiC based Schottky barrier diodes [92, 93, 94]. Normally a linear correlation is seen if the inverse slope ($nk_BT$) of the $ln(I)$ vs. V plot is plotted against $k_BT$ as shown in Fig. 6.3. If the plot is a straight line parallel to the n=1 line then the device is said to show $T_o$ effect and its junction current can be written as follows [3, 5]:

$$I_{T_o} = A^*AT^2 exp\left(-\frac{e\Phi_{T_o}}{k_B[T+T_o]}\right)\left[exp\left(\frac{eV_a}{k_B[T+T_o]}\right) - 1\right] \tag{6.4}$$

Eq. 6.4 is different from Eq. 6.1 in that it uses a constant temperature $T_o$ added to the measurement temperature T and it uses a constant $\Phi_{T_o}$ instead of using $\Phi_B$. Sometimes the diodes show $T_o$ effect at high temperature and sometimes at low temperature and the ideality factor changes its behavior in various manners. In Fig. 6.3 the diode shows $T_o$ effect only at low temperature and tends to become more ideal-like at high temperature. Other behaviors of ideality factor are also reported where the ideality factor is initially close to unity at low temperature and becomes larger and larger as the temperature is increased without showing $T_o$ effect at all. All these different behaviors of ideality factor can be explained by the fact that the Schottky barrier height is not homogeneous and shows spatial variation contrary to the claims of some researcher who have attributed these different behaviors of ideality factor to different conduction mechanisms such as thermionic field emission and tunneling (assuming the SBH to be homogeneous) [3].

For inhomogeneous SBH thermionic emission alone is sufficient to explain all the behaviors for example it can be argued that when the $T_o$ effect is only visible at low temperature the diode current is dominated by that of low barrier height regions. Similarly the $T_o$ effect can be observed at high temperature if some of the low SBH regions are not pinched-off due to their large sizes. If the density of low SBH patches is high in some diode then it is possible to observe an ideality factor behavior similar to that which is independent of temperature. In this case the ideality factor does not show $T_o$ effect at all [3, 4].

### 6.1.4 Reverse Leakage Current

It is very common to observe reverse leakage currents even at high reverse biases which cannot be tied to the edge related effects or image force lowering alone because of the large amount of current. Instead, image force lowering combined with the SBH lowering due to interface states can explain, to some extent, these reverse leakage currents as investigated by Andrews et al. [3, 95]. According to Andrews et al. the total SBH lowering can be written as follows [3]:

$$\delta\Phi_{total} = \delta\Phi_{image} + \delta\Phi_{MIGS} \tag{6.5}$$

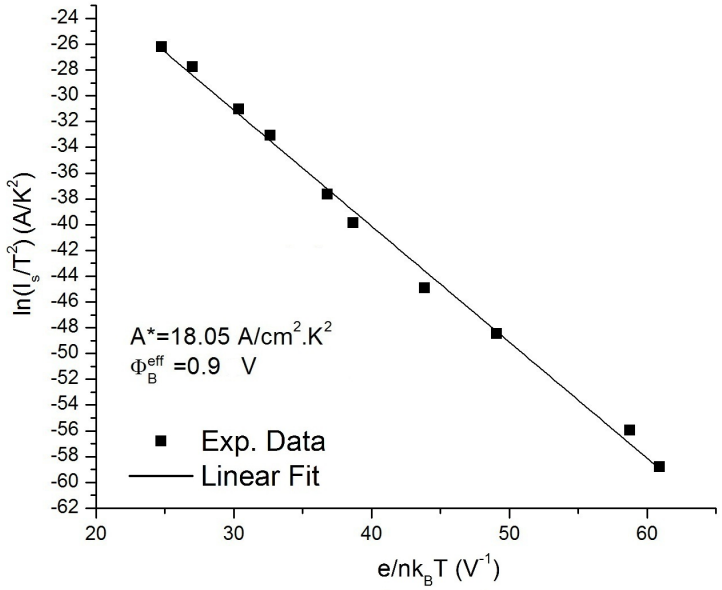


Figure 6.4: Richardson's plot for Mo/4H-SiC SBD 'A'. Taken from [91]

or

$$\delta\Phi_{total} = \frac{1}{2}\left(\frac{eE_{max}}{\pi\varepsilon_s}\right)^{1/2} + z_{max}E_{max} \tag{6.6}$$

Where $\varepsilon_s$ is permittivity of the semiconductor and $\delta\Phi_{MIGS}$ is Schottky barrier lowering due to interface states and $z$ is the distance from MS interface of a point into semiconductor. It is important to note that Eq. 6.6 is only valid for n-type semiconductors while the reverse leakage currents are observed in both n- and p-type semiconductors alike which clearly indicates that the SBH lowering due to image force and interface states is not the sole reason for reverse leakage currents thus a mechanism that could result in the rapid variation of SBH with the electric field, would be more appropriate such as the inhomogeneity of the Schottky barrier height as investigated by Tung [3].

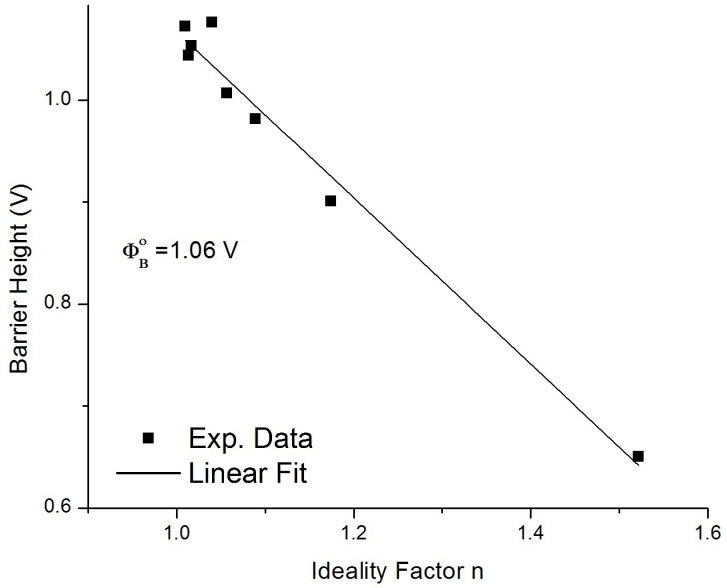


Figure 6.5: SBH vs. ideality factor for Mo/4H-SiC SBD 'A'. Taken from [91]

## 6.2 Modeling the Inhomogeneous MS Interface

To model a metal-semiconductor (MS) contact current-voltage and temperature measurements are taken in order to extract the electrical parameters such as Schottky barrier height $\Phi_B$ and the ideality factor n. Two molybdenum and a titanium Schottky barrier diodes characterized at different temperatures will be applied mathematical model in the purview of thermionic emission theory considering the modifications proposed by Tung [91, 96].

Thermionic emission theory predicts flow of charge either from a surface or over a barrier due to thermal energy of charge carriers by which they can surmount the potential barrier (called work function) of the material from which the charge carriers are emitted. Vacuum tubes are prime examples of devices working on the principles of thermionic emission where a filament is heated to a certain temperature so that it could emit electrons. Thermionic emission also applies when charge carriers are emitted from some regions of semiconductor electronic devices and enter other regions due to excess energy provided by heat. Schottky diodes are comprised of metal-semiconductor contacts which conduct mainly due

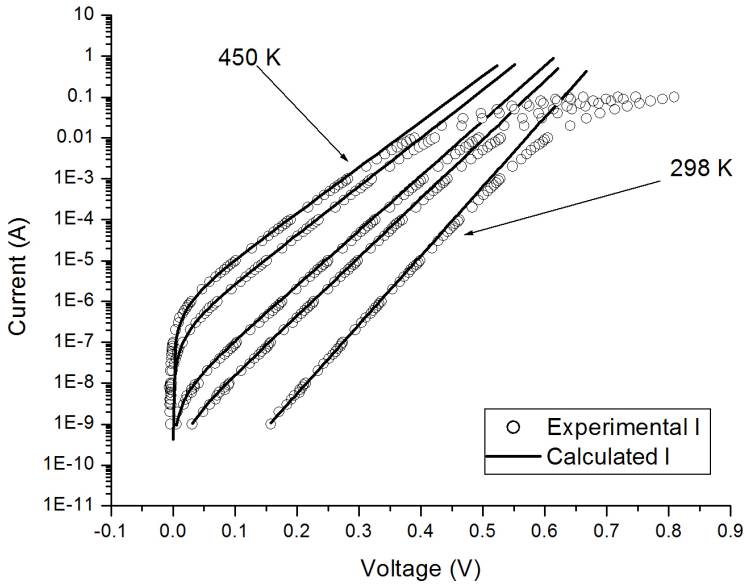


Figure 6.6: Calculated and Experimental current: $ln(I)$ vs. $V$ for SBD 'A'. Taken from [91]

to thermionic current [97]. The current passing through a Schottky barrier diode (SBD) with cross-sectional area A and applied bias $V_a$ can be expressed as follows [93]:

$$I = I_S \left[ exp\left(\frac{eV_a}{nk_BT}\right) - 1 \right] \tag{6.7}$$

Where $I_S$ is the saturation current and is given by:

$$I_S = AA^*T^2 exp\left(-\frac{e\Phi_B}{k_BT}\right) \tag{6.8}$$

Where $A^*$ is the Richardson constant with a theoretical value of

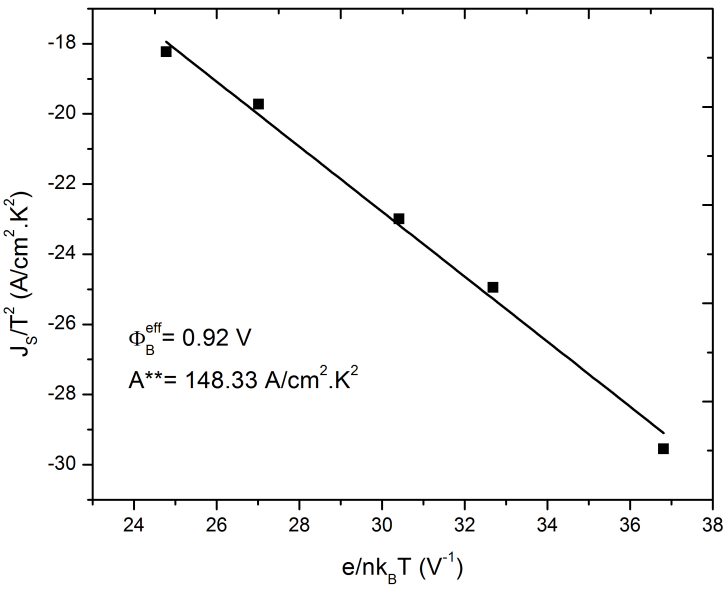


Figure 6.7: Modified Richardson's plot: $ln(J_s/T^2)$ vs. $e/nk_BT$, for SBD 'A'.

146 A/cm$^2$.K$^2$ (for 4H-SiC), $k_B$ is the Boltzmann's constant and $\Phi_B$ is the zero bias Schottky barrier height.

Thermionic emission theory considers the SBH to be homogeneous and cannot predict the diode current in accordance with the experimentally measured current. For this reason it needs to be modified taking into consideration the inhomogeneity of the Schottky barrier. If we assume the SBH to be composed of low barrier height patches then after slight modifications the diode current can be expressed as given below [93, 94]:

$$I = NA_{eff}A^*T^2exp\left(-\frac{e\Phi_B^{eff}}{k_BT}\right)\left[exp\left(\beta V_a\right) - 1\right] \tag{6.9}$$

Where $\beta = e/k_BT$, N is the total number of low SBH patches and $\Phi_B^{eff}$ is the Schottky barrier height of a low barrier patch and can be calculated as follows[93, 94]:

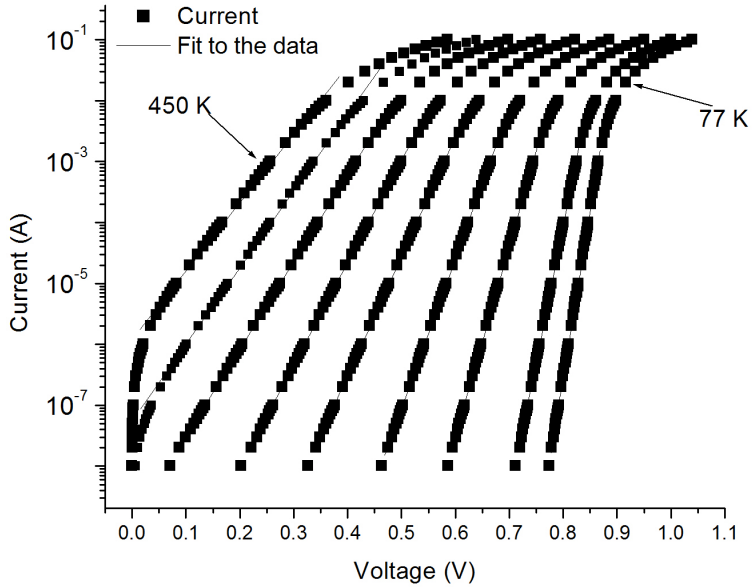


Figure 6.8: Forward I-V characteristics: $ln(I)$ vs. $V$ of Mo/4H-SiC SBD 'B'.

$$\Phi_B^{eff} = \Phi_B^0 - \gamma \left( \frac{V_{bb}}{\eta} \right)^{1/3} \tag{6.10}$$

$\Phi_B^0$ in Eq. 6.10 is the homogeneous Schottky barrier and $V_{bb}$ is the band-bending potential (which is the difference of built-in potential and the applied bias), it is related to the area of a low SBH patch $A_{eff}$ as given below:

$$A_{eff} = \frac{4\pi\gamma}{9\beta} \left( \frac{\eta}{V_{bb}} \right)^{2/3} \tag{6.11}$$

Where $\gamma$ is the low SBH patch parameter which takes into account the area of the patch and $\eta = \varepsilon_s/(eN_D)$ with $\varepsilon_s$ being the permittivity of the semiconductor and $N_D$ being the doping density of the semiconductor. $V_{bb}$ is given by:

$$V_{bb} = \Phi_B^0 - V_N - V_a \tag{6.12}$$

Where $V_N$ is the conduction band minimum and is given by:

$$V_N = \frac{k_B T}{e} ln\left(\frac{N_D}{N_C}\right) \tag{6.13}$$

where $N_C$ is the density of states of the conduction band and can be written as:

$$N_C = 2\left[\frac{2\pi m_e^* k_B T}{h^2}\right]^{3/2} \tag{6.14}$$

In eq. 6.14 $m_e^*$ is the effective mass of electron which is different for each polytype of SiC[70, 98].

### 6.2.1 Electrical Characterization of Mo/4H-SiC SBDs

#### Device Fabrication

Wafers used for the fabrication of these diodes are mentioned in the beginning of this chapter. Schottky barrier diodes were designed with a $p^+$-type guard ring and a mesa-type structure with

| **Temp.(K)** | **SBH (V)** | **n** | $\gamma$ **($10^{-6} m^{2/3} V^{1/3}$)** | **N ($10^7$)** |
|---|---|---|---|---|
| 275 | 0.98 | 1.08 | 7.6 | 8.3 |
| 298 | 1.01 | 1.05 | 7.53 | 5.0 |
| 350 | 1.04 | 1.01 | 7.36 | 4.5 |
| 375 | 1.05 | 1.01 | 7.29 | 4.6 |
| 425 | 1.07 | 1.00 | 7.15 | 4.5 |
| 450 | 1.07 | 1.03 | 7.08 | 4.5 |

Table 6.1: Important SBD parameters for Mo/4H-SiC SBD 'A'

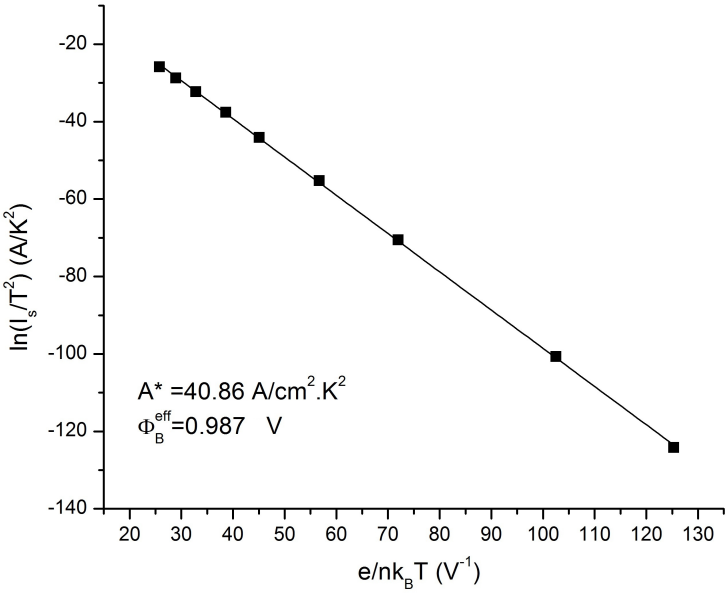


Figure 6.9: Conventional Richardson's plot for SBD 'B'. Taken from [96]

an additional silicon dioxide ($SiO_2$) passivation layer. Aluminum ion implantation was used for the formation of the $p^+$-type guard ring. This step was followed by a Rapid Thermal Process (RTP) at temperatures exceeding 1500 $^o$C, in order to promote lattice damage recovery and to achieve a reasonable electrical activation of the implanted $Al^+$ ions.

A silicon dioxide passivation layer was grown by means of a Low Temperature Oxidation (LTO) process, using TetraEthylOxySilane (TEOS) as a precursor. The $SiO_2$ layer was patterned using standard UV photolithography, and etched by a buffered HF-based solution. The Schottky contact was then realized by the deposition of Mo layer (with thickness of 100 nm) on the 4H-SiC epilayer surface. The Mo deposition was followed by an annealing treatment performed at 400 $^o$C in inert atmosphere and deposition of Al layer on top of Schottky contact for wire bonding of the device. The ohmic contact was obtained on wafer's backside by means of a triple layer of Ti, Ni and Ag, without the need of a post-deposition annealing treatment. The deposition of both Schottky and the ohmic contacts was performed using an electron beam evaporator (ULVAC model EBX-14D), at a pressure of about $10^{-5}$ Pa.

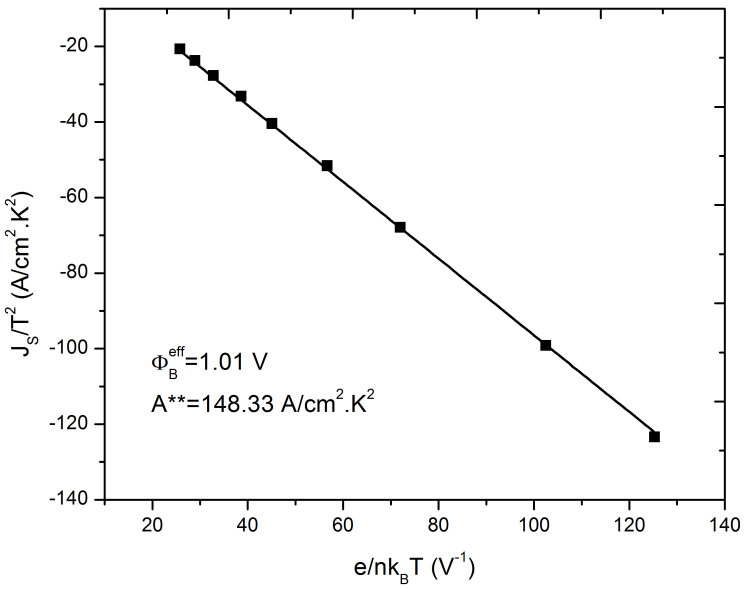


Figure 6.10: Modified Richardson's plot: $ln(J_s/T^2)$ vs. $e/nk_BT$, for SBD 'B'.

The electrical characterization of the SBDs was performed by acquiring the current-voltage (I-V) curves using Keithley 237 and 238 Source Measure Units. The capacitance-voltage (C-V) characteristics were acquired by means of a HP4192A impedance analyzer.

**Electrical Characterization**

In this section the I-V characteristics of Schottky diodes with molybdenum Schottky contact will be analyzed—first the diode which was characterized at 125 K to 450 K temperatures (we can call this diode 'A' for convenience). The values of SBH and n, for this diode,extracted from forward I-V plot are listed in Table 6.1. SBH values are in agreement with some of the recently reported works such as A. Latreche et al.[99] and L. Boussouar et al.[100]. In order to determine the value of Richardson's constant ($A^*$) and the effective SBH, Richardson's plot is normally used which shows a relationship between $ln(I_s/T^2)$ and 1/T, as shown in Fig. 6.4, $I_s$ here represents the saturation current. From the y-intercept of Richardson's plot a value 18.05 $A/cm^2K^2$ of Richardson constant was determined which is apparently lower than the theoretical value of 146 $A/cm^2K^2$. This very low value of $A^*$ can be indicative of an effec-

tive area (the area of SBD involved in the current transport process) very different from the geometric area of SBD [92].

From the slope of Richardson's plot a value equal to 0.9 V of the effective SBH was determined. Richardson constant's very small value could not be explained with the help of thermionic emission theory and is a topic of interest among many researchers. Abnormal value of Richardson constant indicates to the fact that the actual area involved in the current transport is much different from geometric area strengthening the notion that the MS interface contains many interacting, low barrier patches embedded in the high uniform barrier. The current contribution from these patches is considered to be much greater than other current contributions so that the total current passing through the SBD approximately equals the sum of all current contributions from these low barrier patches.

Homogeneous Schottky barrier height ($\Phi_B^0$) appearing in Eq. 6.10, can be determined by plotting the zero bias SBH values versus n as shown in Fig. 6.5. Extrapolating this plot to n=1 yields the value of $\Phi_B^0$, which in our case is 1.06 V. The effective Schottky barrier height ($\Phi_B^{eff}$) (appearing in Eq. 6.10) can be determined from the slope of the Richardson's plot which shows a relationship between $ln(Is/T^2)$ and 1/T. The value of $\Phi_B^{eff}$ found from the Richardson's plot is slightly lower than $\Phi_B^0$ i.e. 0.9 V. By using above mentioned values of $\Phi_B^0$ and $\Phi_B^{eff}$ it was possible to find the values of $\gamma$ which come out to be in the range $7.69 \times 10^{-6}$—$7.08 \times 10^{-6} m^{2/3} V^{1/3}$ (from low characterization temperature to high characterization temperature). We used these values of $\gamma$ in the calculation of effective areas at different temperatures which then were used in Eq. 6.9 to calculate the theoretical diode current (taking N as a free parameter). We used different values of N for different temperatures so that the product $NA_{eff}$ is in the range $4.68 \times 10^{-4}$—$3.36 \times 10^{-4}$ (from low characterization temperature to high characterization temperature).

Figure 6.6 shows a comparison of experimental and theoretical I-V characteristics. In order to calculate the correct value of Richardson constant ($A^{**}$) we modified a little the conventional Richardson's plot so that $ln(Is/NA_{eff}T^2)$ (or $J_s/T^2$) was plotted against $e/nk_BT$, as can be seen in Fig. 6.7. A value 148.33 $A/cm^2K^2$ of $A^{**}$, found by fixing the y-intercept of the modified Richardson's plot is in very good agreement with the theoretical value of 146 $A/cm^2K^2$. The value of $\Phi_B^{eff}$ on the other hand comes out to be 0.92 V, slightly higher than the earlier value of 0.9 V, which is again in good agreement.

Another Schottky diode with molybdenum Schottky contact (we

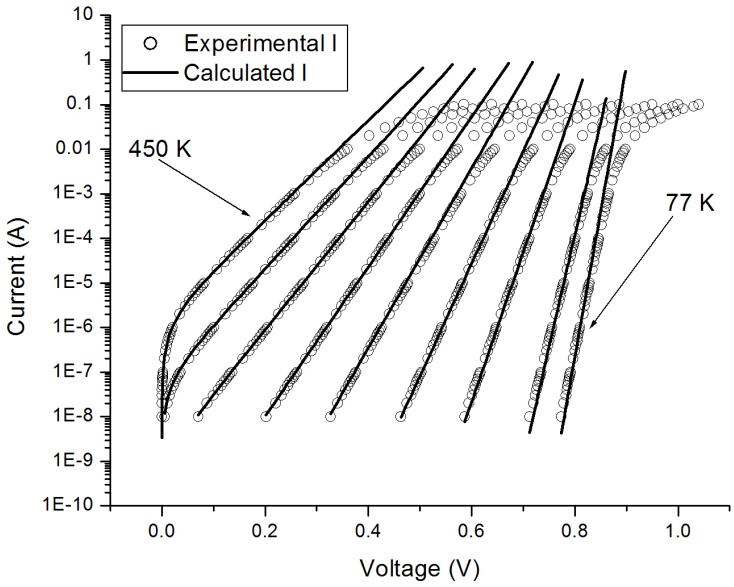


Figure 6.11: Experimental and calculated current: $ln(I)$ vs. $V$ for Mo/4H-SiC SBD 'B'. Taken from [96]

can call it diode 'B') and same contact area but characterized at temperatures ranging from 77 K to 450 K was also analyzed. The current voltage characteristics are shown in Fig. 6.8 and SBH and n extracted from the forward I-V plot are listed in Table 6.2. The methodology is the same as discussed before so the focus will be on the results obtained for any similarities or differences between two apparently similar Schottky diodes. This diode shows better contact quality as is visible from the I-V characteristics which do not show excess current at low temperature. We again start from the Richardson plot shown in Fig. 6.9 . The value of Richardson constant extracted from Richardson plot is 40.86 $A/cm^2.K^2$ which is again very low as compared to the theoretical value indicating inability of thermionic emission theory to predict the diode current. Effective Schottky barrier height extracted from conventional Richardson plot is 0.987 V while the homogeneous SBH extracted from SBH vs n plot is 1.00 V. Values of $\gamma$ range from 9.28 x $10^{-7}$ at low characterization temperature to 5.05 x $10^{-7}$ $m^{2/3}V^{1/3}$ at high characterization temperature as listed in Table 6.2 together with the number of low barrier patches at different temperatures. The value of Richardson constant extracted from the modified Richard-

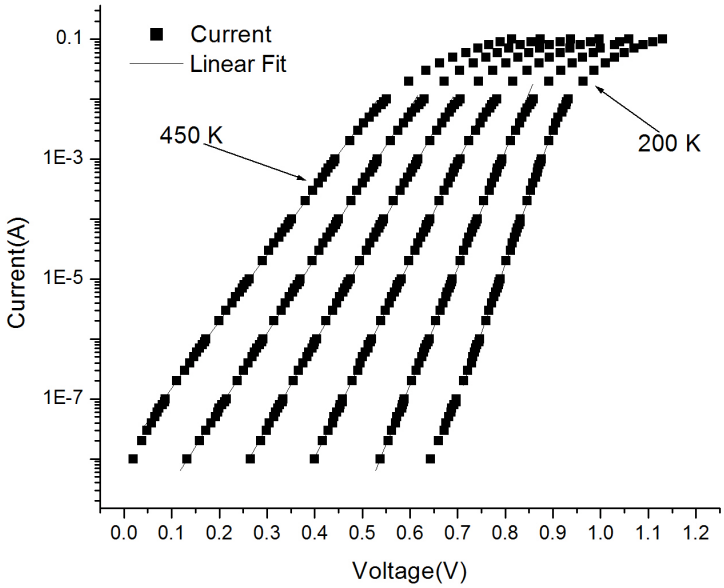


Figure 6.12: Forward I-V characteristics: $ln(I)$ vs. $V$ of Ti/4H-SiC SBD 'C'

son plot shown in Fig. 6.10 is 148.33 A/$cm^2.K^2$ again very close to the theoretical value. The diode current calculated by Tung's model is shown alongside the experimentally measured current (Fig. 6.11). Both the currents are in good agreement indicating the success of the model. Similar results are achieved for Schottky diodes with titanium Schottky contact which will be discussed in the next section.

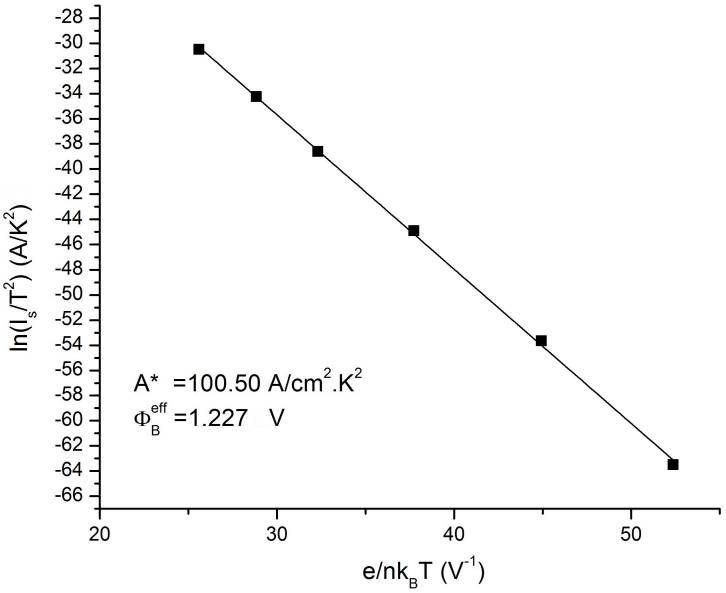


Figure 6.13: Conventional Richardson's plot for diode 'C'. Taken from [96]

### 6.2.2 Electrical Characterization of Ti/4H-SiC SBD

Schottky diode with titanium Schottky contact was also characterized for application of Tung's model. The diode has same area i.e. 0.0305 $cm^2$ and for the convenience will be called diode 'C'. This

| **Temp.(K)** | **SBH (V)** | **n** | $\gamma$ **($10^{-7}m^{2/3}V^{1/3}$)** | **N ($10^{10}$)** |
|---|---|---|---|---|
| 77 | 0.83 | 1.20 | 9.28 | 100 |
| 100 | 0.88 | 1.13 | 8.45 | 50 |
| 150 | 0.93 | 1.07 | 7.38 | 150 |
| 200 | 0.98 | 1.02 | 6.70 | 6 |
| 250 | 0.98 | 1.02 | 6.18 | 6 |
| 300 | 1.01 | 1.00 | 5.81 | 3 |
| 350 | 1.02 | 1.01 | 5.50 | 2.5 |
| 400 | 1.04 | 1.00 | 5.26 | 1.73 |
| 450 | 1.06 | 1.00 | 5.05 | 1.33 |

Table 6.2: Important SBD parameters for Mo/4H-SiC SBD 'B'

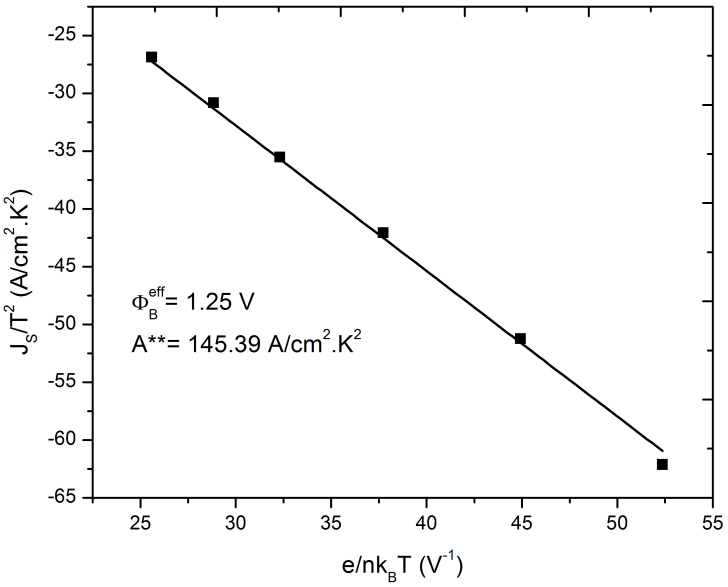


Figure 6.14: Modified Richardson's plot: $ln(J_s/T^2)$ vs. $e/nk_BT$, for diode 'C'.

diode was fabricated using similar laboratory conditions and process techniques as already have been mentioned in the previous section. Analysis of the I-V curves (shown in Fig. 6.12) was carried out using similar techniques as used in the previous section so my focus will be on explanation of the obtained results. For diode 'C' important electrical parameters are listed in Table 6.3. The value of Richardson constant for this diode is 145.39 A/$cm^2.K^2$ extracted from modified Richardson plot shown in Fig. 6.14 and the one extracted from conventional Richardson plot of Fig. 6.13 (which does not

| **Temp.(K)** | **SBH (V)** | **n** | $\gamma$ **($10^{-8}m^{2/3}V^{1/3}$)** | **N ($10^{11}$)** |
|---|---|---|---|---|
| 200 | 1.12 | 1.10 | 4.39 | 125 |
| 250 | 1.19 | 1.03 | 4.32 | 37.5 |
| 300 | 1.20 | 1.02 | 4.24 | 21.3 |
| 350 | 1.21 | 1.02 | 4.17 | 15.0 |
| 400 | 1.23 | 1.00 | 4.11 | 9.6 |
| 450 | 1.24 | 1.00 | 4.04 | 7.5 |

Table 6.3: Important SBD parameters for Ti/4H-SiC SBD 'C'

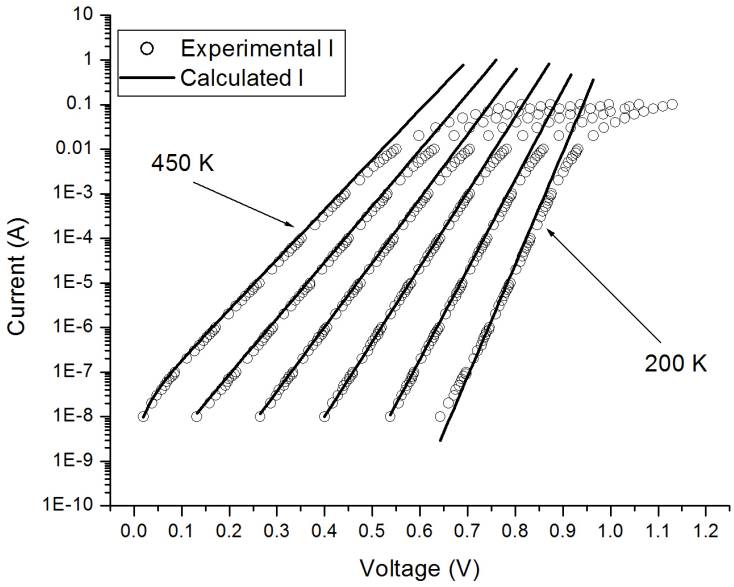


Figure 6.15: Experimental and calculated current: $ln(I)$ vs. $V$ for Mo/4H-SiC SBD 'C'. Taken from [96]

take into account the inhomogeneity of SBH) is 100.50 A/$(cm^2K^2)$. The comparison of theoretical and experimental currents is shown in Fig. 6.15 which indicates a better underlying Schottky contact with relatively minimum inhomogeneity in the Schottky barrier height.

### 6.2.3 Comparison of Characterized SBDs

Now we look at some important parameters reported in Table 6.4 e.g. N, A*, $N.A_{eff}$, $\Phi_B^{eff}$, their interdependence and relationship with the temperature. It is interesting to note that the total number of low barrier patches N, decreases with increasing temperature and is very high in diode B. On the other hand no dependence of N was seen on the type of metal used in the SBD or the geometric area of the diode because both diodes A and B have Mo Schottky contact but with very different number of patches and similarly if the number of patches were dependent on the area of the diodes than all the diodes should have had same number of patches, which in fact is different for each diode. Moreover, total effective area involved in the current transport $N.A_{eff}$, is inversely proportional to the characterization temperature and shows little sensitivity to temperature

| **Diode** | **A (Mo)** | **B (Mo)** | **C (Ti)** |
|---|---|---|---|
| **Area ($cm^2$)** | 0.0305 | 0.0305 | 0.0305 |
| **Temp. (K)** | 275-425 | 77-450 | 200-450 |
| $\Phi_B^0$ **(V)** | 1.06 | 1.00 | 1.228 |
| $\Phi_B^{eff}$ **(V)** | 0.9 | 0.987 | 1.227 |
| **N ($10^7$)** | 8.3 - 4.5 | $10^5$ - 1.33x$10^3$ | 125x$10^4$ - 750x$10^2$ |
| $\mathbf{NA}_{eff}$ ($10^{-4}cm^2$) | 4.68 - 3.36 | 4380 - 54.9 | 2550 - 269 |
| $\mathbf{A}^*$ ($A/cm^2.K^2$) | 18.05 | 40.86 | 100.5 |
| $\mathbf{A}^{**}$ ($A/cm^2.K^2$) | 148.33 | 148.33 | 145.39 |

Table 6.4: Low SBH patch parameters for 4H-SiC SBDs. Source[96]

changes in case of diode A. Diodes B and C show high sensitivity of effective area to the temperature changes. A connection can also be seen between N and A*. The more number of patches are present in the Schottky contact, higher is the value of A* as reported in the Table 6.4. Apart from the diodes which were characterized for Tung's model we also fabricated a number of Schottky barrier diodes with triple layer metallization used for the Schottky contact (in view of simultaneous formation of both Schottky as well as ohmic contacts with low annealing temperature required for the contact formation and low specific contact resistance values). Electrical characterization of some of those diodes is given in the following section.

### 6.2.4 Electrical Characterization of Ni/Ti/Al SBDs

In order to fabricate electronic devices we need suitable metals that could be used as contact materials. Very few materials are able to form both Schottky as well as ohmic contacts to SiC with specific contact resistance of below 1 x $10^{-5}\Omega cm^2$. Low resistance ohmic contacts are needed for the fabrication of high power and high fre-

quency electronic devices such as metal-semiconductor field effect transistor (MESFET) and metal-oxide field effect transistor (MOSFET). To obtain a good ohmic contact on SiC, using conventional materials, high annealing temperatures are needed, while more than 800 $^{o}$C temperature is harmful for devices like MOSFETs due to the possibility of chemical reaction between gate metal and oxide layer which may result in decreased performance of the device [101]. This demands the search for a material or a combination of materials that could form good ohmic contacts with low annealing temperatures. One such contact material is a triple layer of Ni/Ti/Al (/ indicates the order of deposition), as studied by Tsukimoto et al. for p-type SiC [102].

Ni/Ti/Al triple layer can also form Schottky contacts on n-type 4H-SiC with the advantage that it could be done at temperatures well below 800 $^{o}$C. It is also one of the few materials to form ohmic contacts on both n-type and p-type silicon carbide—depending on the relative percentage of the three elements used [102]. In the case of MOSFETs this property could prove to be beneficial because it would reduce the size of the device and might improve fabrication process[102]. The focus here will be on the Schottky behavior of Ni/Ti/Al contact on n-type 4H-SiC. We believe that the simultaneous formation of Ni/Ti/Al based Schottky and ohmic contacts on n- and p-type SiC, respectively, will further simplify the fabrication of devices like JBS and MESFETs. Below we will discuss the experimental setup and the electrical characteristics, along with a discussion on the X-ray diffraction results, of Ni/Ti/Al Schottky diodes.

#### Device Fabrication

Similar SiC wafers were used for the fabrication of these diodes as mentioned in the beginning of this chapter. Schottky barrier diodes were designed with a $p^{+}$-type guard ring and a mesa-type structure with an additional silicon dioxide ($SiO_2$) passivation layer. Boron ion implantation was used for the formation of the $p^{+}$-type guard ring. This step was followed by a Rapid Thermal Process (RTP) at temperatures exceeding 1500 $^{o}$C, in order to promote lattice damage recovery and to achieve a reasonable electrical activation of the implanted $B^{+}$ ions.

The silicon dioxide passivation layer was grown by means of a Low Temperature Oxidation (LTO) process, using TetraEthylOxySilane (TEOS) as precursor. The $SiO_2$ layer was patterned using standard UV photolithography, and etched by a buffered HF-based so-

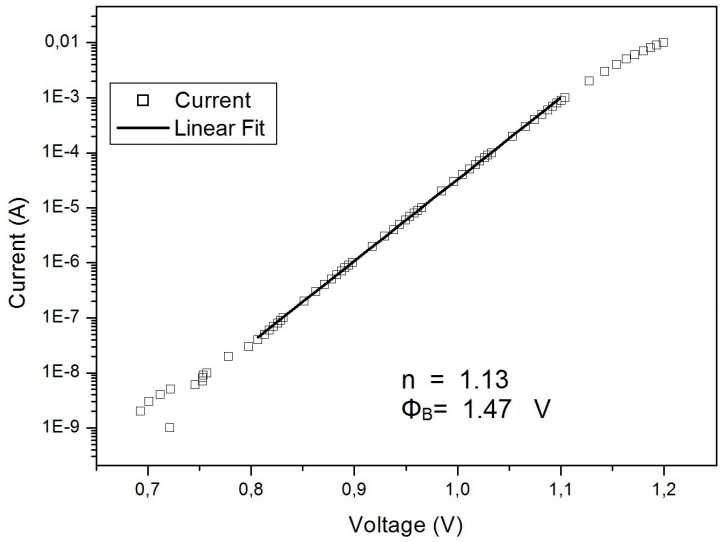


Figure 6.16: Forward I-V ($lnI$ vs. $V$) characteristics of Ni/Ti/Al SBD annealed at room temperature.

lution. The Schottky contact was then realized by the deposition of a Ni/Ti/Al triple layer (with respective thicknesses of 20, 50 and 150 nm) on the 4H-SiC epilayer surface. The Ni/Ti/Al deposition was followed by an annealing treatment performed at 800 $^{o}$C in inert atmosphere. The ohmic contact was obtained on the wafers backside by means of a triple layer of Ti, Ni and Ag, without the need of a post-deposition annealing. The deposition of both the Schottky and the ohmic contacts was performed using an electron beam evaporator (ULVAC model EBX-14D), at a pressure of about $10^{-5}$ Pa.

The electrical characterization of the SBDs was performed by acquiring the current-voltage (I-V) curves using Keithley 237 and 238 SMUs. The capacitance-voltage (C-V) characteristics were acquired by means of a HP4192A impedance analyzer.

#### Electrical Characterization

With the help of thermionic emission theory electrical parameters such as Schottky barrier height, SBH (denoted by $\Phi_B$) and ideality factor n, were extracted. Figure 6.16 shows forward bias current-voltage (I-V) characteristics of one of our diodes at room temper-

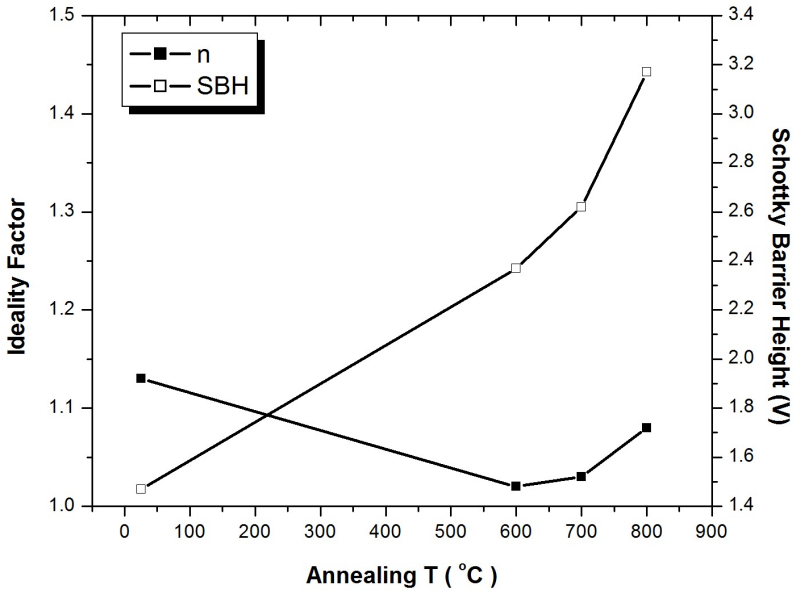


Figure 6.17: I-V SBH and ideality factor vs. annealing temperature

ature—on a semi-logarithmic scale. Schottky barrier height (extracted from the intercept) for this diode comes out to be 1.47 V while ideality factor n (extracted from the slope) is 1.13.

It is clear from Fig. 6.16 that there is no excess forward current for this diode. This indicates a rather homogeneous Schottky barrier as compared to some other diodes that we characterized. All these diodes show non-ideal behavior and abnormal I-V characteristics with excess forward current at low voltage that indicates inhomogeneous Schottky barrier. Figure 6.17 shows both $\Phi_B$ and n in relation to the annealing temperature, general trend shows an increase in the SBH with annealing temperature. For diode without annealing the SBH values are close to the commonly accepted values for Ni/SiC Schottky barrier but at annealing temperatures of 600 $^o$C and above the diodes show bad rectifying behavior and high Schottky barrier heights as reported also by Kestle et al. in the case of Ni/SiC Schottky diodes[103]. The ideality factor shows a decline with increasing annealing temperatures which indicates an improvement in the quality of the diodes at high annealing temperatures. The diode which was not annealed shows best Schottky behavior out of all the diodes characterized. The diode annealed at 800 $^o$C shows very poor Schottky behavior with ideality factor

of 1.08 and SBH of 3.17 V. The increasing trend in SBH accounts for the varying quality of Schottky contact which is deteriorating at high annealing temperature, this behavior is contrary to the normal where diodes tend to perform better after getting annealed at high temperatures [104].

The interesting thing about these non-ideal diodes is that they were all annealed at temperatures as high as 800 $^{o}$C. One possible explanation of this behavior could be the presence of $Ni_2Si$ in the samples annealed at 800 $^{o}$C. $Ni_2Si$ itself forms a Schottky contact on n-type silicon carbide[94]. $Ni_2Si$ may exist as an independent Schottky contact, alongside, Ni/Ti/Al which can affect the I-V characteristics in a manner similar to that of two different Schottky barriers present in the same diode. If this is the case then the barrier lower in height will certainly result in excess current and anomalous current-voltage characteristics. To avoid any chemical reaction between Ni and Si low annealing temperature should be preferred because only at high temperature (800 $^{o}$C) $Ni_2Si$ was present. Peaks related to $Ni_2Si$ could be observed in the XRD profiles obtained for the sample annealed at 800 $^{o}$C, as discussed in the following section.

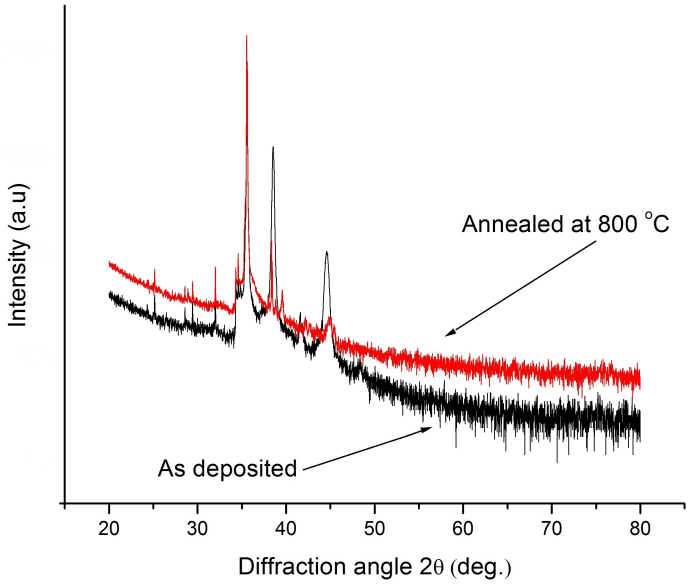


Figure 6.18: X-ray diffraction spectra of Ni/Ti/Al Schottky contacts.

#### X-Ray Diffraction Analysis

XRD data of Ni/Ti/Al contacts as deposited and annealed at 800 $^{o}$C were achieved using PANalytical's PW 3020 set. Figure 6.18 shows XRD spectra for both the samples. Most of the commonly observed peaks, normally present in such ternary contacts, were also found in our samples. Phases of Ni (111), Ti (002) and Al (200) were all present in the sample annealed at 800 $^{o}$C. $Ni_2Si$ was the only compound that we were able to observe. The presence of $Ni_2Si$ was detected only in the sample that was annealed at 800 $^{o}$C.

## 6.3 Summary

In this chapter Schottky barrier inhomogeneity was discussed. Various Schottky barrier diodes were characterized for analysis of Schottky barrier height. Almost all the diodes showed inhomogeneous Schottky barrier. Classical thermionic emission theory fails to account for inhomogeneity in the Schottky barrier and leads to incorrect results with abnormal theoretical current-voltage characteristics and very low values of Richardson constant. After considering modifications in thermionic emission theory, proposed by Tung, it was possible to achieve better results. Very good agreement between experimental data and the data calculated by Tung's model was seen together with nearly correct values of Richardson constant. It was observed that the actual area involved in the current transport process was much different than the geometrical area of the diodes. Important outcomes of this research are highlighted in the next chapter.

# Chapter 7

# Conclusions

In this PhD thesis electrical characterization of various Schottky barrier diodes based on silicon carbide is presented. Silicon carbide is a wide bandgap semiconductor with excellent electrical and thermal properties. Electronic devices based on silicon carbide such as Schottky diodes, MOSFETs, MESFETs and static induction transistors find applications in various important technological fields due to their ability to perform at high temperatures and high voltages. In addition, silicon carbide based electronic devices can handle high power densities which makes them a better candidate for high power electronic devices; their applications range from power conversion in everyday use home appliances to microwave, avionics, hybrid automobiles, radars and military hardware. Because of its importance huge research activity can be seen these days which is focused either on silicon carbide growth or device testing. Progress has been made in the growth of high quality silicon carbide wafers available at affordable price, however much has to be done in this regard. Silicon carbide based devices show abnormal electrical behavior which is also a point of concern for researchers.

Generally the abnormal electrical behavior is attributed to the inhomogeneous metal-semiconductor interface. Although some researchers have tried to fix this problem and have come up with a number of different explanations but the problem persists and needs more attention. In this thesis work one such try is made in order to understand the electrical behavior of silicon carbide based Schottky barrier diodes. Thermionic emission theory is applied to model the forward current-voltage characteristics together with some modification proposed by R. T. Tung.

Three of the diodes characterized were applied Tung's theoretical model in order to fit the forward current-voltage characteris-

tics. Two diodes were fabricated with molybdenum Schottky contact while one with titanium Schottky contact. All three diodes were of the same size i.e. 0.0305 $cm^2$. Almost all the diodes showed anomalous electrical behavior typical of Schottky diodes with inhomogeneous Schottky barrier heights.

Anomalous behavior is evidenced by abnormal forward current-voltage characteristics, greater than unity ideality factor, temperature dependence of the ideality factor and excess leakage currents. All these anomalies are explained by considering the Schottky barrier to be inhomogeneous. Nanometer scale spatial variation of the Schottky barrier can be due to the presence of low barrier height patches thought to exist alongside high uniform Schottky barrier. In case of isolated low barrier height patches the current can be assumed to be the sum of all current components from these individual patches. In case of interaction between two closely located patches pinch off occurs and the patch with low barrier height is supposed to be pinched off. Important outcomes of the research are highlighted below:

- Total number of low barrier height patches was calculated for each diode at various temperatures and was found to depend on the characterization temperature. Usually number of patches is small at high characterization temperature and large at low characterization temperature.

- Schottky barrier height was measured for all three diodes at various characterization temperatures ranging from 77 K to 450 K. The barrier height values are in agreement with recently published works of similar nature.

- Ideality factor was also calculated for all diodes. The ideality factor values are generally close to unity which indicates a better underlying Schottky contact quality.

- Temperature dependence of the ideality factor was also observed alongside $T_o$ effect in some diodes.

- Richardson constant was calculated for all diodes with values close to generally accepted value for 4H silicon carbide.

- Good agreement was seen between experimental current-voltage plots and theoretically calculated current-voltage characteristics.

- In future we are planning to apply other theoretical models together with performing ballistic electron emission microscopy (BEEM) study of the metal-semiconductor contacts.

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