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Majority Voter Full Characterization for NanoMagnet Logic Circuits

Marco Vacca, Mariagrazia Graziano, *Member, IEEE,* and Maurizio Zamboni

***Abstract*—The recently proposed NanoMagnet based Logic (NML) represents an innovative way to assemble electronic logic circuits. The low power consumption, combined with the possibility to maintain the information stored without power supply, allows to design low power digital circuits far beyond the limitations of CMOS technology.**

This work is focused on the key logic block of NanoMagnet based Logic, the Majority Voter (MV). It is thoroughly analyzed through detailed micromagnetic simulations, changing the geometrical parameters, and detecting logic behavior, timing performance and energy dissipation. Our analysis enables to derive important results, substantially enhancing the practical knowledge of NML. First, we demonstrate that NML circuits can be effectively fabricated not only using Electron Beam Lithography, but also using high-end optical lithography without loosing performance. This is a promising opportunity for the future of this technology. Second, we demonstrate the robustness of the MV considering process variations and extracting useful guidelines for its technological implementation. Third, we show how, and how much, the alteration of magnets sizes and distances affect timing and energy consumption. Finally, fourth, we outline the problematic fabrication of the gate with real clock wires, and propose a modification that enables the fabrication of working gates, remarkably enhancing the possibilities of this technology.

***Index Terms*—Quantum Dot Cellular Automata, Nano Magnetic circuits, Micro Magnetic simulation, process variations**

I. Introduction

In the NanoMagnet based Logic (NML) digital values are represented using single domain nanomagnets (Fig. 1.A). If magnets are sufficiently small and are rectangularly shaped, they can assume only two stable magnetization states used to represent the logic values '0' and '1' [1]. Circuits are built placing magnets one near each other. Information propagates using the magnetic interaction among neighbor magnets. The basic logic gate is the Majority Voter (MV, Fig. 1.B), comprised of three input magnets surrounding a central element which performs the logic operation (see sec. II for background on NML). The value of the output magnet is equal to the value of the majority of the three inputs [1].

Although the maximum allowed frequency of this technology is low [2] (about 100 MHz if all constraints are taken into account, compared to THz for the molecular nearest counterpart [3]), NML is interesting because the expected power consumption is much lower than in CMOS circuits (about 100 times less) [4]. Moreover, due to their magnetic nature, they maintain the information stored also without power supply. Therefore this technology offers the possibility to combine logic and memory in the same device. As a consequence new way of developing logic circuits and their applications can be explored, with the possibility to further reduce power consumption.

Many works in the literature analyze the behavior of the basic blocks of this technology and, in some cases, how these blocks are influenced by magnets shapes and positions. [1], [5], [6], [7]. However, no previous study considers with a thorough analysis the impact of the variation of some important parameters, as i) the distances among neighbor magnets, ii) the sizes of the magnets themselves, iii) the impact of these parameters on their switching time and energy consumption, and iv) the relations between the previously mentioned parameters and the clock physical organization. In this work, starting from our preliminary contribution in [8], we study the MV using low level micromagnetic simulators, OOMMF [9], and in particular NMAG [10], which allows not only a behavioral analysis, but also enables to extract quantitative data on timing and energy performance.
We simulate (section III) the gate in various conditions where we change distances among neighbor magnets, as well as their aspect ratio. The purpose of this analysis is to verify whether these circuits can be built using lithographic techniques that have a low resolution, are fast and allow for high volume production (i.e. Ultra Deep Ultraviolet Lithography). We then analyze how the MV behaves considering process variations (in section IV), because a good rejection process related errors highly increases the chances of using this technology. We also study (section V and VI) how the most important features of the gate, timing and energy dissipation, change due to variations in magnets sizes and distances. Finally, we discuss (in section VII) issues related to the fabrication of realistic gates considering the real structure of clock wires. We propose a modification of the clock wires and we achieve a solution that assures to obtain gates that correctly work without the need of complex magnets organization as previously proposed.

II. Background

The correct signal propagation in the NML circuit requires an adiabatic switching [11]. For this purpose, a slowly rising external magnetic field, called clock, is applied to the magnets. This field is directed along the short side of the magnets, and forces them in an intermediate unstable state. When the field is released, nanomagnets start to realign following the magnetization values of the inputs, propagating the information

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along the circuit. This field is normally generated by a current which flows through a wire buried under the magnets plane. This might have a not negligible impact on the whole circuit power consumption, but the solution proposed in [4] has the potential to notably reduce it. Recently, a novel approach has been proposed [15] which would change the clock structure organization. Though this method is worth analyzing, it requires further studies before assessing its superiority to the structures proposed up to now.

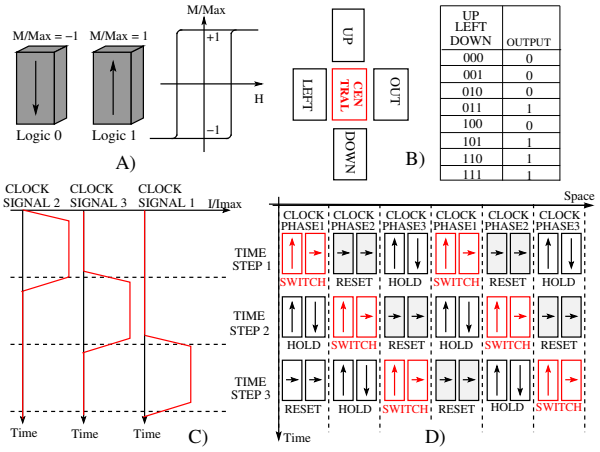


Fig. 1. A) Nanomagnets with their hysteresis cycle, logic bits are represented by the two stable magnetizations. B) Majority voter and its truth table. Three input blocks surround a central element which performs the logic operation. C) Clock signals waveforms, overlapped to assure a correct information propagation. D) Magnetic signal propagation. At every time step, for each group of three clock zones, magnets of one zone are in the SWITCH phase. Magnets of the zone on the left are in the HOLD phase and behave like input for the switching magnets. Magnets of the clock zone on the right are in the RESET phase and have no influence on the switching magnets.

According to the previously mentioned clock organization, to propagate the information in a circuit of realistic complexity, a multiphase clock system is necessary [12]. Circuits are divided in small areas, called clock zones, where only a limited number of magnets is allowed [13]. A different clock signal is applied to every clock zone (Fig. 1.C). At least three overlapped clock signals are required for a correct information propagation, as we demonstrated in [14] (see Fig. 1.C). During each time step magnets of one clock zone can be in one among three different states (Fig. 1.D). In the SWITCH state the magnetic field is removed and magnets tend to realign in an antiferromagnetical order. Magnets of the LEFT clock zone are in the HOLD state, i.e that no field is applied and they act like input for magnets in the SWITCH state. At the same time magnets of the clock zone on the right are in the RESET state, i.e. the external field is applied, and they have no influence on switching magnets because they are in an unstable state. In the next time step the situation is the same but spatially shifted and the switching magnets are the ones in the next clock zone. This situation is periodically repeated for each group of three clock zone allowing the information propagation.

III. Majority Voter Characterization

The simulations here performed have as a target the verification of the correct alignment of the MV magnets magnetization when they move from the RESET to the HOLD phase through the SWITCH phase (see Fig. 1.D). Achieving the correct magnetization is not straightforward for a gate like MV, and depends on magnets shape, distances and material properties. Clearly, an incorrect alignment corresponds to a logic error. The sequence of steps are reported in figure 2. After the application of a strong enough horizontal magnetic field (for example 100000 A/m), magnets are forced to assume the RESET state. The field is then removed, and magnets reach the equilibrium magnetization. It is worth underlining that the signal used in the simulation is an ideal step, while the real clock signal should be a ramp as shown in Fig. 2 (dashed line). The necessity of using a ramp instead of a step in the real case comes from some considerations that are not directly connected to the gate behavior. First, to reduce the

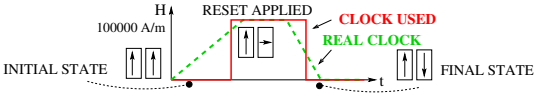


Fig. 2. Real clock signal and clock signal waveform used in the simulation.

energy necessary for the magnet to switch, it is important to favor the so called adiabatic switching [11]. This means that the clock signal should have a rise time of at least 8-10 ns [4]. Further details on this point will be given in section VI. Second, due to thermal noise [13], the maximum number of magnets in a clock zone must be limited. As shown in [13] if the number of magnets is higher than 5, a long fall time is necessary to assure that magnets switching occurs with a reduced probability of error. However, with a limited number of magnets in sequence (less then five [13]) it is allowed to use an abrupt switching, i.e. a very short fall time. So in this case there is no difference between the real clock and the ideal clock, because we are interested only in the behavior of the gate in which the number of magnets is limited. As a consequence, an ideal clock signal was used in the simulations, in order to keep simulations simpler and faster.

The majority voter structure used in the simulation is shown in Fig. 3.A. The majority voter (included in the rectangular box in Figure 3.A) is composed by three inputs magnets (TOP, LEFT and BOTTOM, according to figure 1.B) and one CENTRAL block, which performs the logic operation. Three fixed magnetization blocks (outside the rectangular box) are here used to simulate the multiphase clock system (i.e. the final magnets of the previous clock zone here outside the inner box) and to force the real inputs of the majority voter. It is important to notice that when magnets are horizontally coupled there is an inversion in the signal, while vertically there is no signal inversion. Therefore the fixed magnet used to force the central input (fixed input on the left) must be inverted respect to the input that we want to force. If the input combination is “110”, the values of the fixed (external) magnetization elements must be “100”. For the same reason the value of the CENTRAL block is equal to complemented value of the majority of the among the three inputs. The value of the OUTPUT block (on the right) is instead equal to the value of the majority of the inputs. In Fig. 3.A the relaxed state of the structure is displayed when the inputs (internal) configuration is “110” (i.e. top input

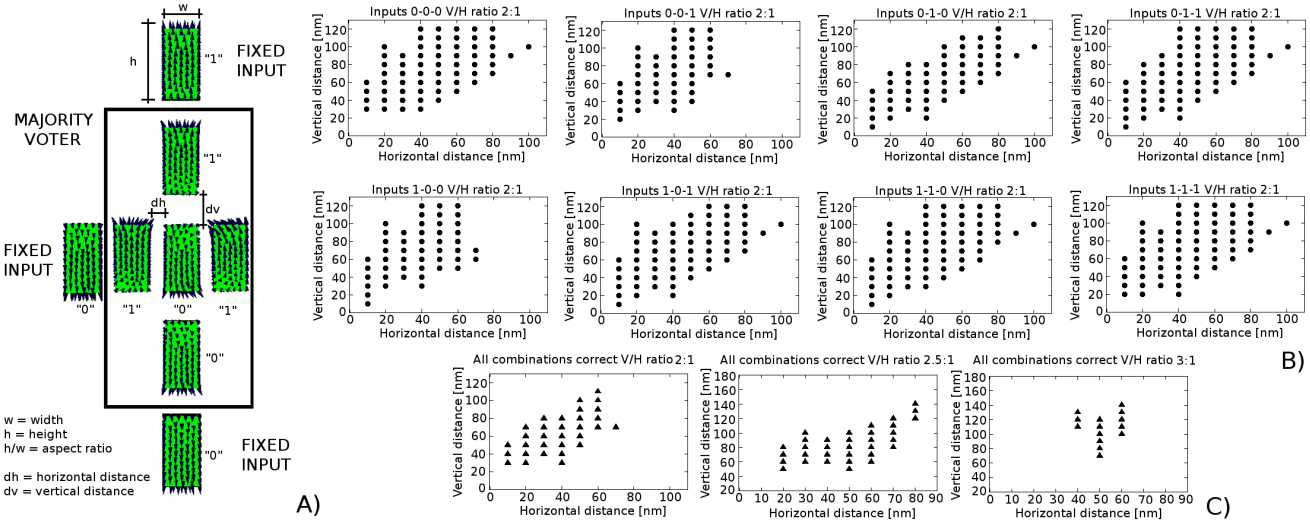


Fig. 3. A) NMAG simulation that shows the Majority Voter (MV) configuration used for this characterization. Fixed magnets are used as inputs for the MV. Horizontal and vertical distances and aspect ratio are changed to verify the MV operating area. B) C) MV working area with the variation of the horizontal and vertical distance. B) Working area for every inputs configuration. C) Complete working area with magnets with an aspect ratio of 2, 2.5 and 3

has up magnetization, central input has up magnetization, and bottom input has down magnetization). Magnets used in the simulation are 20 nm thick permalloy parallelepipeds, their width is 50 nm and their height is 100 nm.

According to literature, to obtain a properly working gate, distances among magnets must be kept as small as possible [1]. This requires the use of Electron Beam Lithography which is too slow to be used for mass production of chips. If we want to cope with a rapid production technique, Deep Ultraviolet Lithography should be used instead, that, on its turn, does not guarantee reproducible distances within a certain range. As we want to explore how NML can tolerate the effect of using high end lithography, the gate was simulated parametrically increasing horizontal and vertical distances among neighbor magnets. The aim of these simulations was to verify if the MV still works correctly when the distances are different with respect to the expected one. Therefore, for each of the eight inputs configurations the gate was simulated with different values of horizontal (dh in figure) and vertical (dv in figure) distances. Results are shown in Fig. 3.B (top two rows of pictures). For each input configuration a map is reported in a different graph. The input configuration is detailed on the top of each picture. Each point of the map represents a combination of distances that allows the gate to behave correctly. We observe that every input configuration has a different working area. In particular, some configurations have a smaller working area than others (for example input case 001 compared to case 111). This is due to the influence of magnets in the reset state on misaligned elements. This is explained in the following with the support of Fig. 4. If two magnets are forced in the unstable RESET state, but they are perfectly aligned (Fig. 4.A), the magnetic flux lines (schematically represented by the lines in Fig. 4) are perfectly symmetric. As a consequence they are kept in the unstable state by the presence of the neighbor dots that hold the same situation. They remain in this state until one of the neighbor magnets changes to the stable state due to the presence of an input magnet. However, if a magnet is misaligned (Fig. 4.B) the situation is more complex. As clear from the simplified representation of the magnetic flux lines in Fig. 4.B, the magnetic flux is not symmetric and the length of the flux lines is not as short as possible. For this reason the misaligned dots turn down, as the length of the flux lines is shorter (Fig. 4.C). Shorter flux lines mean that the global energy of the system is lower, and the situation more stable. Then, when magnets are misaligned, there is a switching that is not due to the logic signal propagation, but to the influence of magnets in the reset state. This problem is normally solved [16] adding shielding blocks (Fig. 4.D in grey), that are always magnetized along the x-axis, keep the misaligned dots in the RESET state until one of the neighbor dots assumes a valid logic value. Shielding blocks tend to slow down circuit operations, therefore they were not used in this work as we were interested to verify the maximum circuit speed (see section V). This problem leads to the consequence that one of the two logic values (logic '0', magnetization pointing down) is easier to reach, and this explains why every input configuration has a different working area.

By merging all the maps of figure 3.B together, we obtain the final MV working area, which is reported in Fig. 3.C on the left. The gate behaves correctly even in presence of horizontal and vertical distances of 50-60 nm. Magnetic dots with distances of 50 nm where already obtained using Ultra Deep Ultraviolet Lithography [17]. This demonstrates that a resolution of 50 nm can be already obtained with optical lithography. This is very promising for the future developments of this technology as opens it to less niche applications with respect to what envisioned up to now.

One important magnet characteristic is the aspect ratio (a.r.), i.e. the ratio between the vertical height (h) and the horizontal width (w) of the magnets (Fig. 3.A). We demonstrated by micromagnetic simulations that, at least in the MV case, it

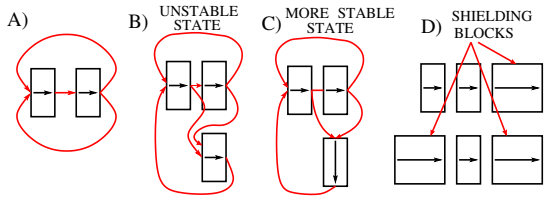


Fig. 4. Reset problem. A) Perfectly aligned magnets. Magnets maintain the (unstable) RESET state due to the perfect alignment of the neighbors magnets. The red lines (magnetic flux) are perfectly symmetric. B) Misaligned magnets. Magnets are not in the minimum energy state. C) The misaligned element turn down due to the influence of the neighbor magnets in the RESET state. Magnetic flux lines are shorter therefore in this situation the total energy of the system is lower. D) Shielding block used to keep the misaligned elements in the RESET state, until the neighbor magnets go in a stable state.

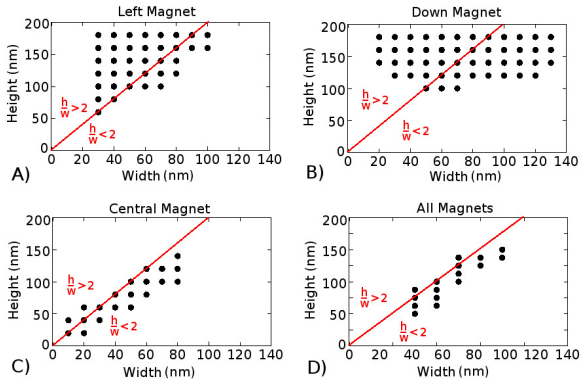


Fig. 5. Majority voter working area considering process variations. Red line represent the a.r. 2. A) Sizes variation of the left magnet. B) Sizes variation of the down magnet. C) Sizes variation of the central magnet. D) Sizes variation of all the magnets together.

seems more convenient, in order to tolerate variations, not to reduce the a.r. below 2. However it can be increased, with the byproduct of increasing the noise immunity of the magnets (although it is good even with a 2 a.r., see section VI), and making the fabrication of dots easier since they are bigger. The same simulations performed for the 2 a.r. were repeated for an a.r. of 2.5 and 3. In figure 3.B, central and right pictures report the merged working area of all inputs configurations for the 2.5 and 3 a.r., respectively. For an aspect ratio of 2.5 the working area of the majority voter is similar or slightly bigger with respect to the 2 a.r., while for bigger increments the working area is greatly reduced. This happens because the magnets energy barrier depends on their a.r (see section VI for further details). Therefore if the a.r is changed the magnetic interaction among neighbor magnets is drastically altered.

IV. Impact of Process Variations

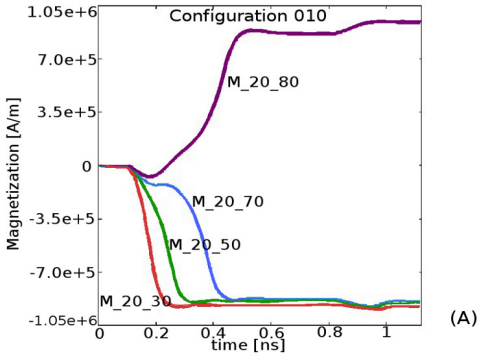
Since the magnetic interaction among magnets strongly depends on magnets distances and sizes, process variations may have a notable influence on the gate behavior. The process variations considered here are related to changes in magnet sizes. In particular, magnets width and height can be different with respect to the one defined at the design stage. Two types of process variations were analyzed: local mask, i.e. substrate defects that lead to differences in sizes of only one magnet of the MV, and global errors, like under/over etching that leads to same sizes variation for all the magnets together. All possible combinations of width and height of magnets were considered in this analysis, from few tenths of nanometers to the maximum possible sizes in which magnets are merged with their neighbors. Simulations are performed considering a 2 a.r. and using the 001 input configuration, which is the most critical as noticed in Fig. 3.A. Results are shown in Fig. 5. Each map represents a combination of widths and lengths that correspond to a proper gate operation. Fig. 5.A shows the impact of sizes variation only of the MV LEFT input magnet (see Fig. 1.B to better understand the position of each magnet). The gate still correctly operates in the 30-100 nm range for the width and in a 60-180 nm range for the height. However, results in Fig. 5.A clearly show that the a.r. should better remain near 2 (the straight line on the map) or higher for a good rejection to process variations. With smaller a.rs the gate does works correctly only in a limited set of combinations. Fig. 5.B, instead, shows the influence of the sizes variation of the DOWN input magnet on the whole gate behavior. Differently from the previous case, here the gate is not influenced by the a.r. It works with all the width values, provided that the height is at least 100 nm. This means that in case of the DOWN magnet the key factor is the height and not the shape of the magnet, because with sizes of 120 nm width and 120 nm height the magnet is a square instead of a rectangle. The influence of the UP input magnet is not reported because it has the same behavior for symmetry. Fig. 5.C shows the effects of sizes variation of the central magnet, which is responsible for the logic computation. The MV is more sensitive to process variations. Indeed, it does not work with too high width values. Moreover, sizes of the magnet can change, but the aspect ratio should remain around 2, or be slightly smaller, to assure the correct gate operations. Fig. 5.D shows the influence of the same process variation applied to all the magnets together. This is a quite common case in the technological processes, as it happens for example in case of under/over etching. Variations of this kind apply in the same way to all the elements. In this case the gate is much more sensitive to process variation than in other cases. The working area is smaller and it is related to the a.r. Sizes can change but again with an a.r. around 2 or slightly lower. Moreover, if the width of the magnets becomes too small, e.g. under 40 nm, the gate risks not to work properly. These simulations show that this logic is quite robust in case of process variations. If the variation is not too big, logic gates still correctly work. The key factor is the a.r. that must be kept near 2 or slightly smaller, in order to reduce the probability of errors. Process variations that affect all the magnets are the most troublesome, but fortunately they can be compensated quite well by correctly setting up the technological process.

V. Timing Analysis

To evaluate how the changes in the horizontal and vertical distances values affect performance, the 50% delay of the gate was measured. In case of NML technology it is the delay between the 50% of the variation of the clock signal (during the fall ramp when the switching can start) and the 50% of the variation of the magnetization of the CENTRAL block. This

CENTRAL block starts with a '0' magnetization value, and moves to a negative (down arrows) or positive (up arrows) values according to the inputs combination. This definition is similar to the CMOS propagation delay, and allows to evaluate NML performance according to standard metrics. A sample of the waveforms obtained by NMAG is shown in Fig. 6.A, showing the CENTRAL block magnetization with time.

Simulations are performed considering the 2 a.r. case, varying horizontal and vertical distances. In Fig. 6.A different waveforms are presented. All of them are obtained with an horizontal distance of 20 nm (the first number after the 'M' near each curve), and for different values of vertical distance (the second number near each curve), considering the input configuration 010. It is interesting to notice that the delay is in the order of few hundreds of picoseconds, and it increases with the vertical distance. If the vertical distance becomes too high (i.e. 80 nm) the final state of the central magnet is wrong (magnetization becomes positive instead of negative), according to the map of Fig. 3.A.



Inputs	Vertical Distances (nm)		
ABC	30	50	70
000	90ps	130ps	160ps
001	230ps	130ps	210ps
010	100ps	140ps	260ps
011	210ps	200ps	200ps
100	240ps	230ps	210ps
101	100ps	120ps	220ps
110	210ps	200ps	200ps
111	110ps	120ps	150ps

(B)

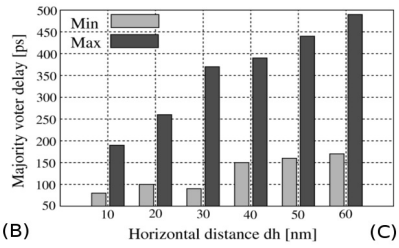


Fig. 6. Timing simulations. A) Timing variation of the central magnet magnetization in a few cases (different waves) of vertical and horizontal distance for the input configuration of 010. The waves label first number represents the horizontal distance while the second number identifies the vertical distance. Different waveforms are presented: In the first three the gate works properly, and in the last one the behavior of the gate is wrong as magnetization is expected to go to a negative value (logic 0) but goes to a positive value (logic 1). B) Timing variation with three values of vertical distance for the each input configuration, considering an horizontal distance of 20 nm. C) Timing variation of the gate. For each value of horizontal distance the minimum and maximum values of delay, measured among all the input configurations and all the vertical distance, are reported.

Table 6.B shows the delay values measured considering an horizontal distance of 20 nm and three different values of vertical distances: 30 nm, 50 nm and 70 nm, reported for each of the eight input configurations. The variation of the delay with the increment of vertical distance depends on the input configuration. With some input configurations the delay shows small variations (considering the relatively high tolerance on the measured values), while with other input configurations the delay considerably increases. This behavior is due to the "reset problem" explained in section III, which leads to the consequence that the logic value '0' is easier to reach.

To better figure out the relations between MV timing and distance variations, values can be properly grouped together. Fig. 6.C shows, for each value of horizontal distance (x axis), the minimum and maximum delays measured among the simulations obtained changing all the possible input configurations and all the values of vertical distances. Results show that the average value is between 100 ps and 300 ps, and it increases with the increment of horizontal distance. As a consequence of this analysis we can conclude that distances must be kept as small as possible, in order to improve the overall circuit speed. However, it is worth noticing that the clock frequency does not depend on the gate delay, because it is determined by others factors: The long rise time necessary for adiabatic switching to reduce power consumption, the high fall time in case of more then 5 magnets for clock zones and also the necessity to use a three phase overlapped clock system. The delay determined here represents the lower bound of this technology, and it will lead to a maximum allowed clock frequency of about 1 GHz. Considering all the other constraints, if the mentioned issues will not be solved, the obtainable clock frequency is expected to be between 10 MHz and 100 MHz [2].

VI. MV ENERGY ANALYSIS

Similarly to what done for the gate timing simulations, we used NMAG to evaluate the power consumption of the majority voter. There are two main contributions to power consumption in NML technology: clock system losses and intrinsic energy consumption necessary to force magnets in the RESET state. Clock system losses cannot be evaluated using Micromagnetic simulators. They can be estimated using other methods as we proposed in [14]. Considering the best clocking solution proposed [4], clock power losses can be estimated of the same order of the intrinsic energy consumption [18] [19]. The intrinsic energy consumption, instead, depends on the energy barrier of the magnets. The energy barrier is the difference between the magnets energy in the unstable state and the magnet energy in the stable state. The intrinsic energy consumption is equal to the value of the energy barrier (multiplied for the total number of magnets) if an abrupt switching is adopted. A very short rise time for the external magnetic field (one hundred picoseconds) allows the magnets to be forced into the RESET state correctly, but the energy necessary to switch the magnets is equal to the whole energy barrier. If, on the contrary, an adiabatic switching is adopted, which means a rise time of at least 8-10 ns, the intrinsic energy consumption is smaller than the energy barrier [4]. If the rise time is increased, the energy consumption decreases, and it can be reduced until it reaches the minimum value of 30-40 KbT [4], independently from the original energy barrier.

Following the maps of Fig. 3 it is possible to evaluate the average energy barrier of the MV magnets for all the distances. Results are shown in Fig. 7.A. For each horizontal distance value (x-axis) the minimum and maximum energies are reported. The minimum value of barrier is obtained when

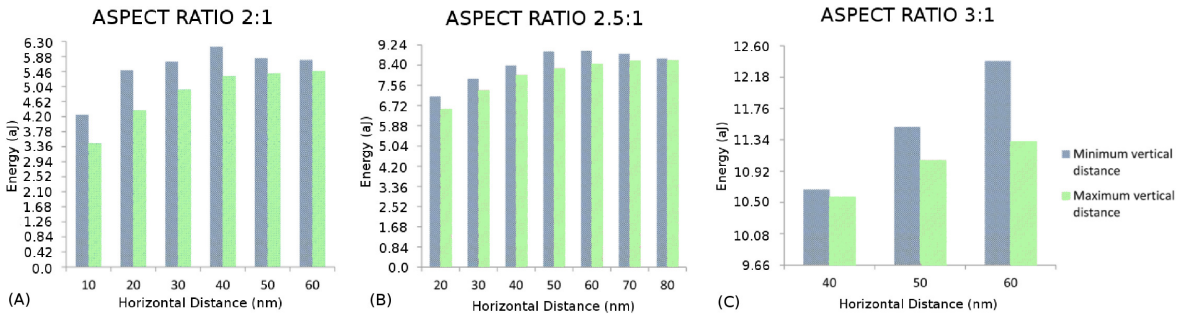


Fig. 7. Power analysis with all the possible inputs configurations, vertical and horizontal distances. A) a.r. 2. B) a.r. 2.5. C) a.r. 3.

the vertical distance is maximized, while the maximum energy value is obtained for the minimum value of vertical distance. Moreover, when the horizontal distance is risen, the energy barrier increases, but it shows a saturation with horizontal distances higher than 50 nm. This behavior can be explained considering the composition of the energy barrier. It has, indeed, two components. The first one depends on the volume of the magnets and its physical properties (demagnetization energy). The second one depends on the interaction with neighbor magnets (exchange energy), which contributes to a reduction of the overall value of the energy barrier. The interaction between horizontally coupled magnets is lower than the vertical one. Moreover, horizontal interaction increases when the distance is enlarged, while vertical interaction decreases. Therefore, the value of energy barrier can be reduced if the horizontal distance decreased and the vertical distance increased. When distances become too big the contribution of the exchange energy drops to zero, and the value of the energy barrier becomes constant and equal to the demagnetization energy. Fig. 7.B shows the variation of the energy barrier considering a 2.5 a.r. The general trend is the same but the absolute values are different with respect to the 2 a.r. case. With an horizontal distance of 50 nm the energy barrier increases from 5.2 aJ to 8 aJ. This happens because the value of the demagnetization energy depends on the volume of the magnets but also on the a.r. Increasing the a.r. the energy barrier rises, as well as the noise immunity. However this also causes higher power consumption if an abrupt switching is adopted, or means lower clock frequency in case adiabatic switching is the choice. Outcomes are similar if the a.r. of 3 is used (Fig. 7.C). The general trend is again the same but the absolute value is notably risen. With a width of 50 nm the value of the energy barrier is 11 aJ. This means that with an increment of the a.r. from 2 to 3 (50%) the value of the energy barrier is doubled.

We can derive now a few conclusions. First, the value of the energy barrier can be considered independent of magnets distances, if magnets are fabricated using Deep UV lithography, which means distances of 40-50 nm. Second, the a.r. must be kept as small as possible to reduce the absolute value of energy barrier and to increase the clock frequency, in case the adiabatic switching regime is chosen. By increasing the a.r., the noise immunity also is improved, but with an a.r. of 2 the noise immunity is quite high as well. An energy barrier of 5,2 aJ, for example, corresponds to 1250 KbT, which is much higher than the value of 40 KbT, the minimum value necessary to assure the thermal stability and a low error probability. Third, a final note can be done on magnet sizes. If technology allows it, in case magnet sizes are reduced at least to a width of 15 nm, a height of 30 nm height, and a thickness of 5 nm, the value of the energy barrier decreases to 40 KbT. In this case it is possible to use an abrupt switching, obtaining clocking frequency of 1 GHz, and thus minimizing at the same time power consumption.

VII. Majority voter inputs extension

The classic MV analyzed in this work requires that all the inputs arrive at the same time. For this to happen the clock zone should be limited to exactly the size of the majority voter. However a feasible normal clock signal is generated using parallel wires placed under the plane of the magnets. In this case, inputs are required to come from the same direction as shown in Fig. 8.A. The left picture in the dashed box shows the structure in a simple sketch, the right picture shows the result obtained by a OOMMF simulation [20] in the same configuration. This magnets organization is problematic because, while in the classic case (Fig. 1.B) the length of every input arm of the gate is equal, in this case the length of the upper and lower arms is bigger, due to the presence of an angle. The consequence is that the left input signal arrives before the others two, and the gate does not work properly in all the configurations. Moreover, while the classic majority voter can work also without the use of shielding blocks, in this case they are mandatory. A possible solution is presented in Fig. 8.B [20], where the length of the arms are equalized reducing the number of magnets in the upper and lower arms, placing them at an higher distance. Another alternative solution is sketched in Fig. 8.C [20] where the number of magnets is increased in the left arm, using smaller magnets. Again, simulations show that both these solutions do not give the expected results in all the configurations. The structure of NML circuits must be symmetric with magnets of the same sizes, and possibly with the same distances. A further possible solution is presented in Fig. 8.D [20], where dots are misaligned. Simulation shows that this solution does not work due to the “reset problem” described in section III, and to the impossibility to to place shielding blocks due to lack of proper space.

These simulations highlight a characteristic of NML circuits: they must be as much symmetric as possible, with mag-

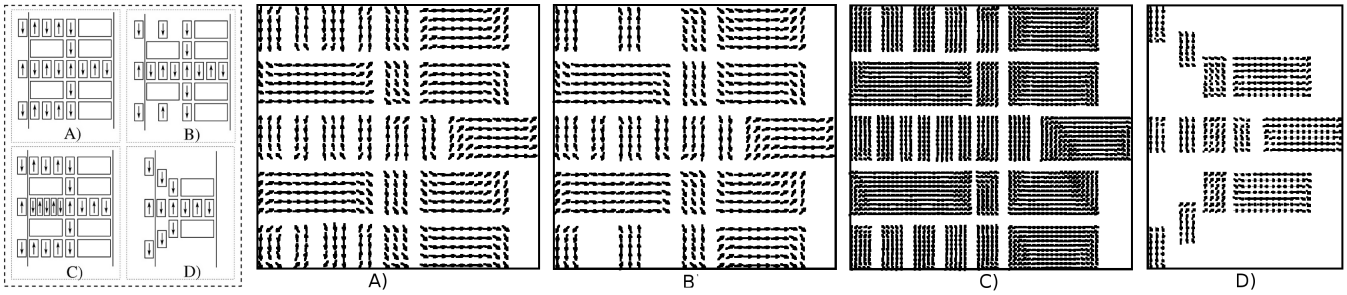


Fig. 8. Majority voter possible solutions with inputs coming from one direction. Left pictures in the squared box: a sketch to clearly show the magnets organization and magnetization. Right pictures: OOMMF simulation of the same configuration. A) Classical structure with inputs extended. B) Reduction of the number of elements in the up and down arm. C) Increment of the number of elements in the central arm, making them smaller. D) Displacement of the corner elements to equalize the number of magnets in each arm.

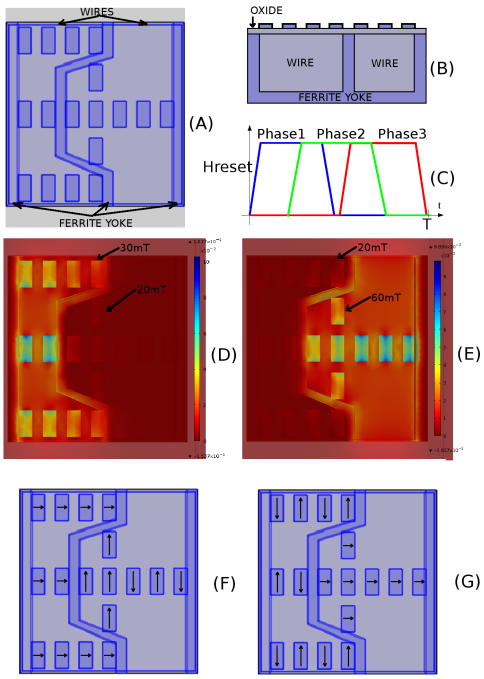


Fig. 9. Comsol Simulation of clock wires A) Clock wires model, upper view. B) Clock wires model, section view. C) Clock signals waveform. D) Simulation results with current flowing in the first clock wire. Color gradations represent the horizontal component of the magnetic flux density (B) expressed in Tesla. E) Simulation results with current flowing in the second clock wire. F) G) Magnetization schematic representation of Comsol simulations.

nets of the same sizes and with the same distances. Therefore the use of the classic majority voter with this clock system seems impossible. A possible solution is to use a AND/OR gate as presented in [21]. However this is an important limitation, because the use of the MV can greatly improve the set of logic gates available in the NML technology, allowing the design of more dense circuits. For this reason, here, we propose a different solution: a local modification of the clock wires that makes possible the fabrication and the proper operations of a MV. The structure is shown in figure 9.A. Clock wires are shaped (routed in a different plane clearly, see [14]) around the majority voter. In this way signals arrive at the gate inputs simultaneously. The darker lines which surround the wires represent a ferrite yoke used to confine magnetic flux lines and to reduce the current necessary for magnets switching as proposed in [22] (a section view is in figure 9.B).

Although this solution is not of easy implementation from the technological point of view, simulations obtained using Comsol Multiphysics [23] show that the structure assures a proper MV behavior. In Fig. 9.D the magnetic flux density is shown (top view) when the current flows through the left wire. The current values applied are such that the intensity of the magnetic field is kept at the minimum value necessary for magnets to switch. This is done to reduce clock power consumption. Magnets of the left clock zone should be forced in the RESET state, while magnets on the right clock zone are supposed to stay in the HOLD state (see figure 9.F). Considering the worst case measured in the simulation, the magnetic flux density is double on the magnets of the left clock zone with respect to magnets of the right clock zone. However, Fig. 9.D shows that on magnets of the left clock zone placed in the corner the magnetic flux density is low, and might be too low to assure the magnet reset. To assure magnets reset an higher current should be used. However, in this case also the (peripheral) magnets of the right clock zone might reset. But this is not a problem if a three overlapped phases clock regime is used as we proposed in [14] (figure 1.C). In this clocking system, magnetic field is first applied to the left clock zone. Afterwards, when the magnetic field is still applied to the left clock zone, the magnetic field is applied also to the right clock zone (magnetic field of the two phases are overlapped for a small time). As a consequence it is not a problem if the magnetic field of the left clock zone forces to the RESET state also some magnets of the right clock zone due to bad field confinement. In any case there will be a moment in which the magnetic field will be applied to both clock zones. After this moment, then, the magnetic field will be removed from the left clock zone but still it will be applied to the right clock zone [14]. In this moment it is important that the magnetic field of the right clock zone will not interfere with magnets of the left clock zone that are in the switching phase. But, again, this is granted as shown in figure 9.E, which shows the magnetic flux density when current flows through the right wire. Here, in the worst case the difference of the magnetic flux density of the left magnets and of the right magnets is quite high. This means that magnets of the left clock zone will not be forced to reset when the magnetic field is applied to the right zone. Therefore this modification

of clock wires, although not easy to implement, assures the possibility to fabricate properly working MVs, increasing then the set of gates available and the density for NML technology.

VIII. Conclusions

Our contribution notably improves the practical knowledge on NML especially considering to the impact that technological implementation has on NML circuits. We showed that it is possible to obtain correctly working circuits if specific constraints are respected: i) with gaps of 40-50 nm between nanomagnets the logic gate considered behaves correctly, thus deep UV lithography becomes the preferred fabrication technique; ii) magnets aspect ratio not far from 2 is the best solution for behavior and performance; iii) small magnets sizes assure a better rejection to process variations; iv) timing and energy consumptions are precisely related to magnets distances, sizes and input configurations, and values for a correct optimization are given; v) Majority Voter realistic implementation might require to satisfy considerably impractical constraints, that our proposed solution based on an alternative clock distribution technique can successfully overcome.

We are working on the experimental validation of these results with focus on the analysis of the clock system, both from the simulation and the experimental point of view, as we believe the clock system being the real obstacle to a realistic implementation of this technology.

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