TAMTAMS: a flexible and open tool for UDSM process-to-system design space exploration

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***Abstract*—Ultra Deep Sub-Micron (UDSM) processes, as well as beyond CMOS technology choices, influence circuits performance with a chain of consequences through devices, circuits and systems that are difficult to predict. Nonetheless effective design-space exploration enables process optimization and early design organization. We introduce TAMTAMS, a tool based on an open, flexible and simple structure, which allows to predict system level features starting from technology variables. It is modular and based on a clear dependency tree of modules, each related to a model presented in literature of specific quantities (e.g. device currents, circuit delay, interconnects noise, ...). Models can be compared and sensitivity to parameters observed. We believe our contribution gives a fresh point of view on process-to-system predictors. Though still partially in development, it already shows flexibility and allows a traceable path of a technology parameter on its way to the system level.**

I. Introduction and motivation

It is well understood that the consequences of technological choices in advanced CMOS processes are to be evaluated at the system level. Here, complex interaction mechanisms among the different parameters require a detailed analysis. Scaling trends in CMOS technology have been and are tackled by different points of view in several specific research contributions. A few examples are [1]-[4], where device and/or system level parameters are analyzed and modelled under the light of scaled technology processes and possible choices. Effective predictors were proposed in these and other works to help technologists to understand the effects of their decisions on the electrical parameters of basic devices. However, currently it is not completely possible to clearly identify how these effects will influence the system performance as clock frequency, power consumption, design robustness and so on. Designers generally struggle with these problems during advanced phases of the design flow with two main drawbacks: i) the system level effects of technological choices can be used to optimize processes too late increasing the costs in the development of new technology nodes; ii) the skills in terms of system level predictions are only partially shared between technologists and designers, making more difficult the definition of common objectives.

A comprehensive point of view on these aspects inspires the International Technology Roadmap for Semiconductors (ITRS) [5], which gathers up-to-date trends and information from technologists and circuits designers and provides an overview of what to be expected for the future. From a practical point of view only a few are the contributions which allow to analyze devices and circuits features and trends. At the device level MASTAR [6] gives detailed device level information (transitor currents, timing, etc..) for an exhaustive and up-to-date set of technology families and processes. At the system level, BACPAC [7] (and more extensively GTX [8], based also on other specific tools similar to BACPAC), enables system level performance exploration considering ITRS technology data. These tools can only be used separately, and are partially open. However, the combination of the two still does not represent what needed for a process-to-system design exploration in the light of current and future technologies. In fact, the predictions on system level performance starting from the description of technological parameters, requires perfect transparency at each level to avoid that the final results give information not readable for the designer in terms of technology-system effects. The definition of a tree of dependencies is essential. This means that, for each predicted electrical quantity, the model adopted must be shown, as well as possible dependencies from other evaluated parameters should be underlined, in order to make the results completely traceable. In the same way it is important that at the system level the electrical parameters used to predict performance assume clear definition about the design as complexity, design style, constraints.... The results accuracy in predictors with these characteristics is not always satisfactory, if compared with detailed data obtained by back-end simulations. Nonetheless, as a counterpart, a large amount of information can be obtained when parametric analysis are performed by varying: a) the target technology (for instance for the same technology family the different nodes can be used to understand the effect of scaling); b) some specific parameters in the same technology node (for instance gate oxide, doping levels...) c) some operating conditions (for instance temperature, supply voltage...) d) different models for the evaluation of a specific electrical or system quantities (models proposed in literature can be compared).

At present time then, the evolution in technology, the advances and variety of device models, the increased need to link technology to device and to system, as well as the arising demand to compare next generation CMOS devices

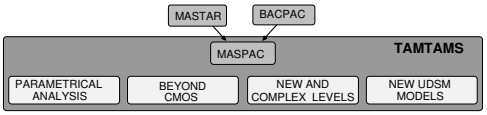

Fig. 1. TAMTAMS general features.

to emerging beyond CMOS structures are among the motivations behind our contribution. Inspiring to MASTAR and BACPAC (partially to GTX), but with a fresh approach and holding to the above mentioned requisites, we propose TAMTAMS: "Torino Assessment of Mos Technology and Advanced perforMance of System calculator", which general features are summarized in figure 1 and overviewed in section II, while in section III some sample results are shown to give an idea of possible capabilities. No details are given on the implemented models as out of the focus of this paper.

II. TAMTAMS Organization

TAMTAMS characteristics are synthetically outlined in the following, referring to figure 1.

- A complete bottom-up link from process to device and from device to system was freshly set up, in order to consider the impact of a device level parameter or technology process parameter on system level performance (MASPAC was the first stage of development, as a merge between MASTAR and BACPAC in the figure).
- New levels were added between device itself (focus of MASTAR) and system (focus of BACPAC), as gate/circuit/memories, or detailed interconnect system level.
- New and up-to-date models were added at all levels considering the most innovative contributions from literature as well as models we ourselves proposed; the aim is not only to adapt models to current UDSM technology trends, but also to allow a critical comparison among different modeling features.
- Every figure of merit and/or predictor is reachable for inspection.
- Parametrical (sensitivity) analysis is possible and can be added to any available feature.
- Models for alternative structures can be (and have partially been) inserted, for example FinFETs or Gate-All-Around FETs, or even beyond CMOS devices. This flexibility is essential in the current context where technology evolution has variety as first direction.
- TAMTAMS is based on a set of modular and flexible OCTAVE [9] scripts, that are then totally open and can be easily modified.

TAMTAMS is partially in development, but already supports all the abovementioned features. We believe that

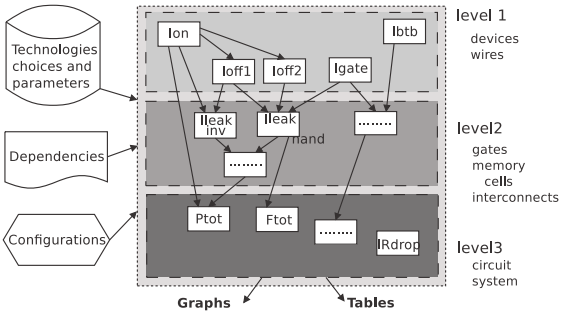

Fig. 2. TAMTAMS general organization. Several modules (here just a few examples) are organized in three levels. Each module represents a different model or set of models for a specific structure. Modules can be independent or rely on other modules. Specific files are available to choose the correct technology parameters. A list of dependencies among modules allows to compare the effect of a model on system level. The output can be graphical or numerical.

it can be used i) by the system and circuit designer to explore the design solution space, ii) by the technologist to rapidly have a hint on the effect of process choices, iii) by the model expert (at all levels) that can immediately compare his/her model to others already proposed, iv) from students/teachers that can have/give a tangible idea of ultimate microelectronics trends, issues and models.

The structure of TAMTAMS is sketched in figure 2. It is organized in a set of modules (each based on a OCTAVE script) and in a few support files. Modules can be referred to as LEVEL1 for device level, LEVEL2 for intermediate gates and small circuits level, and finally LEVEL3 for system data. Each module calculates specific figures of merit using a model chosen from the literature. New models can be then easily added using simple compatibility rules. Modules are hierarchically organized, as evaluation of certain data requires previous calculation of other modules (i.e. certain models of transistor I_{off} current are calculated starting from the value of I_{on} current). A special dependency system is implemented to handle this parameter interdependency. When a particular module is selected this system checks if others modules are required and indicates which modules must be loaded. Moreover, for each module the system checks if two or more models are available and lets the user select which model is to

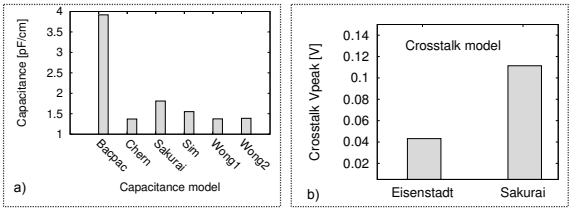

Fig. 3. TAMTAMS output: a) (LEVEL1) comparison among different models of a wire capacitance implemented in separate TAMTAMS modules. b) (LEVEL2): peak of voltage due to crosstalk according to two models proposed in literature ([11] and [10]).

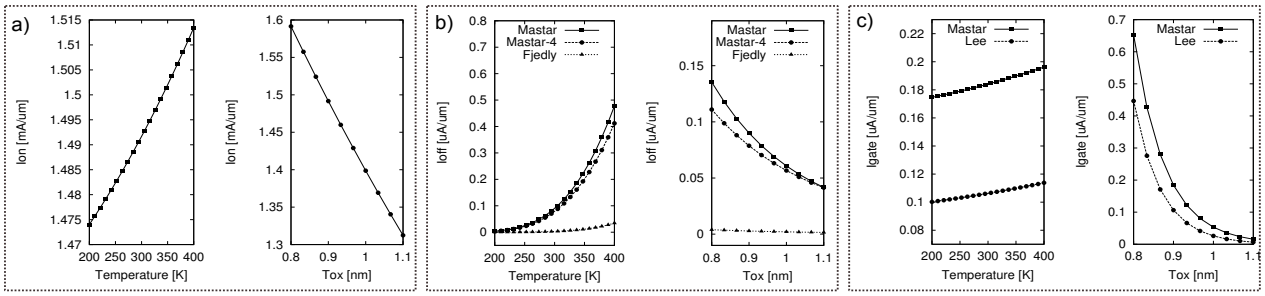

Fig. 4. TAMTAMS output (LEVEL1): a) I_{on} current according to original MASTAR model. b) I_{off} current according to original MASTAR model, to a modified model also present in a new MASTAR version and to another model proposed in literature (Fjedly [12], [13]). c) I_{gate} current according to original MASTAR model and to another model proposed in literature (Lee [14]). In the three cases the analysis is parametric: left of each graph: current as a function of temperature; right, current as a function of a variation on gate oxide thickness.

be used. A predefined automatic dependency list can be used as well (dependency support file). with parametric analysis. Clearly, then, this structure allows high flexibility and virtually infinite possibility of extension.

Other external inputs are technology files describing the physical parameters of each technology process.

Results are shown by means of graphs or tables. Many modules can be evaluated on the same graph or table to allow an easy comparison also as a function of technology nodes. Moreover, each module can be evaluated considering the variation of a specific technological or physical parameter. The tool is structured to allow an easy expansion of this parametric analysis, and any desired parameter can be added to the analysis.

Finally the tool allows also the analysis of circuit and/or system features that, for their nature, not necessarily depend on other modules.

III. SAMPLE RESULTS

In order to give some example of TAMTAMS characteristics we show here some cases of outputs at the three levels, both with and without hierarchical dependency. No details are given on the specific models, for space reasons and because out of the focus of this paper. All results shown here are obtained for a 65nm technology. All the other nodes normally available from ITRS are implemented and here not shown as identical to what is possible to obtain using MASTAR or GTX.

Figure 3 is related to interconnects models. It shows a comparison a) among six different models of wire capacitance for what concerns LEVEL1 and b) between two different models which estimate the peak of crosstalk (LEVEL2) between two lines with same characteristics.

In figure 4 device level currents are shown: a) I_{on}, b) I_{off}, c) I_{gate}. In all the cases a parametric analysis is performed with two different kind of parameters: temperature, as an example of environment condition, and gate oxide thickness as an example of process parameter. In graphs b) and c) a comparison is offered among different models chosen from the literature.

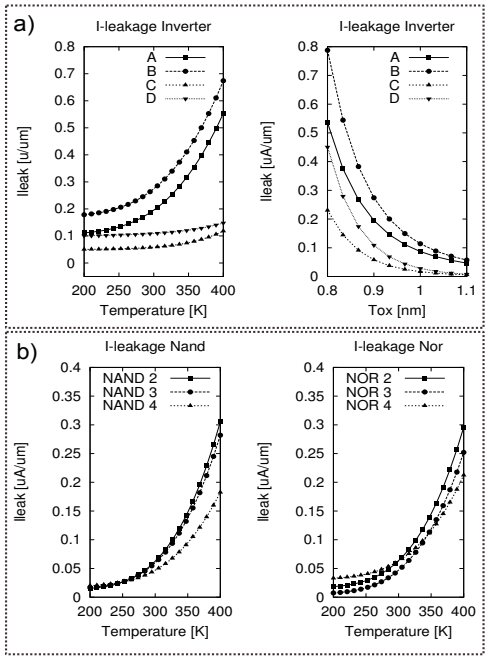

Fig. 5. TAMTAMS output (LEVEL2): **a)** leakage current of an inverter according to four of device currents models adopted: A) Igate-Mastar and Ioff-Mastar (no Ibtb); B) = Igate-Mastar, Ioff-Mastar, Ibtb-Roy ([15]); C) Igate-Lee, Ioff-Fjeldly; D) Igate-Lee, Ioff-Fjeldly, Ibtb-Roy. **b)** leakage current of a NAND gate (left) and a NOR gate (right) according to original MASTAR models of device currents. Different curves represent different number of inputs for each gate. In both cases: parametric analysis. Examples: left, current as a function of temperature; right, current as a function of a variation on gate oxide thickness.

Figure 5 deals with a case of LEVEL2 modules related to gate leakage current. Leakage depends at least on I_{off} and I_{gate}, and in some models, also I_{btb} is taken into account. In figure 5.a) four combinations of current models are considered, again using a parametric analysis, and their impact on a gate leakage evaluation is well evidenced by different behaviors. For figure 5.b) one of these combination were used in order to evaluate the leakage current for a NAND (left) and for a NOR (right) gate with increasing inputs.

Figure 6 shows a comparison among system level

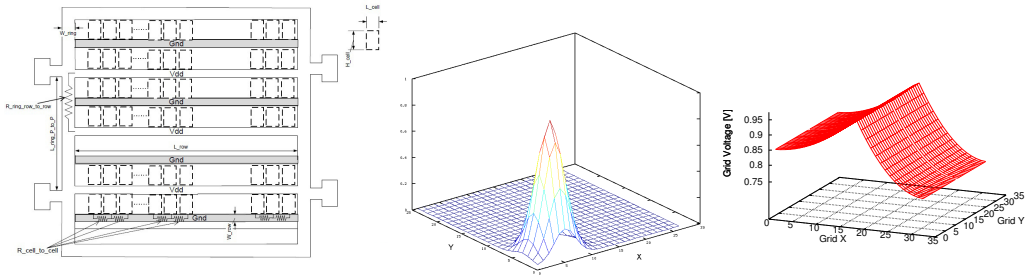

Fig. 7. Example of a new model introduced at LEVEL3 to estimate IRdrop as a function of a possible power grid structure and a current distribution [17]. Left: example of power grid defined by the user. Center: example of current distribution along the chip. Right: an example of voltage drop due to a current linearly increasing from one side to the other of the chip, and a power grid distributed like in left figure with a stripe added in the center.

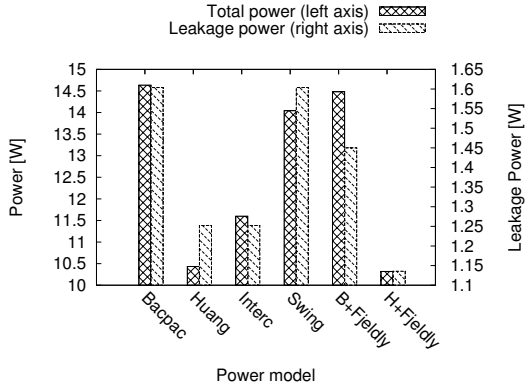

Fig. 6. TAMTAMS output (LEVEL3): total power (left Y axis) and total leakage power (right Y axis). Comparison among different models. *Bacpac* is the original model present in BACPAC; *Huang* [16] and *Swing* are new models introduced at LEVEL3 which relies on same submodules as Bacpac; *Interc* is estimated considering new modules on interconnect features introduced at LEVEL2; *B+Fjedly* and *H+Fjedly* are the same *Bacpac* and *Huang* models that rely on the I_{off} LEVEL1 model (fig. 4).

(LEVEL3) total and leakage power consumption. A few of these models are related to a combination of other modules included in the hierarchy related to process choices, to device models, to interconnects models or to circuit level models. Independently on the model details, this result show how much important is to have transparency at all levels in order to capture the influence of a choice on the examined parameter.

A final LEVEL3 example is in figure 7 where a model for estimating IRdrop distribution as a function of power grid design choices and of current distribution is used, reported as an example of a module which is sensibly independent on the others.

IV. Conclusion

We presented TAMTAMS, an open tool for process-to-system analysis. Its flexibility and modularity allows the technologist to estimate the effects of choices at technology not only on devices, but on circuit and on system as well. Its transparency enables the system designer to handle the cause-to-effect concatenation of technology and design choices. Its versatility lets the model engineer to compare with same other conditions his/her model with the others already proposed in literature. As shown here through a few examples, several parametric analysis comparisons are already possible, even though the open scenario of current technology advances will require more work to have an exhaustive anc complete tool.

V. Acknoledgements

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