From the foundry to the model - A fully automated system for on-wafer MESFET characterization

FROM THE FOUNDRY TO THE MODEL

A fully automated system for on-wafer MESFET characterization

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Abstract

The fabrication of microwave integrated circuits requires several tests to be carried out on wafer in order to check the effectiveness of the process. That is accomplished by measuring some parameters of a small group of test devices named PCM (Process Control Monitor), located on the same wafer and fabricated with the same process.

In this paper a system is presented which integrates in a single workstation the experimental procedures, and the data processing which allow to carry out on line the more significant parameters of microwave GaAs FET. In order to achieve significant results in MMIC device modeling, a proper design of the PCM layout is required. This is accomplished by using special metallized patterns on GaAs, for the network analyzer calibration, which allow to define the reference planes very close to the active area of the device.

A software package drives the user through all the operations up to the development of a small signal MESFET model, so that the procedure overcomes the peculiarity of laboratory experiment and gains the characteristic of a more general and operative tool, useful for recurrent applications.

1 Introduction

One of the main problems in monolithic circuits manifacturing, especially when a "foundry" service is provided, is to set up and to warrant a stable fabrication process in order to improve both the repeteability of the device electrical characteristics and the customer's circuit performances and the yield. To assure a very effective process control, both DC and RF tests are performed on PCMs, located on each wafer, which contain, among the other devices, a mesa resistor, a Schottky diode and a MESFET. Measured data are then used to extract the main process parameters (i.e. the sheet resistance and the doping profile) and MESFET parameters (i.e. I_{dss}, g_m, pinch-off voltage, the ideality factors of gate-source and gate-drain Schottky diodes). The measurement accuracy and the time involved with the procedure, are the main parameters to be improved, because of the large amount of data required for a statistically significative characterization.

The final step of the procedure consists in the PCM MESFET measurement in order to extract a circuit model of the device. All the DC and RF measurements, required for this purpose, are carried out directly on wafer, with coplanar RF probes put into contact with pads built around the active device.

In order to de-embed the influence of such environment at RF, a TRL calibration procedure is followed, which makes use of some layouts properly designed and built on the same PCM, as reference standards.

Several software packages [1,2,3] are commercially available, by which the MESFET circuit model can be extracted from measurements. These ones, generally devoted to CAD applications, follow somewhat rigid procedures without the flexibility required when they deal with the research and development problems. In this case the tests should be rather carried out step by step, in order to give a good visibility of the parameter extraction process.

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This goal is pursued by our procedure, which leads in addition to extract several parameters by using different methods. In this case the parameter final values can be selected, on the basis of the experimental data dispersion and consistency, evaluating the fitness between the simulated and the actual device behaviour.

2 Test system description

The system, whose basic hardware consists on a HP8510 vector network analyzer, a HP9000 series 300 desktop computer and a microwave wafer probing station, has the block diagram represented in figure 1 and usually performs both DC and RF tests without removing the wafer from the set.

The computer controls the whole procedure, which includes calibrations, measurements and data processing, by means of modern interactive software technique, using icons, mouse driven menus and high graphic effectiveness.

Furthermore, to avoid the device selfheathing the DC source were impulsed to minimize the dissipated power, and both the pulse width as well as the duty cicle were adjusted in order to keep constant the dissipation while varying the pulse amplitude. It is important to note that a procedure for accurately calibrating the test set is performed before the DC measurement session; this allows to remove the effects of the wire and probe resistances, which can drammatically affect the results.

All the circuit configurations capable of measuring the characteristic of PCM devices, like mesa resistor and Schottky diode are implemented and follow customary procedures found in the literature [4,5,6]. The MESFET characteristics like the gate-source and gate-drain parameters (i.e. ideality factor, the barrier built-in voltage and the reverse saturation current of both the diodes), the pinch-off voltage, the active channel resistance and the DC trasconductance, are also measured by usual techniques [7,8,9,10,11,12,13].

The extrinsic reactive elements, bias independent, are extracted by RF measurements, with a proper bias or short circuits between the device terminals, [14,15] by means of "cold" FET S-parameter measurements [16,17] and so on.

These additional measurements reduce drastically the number of unknown parameters of the model, making it easier to determine the intrinsic part of the equivalent circuit [18].

The intrinsic parameters are evaluated by measuring the S parameters of the device, biased at the desired point, and following the procedure developed by Dambrine [14].

Since the parameter exctraction is performed at each frequency, an important program facility is the possibility to plot the values of the intrinsic model parameters versus frequency. The operation is carried out almost istantly and the curve flattness is a very good test to validate the effectiveness of the characterization and modeling process. The experimental results, reported in the next section, show variations of the parameter values in a range of a few percent over the frequency range between 4 to 18 GHz. This is very encuraging and is in support of the validity of the approach we followed.

Another program facility consists in the possibility of carrying out measurements while varying the device bias point, by independently setting numerous steps of gate-source and gate-drain bias values. Several circuit models can be consequently obtained, in which the bias dependendence of the MESFET parameters is inferable.

3 Definition of the input and output reference planes

In MMIC applications, FETs are generally used in a microstrip envirorment, while the measurements are carried out with coplanar probes.

The large time, the yield and the cost involved in the fabrication process, preclude the use of via-hole transitions between coplanar to microstrip line, but they suggest to built special coplanar patterns around the active device area, as shown in figure 2.

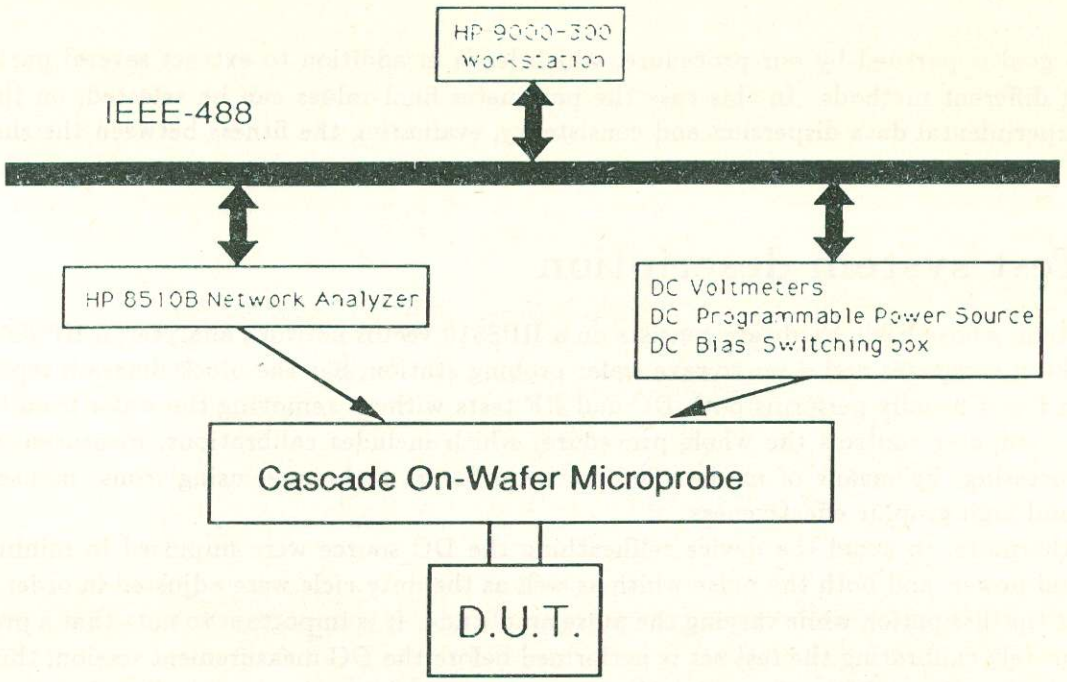


Figure 1: Measurement Test Set

With the ordinary calibration technique, which uses a 50 Ω load, a short, an open and a thru as standards, everything past the end of the probe tip is measured, including the open stub capacitance due to the gate and drain pads just before the probe tip contacts, and the part of coplanar line between the probe tip contact and the device edges.

Because these parasitics can heavily modify some equivalent circuit parameters, such us L_g, L_d, L_s, C_{ds}, C_{gs} [1], when the model validity shall be extended up to the higher frequencies, the measured S parameters shall be de-embedded from such elements.

That is accomplished by a TRL (thru-reflection-line) technique, which became the ordinary technique to correct the errors introduced by the network analyzer measurement system in a fixture environment.

The standard elements, required for this approach, are a thru connection, a transmission line, whose characteristic impedance defines the reference impedance of the measurements, and two equal offset shorts; they are properly designed and fully integrated on the same PCM, as shown in figure 3, to match our MESFET layout, so that the reference planes can be located at the device edges.

To obtain maximum of repeatibility, a reference metal bars were evaporated to mark where the front of the probe tips should land.

Since the 50 Ω line on GaAs, has the spacing between the ground and signal line inconsistent with the gate width beyond 300 μm, in order to extend the testing capability to wider FETs, another set of standard components was built with characteristic impedance of 61 Ω (with spacing between ground and signal line equal to 80 μm). In this case the system automatically computes the S parameters referred to the normal 50 Ω impedance.

Some experimental results which refer to a 600 μm MESFET are reported in figure 4 as an example of a particular characterization. The curves show the circuit model g_m and C_{gs} parameters as a function of the frequency. It can be noted that the variations are in the range of a few percent of each parameter value; this testifies the effectiveness of the circuit modeling and characterization technique.

4 Conclusion

A very flexible and fully automated procedure was developed and tested on several MESFET fabrication processes. The data necessary to check the various process steps are provided by quick and reliable procedures and, if required, more detailed information on the device can be obtained. The latter concerns reliable data of extrinsic and intrinsic device parameters up to a complete circuit model.

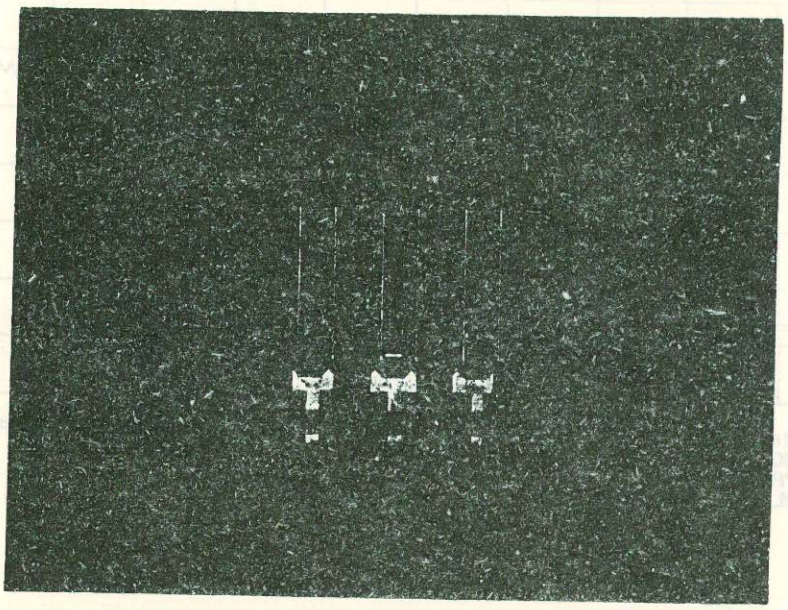


Figure 2: Layout of the MESFET pads

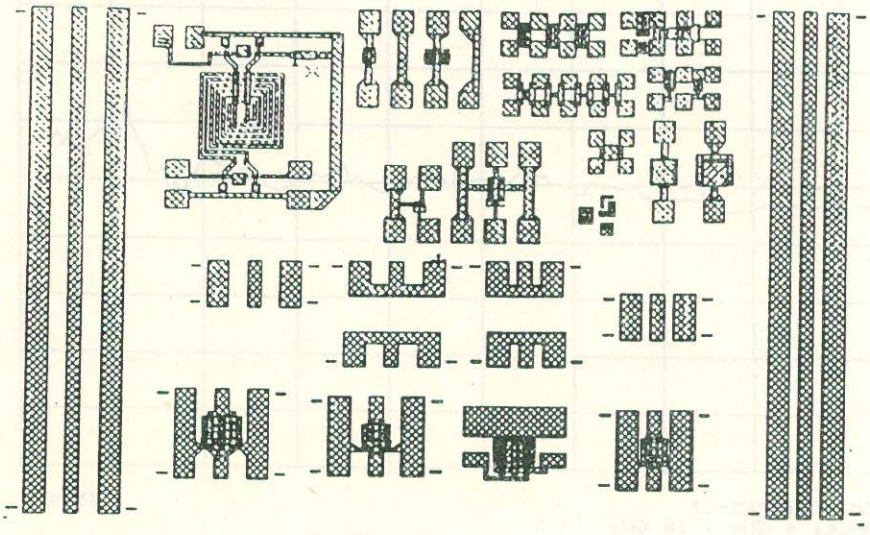
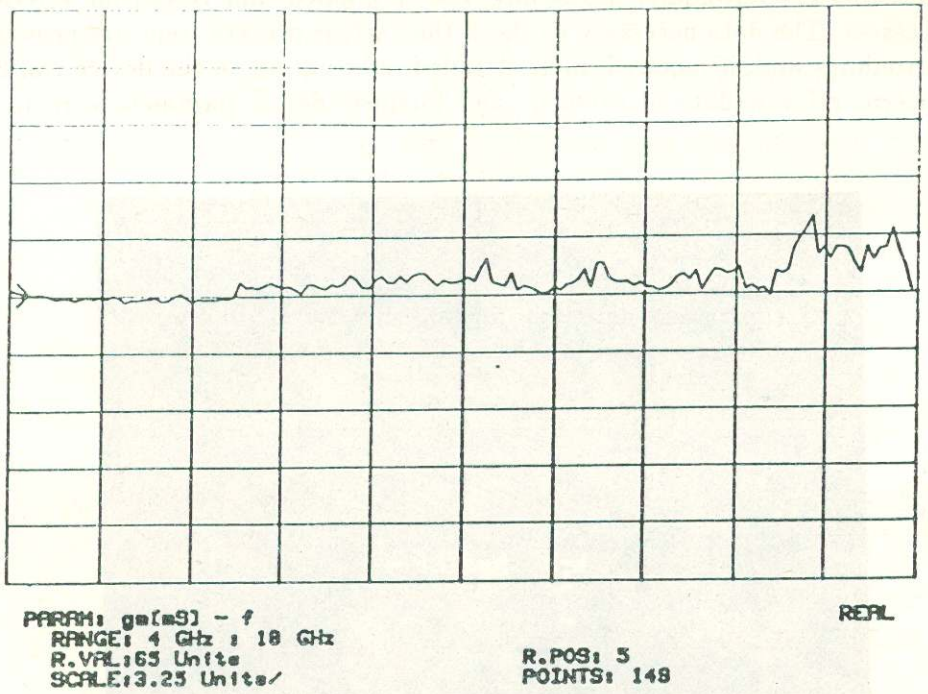


Figure 3: The PCM layout



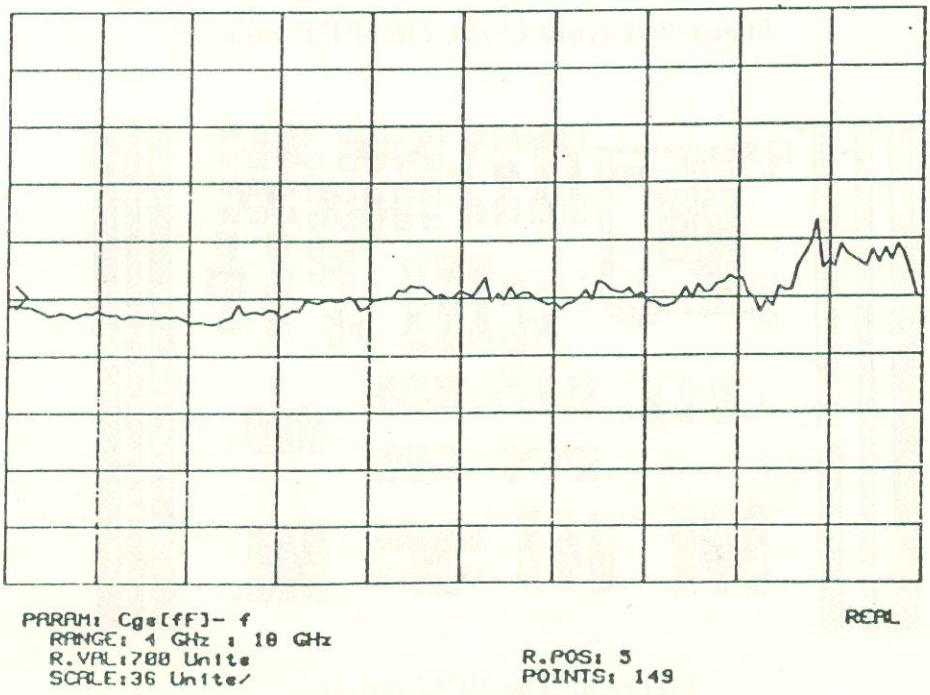


Figure 4: Some MESFET intrinsic parameters as a function of frequency

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