TIME DOMAIN REFLECTOMETRY APPLIED TO MMIC PASSIVE COMPONENT MODELING

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Abstract

The time domain facilities of a network analyzer, combined with the tools of network synthesis, were recently used for experimental modeling of discontinuities in an S-parameter measurement set, so as to allow the instrument calibration directly to the ports of the device under test.

The technique proved to be very useful in those cases where the discontinuities, that lie before the unknown device, cannot be isolated by the usual calibration methods, and therefore, since network synthesis deals only with frequency domain information, it is impossible to optimize the model's parameters, since they are affected by errors due to discontinuities.

This paper describes a procedure which allows to isolate the response of the device under test, and to derive its complete model; when it fails to reach a reasonable accuracy it gives anyway a topology, which is a good starting point for other optimization routines that can be used for obtaining a better match on a broad frequency band.

This can be accomplished by optimizing the first approach topology to which other circuit elements have been added, so as to take into account second order effects especially at the higher frequencies.

The technique was applied to model and characterize passive discrete components used in MMIC.

The experimental results show the validity of the approach.

Introduction

Several recent works were oriented to the application of the "synthetic pulse reflectometry" in the recognition of transmission lines discontinuities, with the purpose of de-embedding their effects while measuring the scattering parameters of a device [1,2,3].

Recently we proposed a technique [4,5,6] which, by using the time domain capabilities of a network analyzer and the tools of network synthesis, allowed to thoroughly characterize a passive device, such as a microstrip transistor fixture, by modeling and de-embedding the coaxial-microstrip launchers.

Following the already described technique, we developed an user oriented software package, which runs on an *hp9000-300* series computer, connected with a measuring system (*hp8510B*) in order to realize an integrated workstation for device characterization purposes. A Microtech Cascade wafer probe extends the work station capabilities to MMIC device modeling.

In this paper we present some examples of application of the software package to the characterization of MMIC components. After testing several devices, we could improve the procedure in some aspects, so as to get an effective algorithm irrespective of the model complexity.

In order to prove the effectiveness of the approach, we report some experimental results in which a good accuracy of the model is achieved also when tests are intentionally carried out on imperfect devices, whose models correspond to more complex topologies.

Procedure description

In order to model an unknown one-port passive device embedded in a passive network, the analysis is carried out by examining the time domain impulse response at the input port of the device under test, obtained by processing frequency domain data of the input reflectance.

By using the gating facilities of the ANA, the first echo can be isolated and an equivalent network can be synthesized, which matches its frequency response. A matrix product de-embedding procedure is used in order to remove the effects of the first discontinuity from the experimental response of the original network. The procedure can be repeated on the following echoes of the time domain response, so as to identify and model the other discontinuities, [3,4,5,6], and to remove their echoes from the time domain response, as shown in fig.1.

Obviously, if the first step of TDR analysis does not show spurious echoes before the one produced by the DUT, we can bypass the de–embedding procedure and directly use the synthesis tools to extract the device model.

It must be pointed out that the synthesis procedure is based on the Darlington theorem, by which a generic passive one–port may be synthesized as a resistance loaded reactive two–port.

We apply this theorem for synthesizing the equivalent circuit corresponding to the gated echo, and we use the reactive part of the synthesized circuit for modeling the discontinuity to be removed. For simplicity the synthesis procedure takes into account only first and second order lumped circuits plus a cascaded line, which is needed for matching the phase response.

The last echo, after all the discontinuities have been de–embedded, is produced by the unknown device, and it must be considered as the response of a one port component. The frequency domain transformation of this echo represents the reflection coefficient of the unknown device to be modeled.

In several cases, due to the complexity of the response, the second order network is not sufficient for a good approximation on a broad frequency band; furthermore the Darlington theorem produces only lossless topologies.

In order to overcome these drawbacks, the network synthesis procedure was modified so as to allow the user to insert other components into the model obtained in the first step. A simulation routine combined with an optimization one allows to adjust the component values of the model in order to obtain a better fit of the frequency response of the device under test over the whole frequency band. Since the first step model is already a good one, the optimization routine works only on a limited number of element parameters, and converges very quickly.

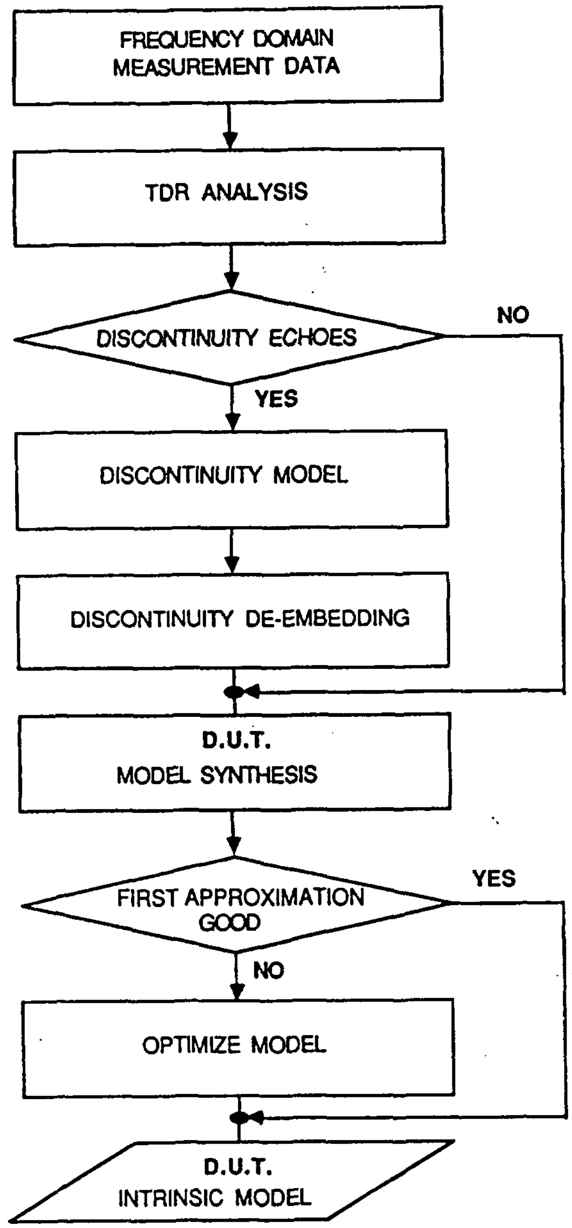


Figure 1: Flow diagram of the procedure

Experimental results

The described technique was successfully applied to the experimental characterization of some MMIC components in which interface problems between the coaxial cable instrumentation, RF probes and chip can arise. The tests were carried out by means of coplanar rf probes calibrated on wafer. Figure 3 shows the time domain reflectance of the Schottky diode capacitance of fig.2, seen at port 1 when port 2 is loaded on a 50 Ω resistance.

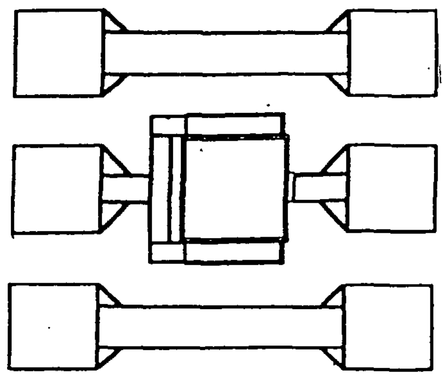


Figure 2: Schottky diode layout

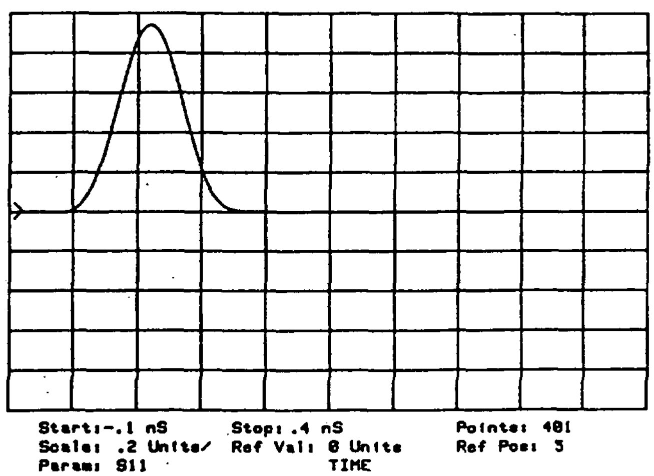
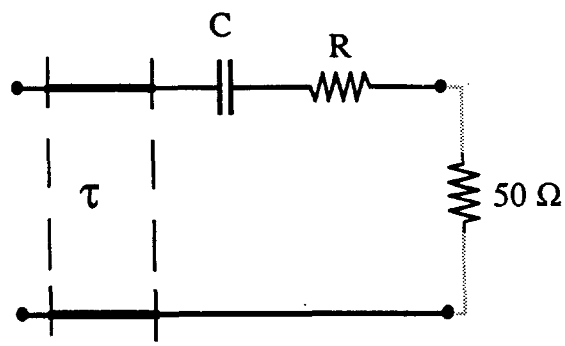


Figure 3: Time domain response

Since non relevant echoes appear before that related with the device to be modeled, the de-embedding procedure is obviously overcome, and the synthesis algorithm yields directly the model of figure 4. The comparison between the actual and the modeled reflection coefficient shown in figure 5 exhibits differences smaller than ± 0.05 dB and $\pm 0.8°$ on a 45 MHz $\div$ 18 GHz frequency band.



Bias voltage V	C pF	R Ω	τ ps
3	0.1191	35.6	1.806
5	0.0947	39.9	1.792

Figure 4: Reverse biased Schottky diode model

The line, that appears in the model, well matches the effects of the length of strip line between the probes and the capacitor. Note that this length doesn't change if we repeat the Schottky diode characterization with a different bias voltage, while the capacitor and the series resistance values change according with the physical behaviour.

A spiral inductor, with a layout studied specifically for a better interface between the GND-SGN-GND coplanar probes, as shown in figure 6, was

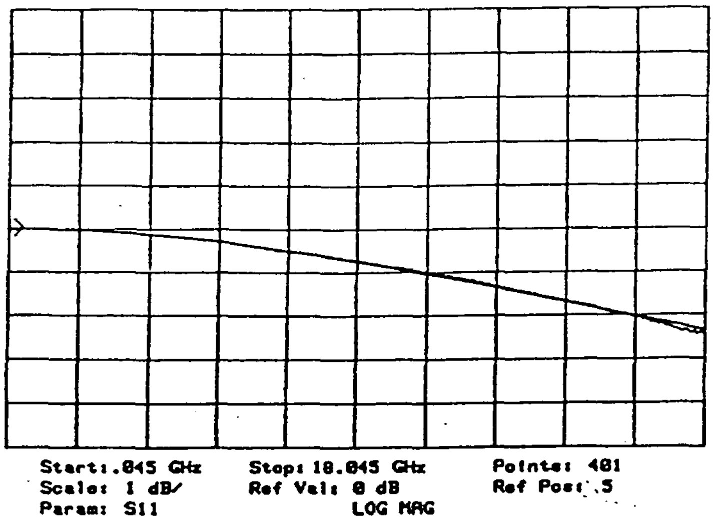


Figure 5: Simulated and actual Schottky diode reflection coefficient

also tested. Figure 7 shows the equivalent circuit of the inductance, and its frequency response compared with the measured one. While performing routine measurement on some spiral inductors on a broader frequency band (up to 26 GHz), we stepped onto a defective one, whose second order model did not fit the frequency response. So we had an opportunity to test our procedure on a more complex device by adding some circuit components, and by optimizing their values, as shown in figure 8; figure 9 shows the reflection coefficient of this device compared with that of the synthesized circuit.

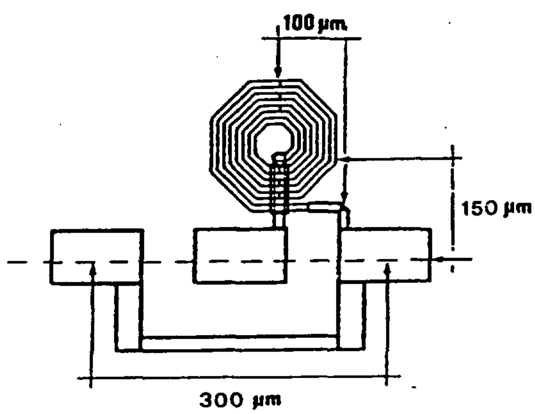
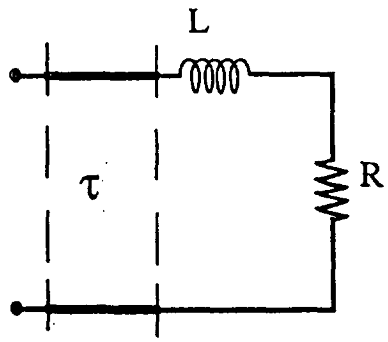
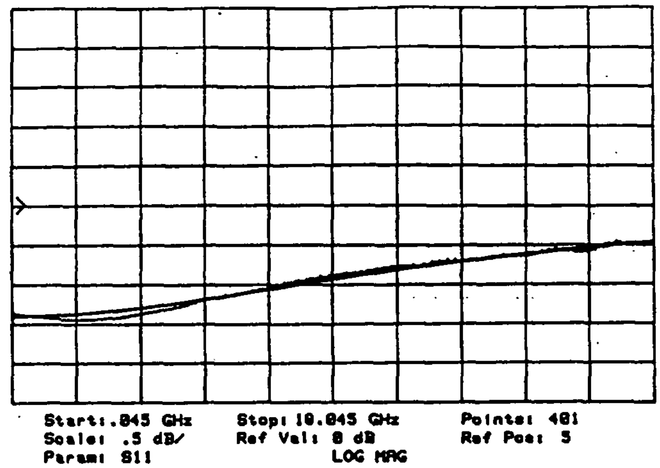
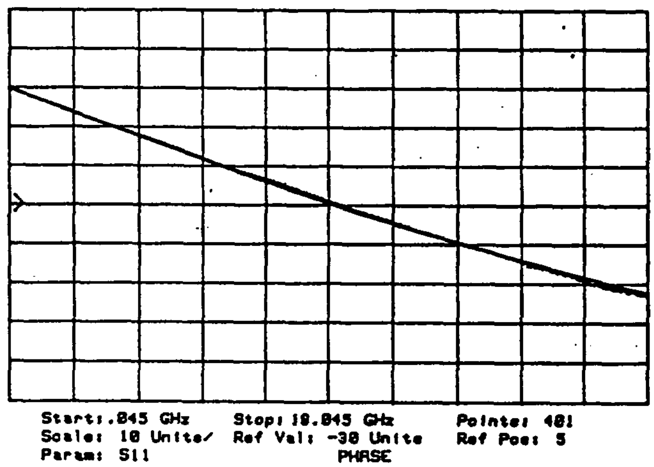


Figure 6: Inductor layout

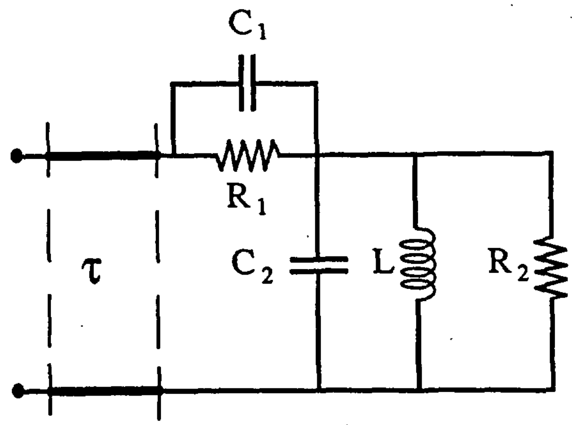






L	R	τ
nH	Ω	ps
0.6276	4.06	4.255

Figure 7: Inductor model and frequency response



L	C_1	C_2	R_1	R_2	τ
nH	pF	fF	Ω	Ω	ps
1.149	30.1	98.7	4.1	20.56	6.77

Figure 8: Faulty inductor model

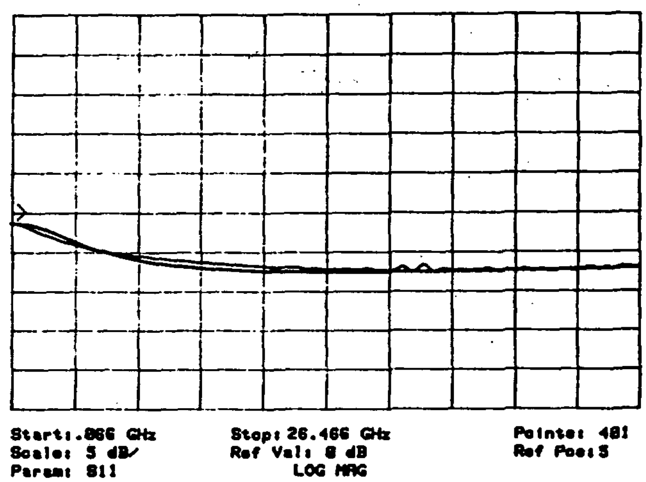


Figure 9: Faulty inductor actual and simulated reflection coefficient

Conclusion

A synthesis procedure based on time domain reflectometry data has been presented that allows to generate circuit models of both fixture discontinuities and devices under test. The experimental results are very good and prove the procedure reliability.

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