Accurate large-signal equivalent circuit of surface channel diamond FETs based on the Chalmers model

Highlights

- Circuit-oriented model of surface-channel diamond FETs presented for the first time;
- Nonlinear equivalent circuit based on the III-V HEMTs Chalmers approach;
- Model validated under power operation against RF power measurements;
- Application to polycrystalline and single-crystal diamond FET technologies described.

Accurate large-signal equivalent circuit of surface channel diamond FETs based on the Chalmers model

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Abstract

The paper presents a large-signal nonlinear circuit-oriented model for poly-crystalline and single-crystal H-terminated diamond MESFETs implemented within the Agilent ADS design suite. The DC characteristics of such devices suggest that the channel free charge control law may be modeled using the same strategy adopted for III-V HEMTs. For this reason, the well-known nonlinear Chalmers (Angelov) circuit model was chosen as the starting point for the development of the present non-linear diamond MESFET model. Model fitting was performed against DC and multibias small signal measurements, with good agreement. Model validations versus large-signal (power) measurements point out the accuracy of the proposed approach to simulate the behavior of H-terminated diamond MESFETs under large-signal operation.

Keywords: Diamond, Hydrogen termination, Field Effect Transistor

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(FET), RF power, Large-signal equivalent circuit

1. Introduction

As well known, diamond has in principle outstanding semiconductor properties (such as high carrier mobility, high breakdown field, and record thermal conductivity) that can be profitably used for the development of power radio-frequency (RF) and microwave FETs [1]. Although diamond devices were first demonstrated almost twenty years ago [2], only during the last few years, advances in growth techniques both for single-crystal and polycrystalline diamond substrates (see [3] for a review), have led to devices able to exhibit reproducible RF behavior and power characteristics [4]-[8]. Of the two approaches currently pursued to achieve charge control, namely extrinsic acceptor doping with boron [9], and hydrogen (H) surface termination [10], results from the literature seem to point out that H-terminated surface-channel MISFETs [11] and MESFETs [4]-[8] have demonstrated superior performances in terms of cutoff frequency (e.g. 45 GHz for 0.1 μm gate length polycrystalline H-terminated MESFETs, [6]). For this reason, the rest of the work will focus on H-terminated MESFET technology.

Despite stability problems that still have to be overcome from a technological standpoint, the current availability of large-signal characterizations [5], also carried out by the present authors [8], suggest that the diamond technology may be close to the stage where devices can be exploited in the design of power circuits (typically power amplifiers or oscillators). To this aim, a large-signal, circuit-oriented model for the nonlinear simulation of diamond devices is needed, and, to be effectively exploited in the circuit design

phase, it has to be implemented within a CAD commercial simulator. In this work we present, for the first time, a circuit-based nonlinear model of surface channel diamond FETs based on the Chalmers model approach [12], and embedded within the ADS Agilent CAD tool.

The use of the Chalmers approach (first proposed for the modeling of High Electron Mobility Transistors, HEMTs, on III-V semiconductors), rather than of other available circuit-oriented models, was suggested by a possible analogy between the behavior of H-terminated diamond MESFETs and III-V HEMT. In HEMTs, the free charge density of a two-dimensional carrier (typically electron) gas induced in a quantum well by modulation doping [13], is controlled by a Schottky contact through a non-conducting interface layer, and the charge control law exhibits a typical saturation behavior for large values of the controlling voltage. Although in H-terminated diamond devices the composition of the very thin interface layer and the physical mechanism inducing the quantized hole channel are still controversial, the electrical behavior of such devices shows features (such as the current saturation with gate voltage), which are consistent with the specific *tanh*-like shape of the charge control law on which the Chalmers circuit model is based. The results shown in the present paper clearly suggest that, at least at an empirical level, the Chalmers approach indeed seems to be an excellent candidate for the large-signal simulation of H-terminated diamond MESFETs.

2. Experimental

The devices characterized and modeled in the present paper are H-terminated MESFETs grown on large grain size polycrystalline diamond sub-

strates supplied by Element Six. The devices are fabricated with the process described in [7, 8]. They exploit a coplanar two-finger layout with I-shaped gate electrodes with 200 nm and 50 μm gate length and width respectively, and are printed by a single-layer electron beam lithography process. Two sets of device were fabricated, referred in the following as first and second generation. In the latter, source and drain pad thickening was carried out to improve the electrical contact with the RF measurement probe tips, and to overcome probe scratching issues observed in the first generation devices. The fabricated devices were characterized under DC, small-signal at different bias points, and large-signal conditions using the active load-pull bench described in [8].

3. Model theory

The Chalmers (Angelov) microwave FET large-signal model (first presented in [12, 14]) is a widely exploited general-purpose circuit-oriented model. Contrarily to other, previously proposed JFET, MESFET or MOSFET large-signal models, the Chalmers model incorporates features that make it particularly well suited to simulating III-V High Electron Mobility Transistors (HEMTs). In particular, the DC trancharacteristics are approximated by a hyperbolic tangent function of the gate to source voltage V_{GS}, in agreement with the physics-based channel free charge control model exhibiting a linear region and then saturation, suggested for AlGaAs/GaAs HEMTs by Roblin et al. [15]. The surface-hydrogenated polycrystalline diamond MESFETs initially considered in this research (see [8]) showed measured DC output characteristics in which the drain current is almost independent from V_{GS} in

the linear region (see Fig.[5] in [8] and Fig. 2 in the present paper). This can be related to the saturation of the channel hole mobile charge for large V_{GS} absolute values. Although the detailed physical mechanism of the charge control in surface-hydrogenated diamond MESFETs is still object of discussion (see [16]-[18]), the, at least extrinsic, similarity between the charge control in diamond MESFETs and III-V HEMTs, suggests to apply the Chalmers approach to diamond devices, with encouraging results not only concerning the devices considered initially [8], but also other devices from literature [5].

The implemented model (see Fig. 1 for the circuit scheme) exploits an analytical expression of the intrinsic drain current as a function of the gate to source and drain to source voltages, V_{GS} and V_{DS} respectively [12]:

$$I_{\mathrm{DS}} = I_{\mathrm{pk}} \left(1 + \tanh(\Psi)\right) \tanh(\alpha V_{\mathrm{DS}})(1 + \lambda V_{\mathrm{DS}}) \tag{1}$$

where I_{pk} is the drain current at which the maximum transconductance g_{mpk} occurs, and the function Ψ is a power series centered at V_{pk} (the gate voltage corresponding to g_{mpk}):

$$\Psi = P_1(V_{\mathrm{GS}} - V_{\mathrm{pk}}) + P_2(V_{\mathrm{GS}} - V_{\mathrm{pk}})^2 + P_3(V_{\mathrm{GS}} - V_{\mathrm{pk}})^3 ... \tag{2}$$

The hyperbolic tangent term $\tanh(\alpha V_{\mathrm{DS}})$ in eq. 1 accounts for the drain current saturation as a function V_{DS}, being α the parameter that controls the sharpness of the transition from the linear to the saturation region, while factor $(1 + \lambda V_{\mathrm{DS}})$ models the non zero output conductance in the saturation region.

Similar analytic functions are adopted for the non-linear bias-dependent

capacitances $C_{\rm GS}$ and $C_{\rm GD}$:

$$C_{\rm GS} = C_{\rm GS0}\left(1+\tanh(\Psi_1)\right)\left(1+\tanh(\Psi_2)\right) \tag{3}$$

$$C_{\rm GD} = C_{\rm GD0}\left(1+\tanh(\Psi_3)\right)\left(1+\tanh(\Psi_4)\right) \tag{4}$$

where

$$\Psi_1 = P_{0\rm gsg} + P_{1\rm gsg}V_{\rm GS} + P_{2\rm gsg}V_{\rm GS}^2 + P_{3\rm gsg}V_{\rm GS}^3 + ... \tag{5}$$

$$\Psi_2 = P_{0\rm gsd} + P_{1\rm gsd}V_{\rm DS} + P_{2\rm gsd}V_{\rm DS}^2 + P_{3\rm gsd}V_{\rm DS}^3 + ... \tag{6}$$

$$\Psi_3 = P_{0\rm gdg} + P_{1\rm gdg}V_{\rm GS} + P_{2\rm gdg}V_{\rm GS}^2 + P_{3\rm gdg}V_{\rm GS}^3 + ... \tag{7}$$

$$\Psi_4 = P_{0\rm gdd} + (P_{1\rm gdd} + P_{1\rm cc}V_{\rm GS})V_{\rm DS} + P_{2\rm gdd}V_{\rm DS}^2 + P_{3\rm gdd}V_{\rm DS}^3 + ... \tag{8}$$

The model has been implemented within the Agilent ADS CAD suite, which has been exploited in all simulations shown [19]. Additional details on the model implementation (that is slightly different from the one proposed in the original Angelov papers [12, 14]) can be found for example in [19].

4. Results and Discussion

4.1. Model extraction from DC and small-signal multibias measurements

The extraction of the model is carried out on the basis of DC and scattering multibias measurements according to the following steps: first, parasitics elements (drain, source and gate parasitic inductances and resistances) are extracted from cold FET measurements; then, the static DC characteristics are fitted by optimizing the parameters of the static intrinsic model; finally, the dynamic part of the model (gate-source, gate-drain and drain-source capacitances) is extracted from S-parameters data measured in different bias conditions (multibias S-parameters), and at several frequencies.

To test the model strategy to different diamond-based devices, the extraction approach has been applied to the first and second device generations, on polycrystalline diamond and, as a further test, also to a single crystal device taken from the literature [5]. In this latter case, due to lack of detailed information on the small-signal behavior, and on the adopted large-signal load termination, the model validation has been limited to DC behavior.

Typical measured and simulated DC output and trans-characteristics are compared in Fig. 2 for the first device generation, showing a good agreement. The crowding of the output characteristics in the linear region (-4 V $< V_{\mathrm{DS}} <$ 0 V) corresponds to a reduced V_{GS} control on the drain current, as highlighted from the transcharacteristic plot, consistently with the previously discussed 2D hole gas concentration saturation well approximated by the *tanh*-like charge control model. A similar behavior has been observed also for the 2nd generation devices, as shown in Fig. 3. This second set of devices showed slightly inferior performance, with respect to the first generation one, that can be attributed to the technological process variability. Finally, Fig. 4 presents a comparison between the measured and simulated DC output characteristics and transcharacteristics for the single-crystal FET (100 nm and 100 μm gate length and width, respectively) reported in [5]. In this example, the charge control behavior is markedly more linear than in our in-house devices; it is worth noticing that it is still well captured by the model.

The extraction of the equivalent circuit model is completed with the identification of the parameters of the capacitive components. This is done by fitting the S-parameters as a function of frequency, for different bias points.

An example of measured and fitted S-parameters, for a bias point close to the one exhibiting the maximum transconductance, is shown in Fig. 5 for the first device generation.

4.2. Validation against large-signal power measurements

To conclude the model validation, large-signal simulations have been carried out in order to evaluate the RF power performance of the first and second generation devices under class A operation, using the optimum load impedances derived from load-pull measurements [20, 21]. Fig. 6 compares the simulated against measured P_{in}-P_{out} curves, gain and power added efficiency (PAE) at 2 GHz for the first generation devices biased at $V_{\mathrm{DS}} = -14\,\mathrm{V}$ and $V_{\mathrm{GS}} = -1\,\mathrm{V}$. A similar comparison os reported in Fig. 7 for a second generation device measured at 1 GHz and biased at $V_{\mathrm{DS}} = -14\,\mathrm{V}$ and $V_{\mathrm{GS}} = -1.15\,\mathrm{V}$.

Both examples stress the model capability to accurately predict the nonlinear device dynamic performance over a wide range of RF input power, in terms of output power, gain, and power added efficiency.

5. Conclusions

We have presented a large-signal nonlinear circuit-oriented model for polycrystalline and single-crystal H-terminated diamond MESFETs implemented within the Agilent ADS design suite; the model is derived from the Chalmers (Angelov) approach, starting from an analogy between the charge control laws in III-V HEMTs and in diamond FETs. Good agreement has been found between the simulated and experimental data in DC, small-signal

and RF power (large-signal) conditions, for both polycrystalline and single-crystal H-terminated diamond devices.

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[1] C. J. H. Wort and R. S. Balmer, "Diamond as an electronic material," *Materials Today*, vol. 11, no. 1-2, pp. 1–2, 2008.

[2] A. J. Tessmer, L. S. Plano, and D. L. Dreifus, "Current-Voltage Characteristics of In Situ Doped Polycrystalline Diamond Field-Effect Transistors", *Trans. Electron Dev.*, vol. 39, no. 11, pp. 2666–2667, 1992.

[3] T. Teraji, "Chemical Vapor Deposition of Homoepitaxial Diamond Films", in Phisics and Applications of CVD Diamond, edited by S. Koizumi, C. Nebel, and M. Nesladek, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim, 2008.

[4] A. Kubovic, A.Denisenko, W.Ebert, M. Kasu, I.Kallfass, E.Kohn, "Electronic surface barrier characteristics of H-terminated and surface conductive diamond", *Diam. Relat. Mater.*, vol. 13, pp. 755-760, 2004

[5] M. Kasu, K. Ueda, H. Ye, Y. Yamauchi, S. Sasaki, T. Makimoto, "2W/mm output power density at 1 GHz for diamond FETs," *Electron. Lett.*, vol. 41, no. 22, p. 1249, 2005.

[6] K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. J. Twitchen, G. A. Scarsbrook, S. E. Coe, "Diamond FET Using High-

Quality Polycrystalline Diamond With fT of 45 GHz and fmax of 120 GHz", *IEEE Electron Dev. Lett.* vol. 27, no. 7, pp. 570–572, 2006.

[7] P. Calvani, A. Corsaro, M. Girolami, F. Sinisi, D. M. Trucchi, M. C. Rossi, G. Conte, S. Carta, E. Giovine, S. Lavagna, E. Limiti, V. Ralchenko, "DC and RF performance of surface channel MESFETs on H-terminated polycrystalline diamond," *Diam. Relat. Mater.*, vol. 18, pp. 786–788, 2009.

[8] V. Camarchia, F. Cappelluti, G. Ghione, M.C. Rossi, P. Calvani, G. Conte, B. Pasciuto, E. Limiti, D. Dominijanni, E. Giovine, "RF power performance evaluation of surface channel diamond MESFETs", *Solid State Electron.*, vol. 55, pp. 19–24, 2011.

[9] H. El-Hajja, A. Denisenko, A. Kaisera, R.S. Balmerb and E. Kohn, "Diamond MISFET based on boron delta-doped channel", *Diam. Relat. Mater.*, vol. 17, pp. 1259-1263, 2008.

[10] M.I. Landstrass and K.V. Rabi, "Resistivity of chemical vapor deposited diamond films", *Appl. Phys. Lett.*, vol. 55, p. 975, 1989.

[11] K. Hirama, T. Koshiba, K. Yohara, H. Takayanagi, S. Yamauchi, M. Satoh and H. Kawarada, "High-performance p-channel diamond MOSFETs with alumina gate insulator," Proceedings of the *IEEE International Electron Devices Meeting*, IEDM 2007, pp.873–876, 2007

[12] I. Angelov, H. Zirath, N. Rosman, "A new empirical nonlinear model for HEMT and MESFET devices ," *IEEE Trans. Microw. Theory Tech.*, vol.40, pp 2258–2266, 1992.

[13] H. Morkoc, H. Unlu, G. Ji, "Principles and Technology of Modfets", John Wiley & Sons Inc., 1991.

[14] I. Angelov, H. Zirath, N. Rorsman, "Validation of a Nonlinear Transistor Model by Power Spectrum Characteristics of HEMTs and MESFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 43, no. 5, pp. 1046–1052, 1995.

[15] H. Rodin, P. Roblin, "A MODFET dc Model with Improved Pinchoff and Saturation Characteristics ," *Trans. Electron Dev.*, vol. 33, no. 5, pp. 664–672, 1986.

[16] J. Ristein, "Surface science of diamond: familiar and amazing", *Surf. Sci.*, vol. 600, p. 3677, 2006.

[17] M. Kasu, K. Ueda, H. Kageshima, Y. Yamauchi, "Gate interfacial layer in hydrogen-terminated diamond field-effect transistors", *Diam. Relat. Mater.*, vol. 17, pp. 741-744, 2008.

[18] D. Kueck, A. Schmidt, A. Denisenko, E. Kohn, "Analysis of passivated diamond surface channel FET in dual-gate configuration: Localizing the surface acceptor," *Diam. Relat. Mater.*, vol. 19, pp. 166-170, 2010

[19] ADS Release 2005A Documentation, Agilent EEsof EDA, 2005.

[20] M. Pirola, V. Teppati, V. Camarchia, "Microwave Measurements Part I: Linear Measurements," *IEEE Instrumentation and Measurement Magazine*, Vol. 10-2, pp. 14-19, 2007.

[21] V. Camarchia, V. Teppati, S. Corbellini, M. Pirola, "Microwave Mea-

surements. Part II - Nonlinear Measurements," *IEEE Instrumentation and Measurement Magazine*, Vol. 10-3, pp. 34-39, 2007.

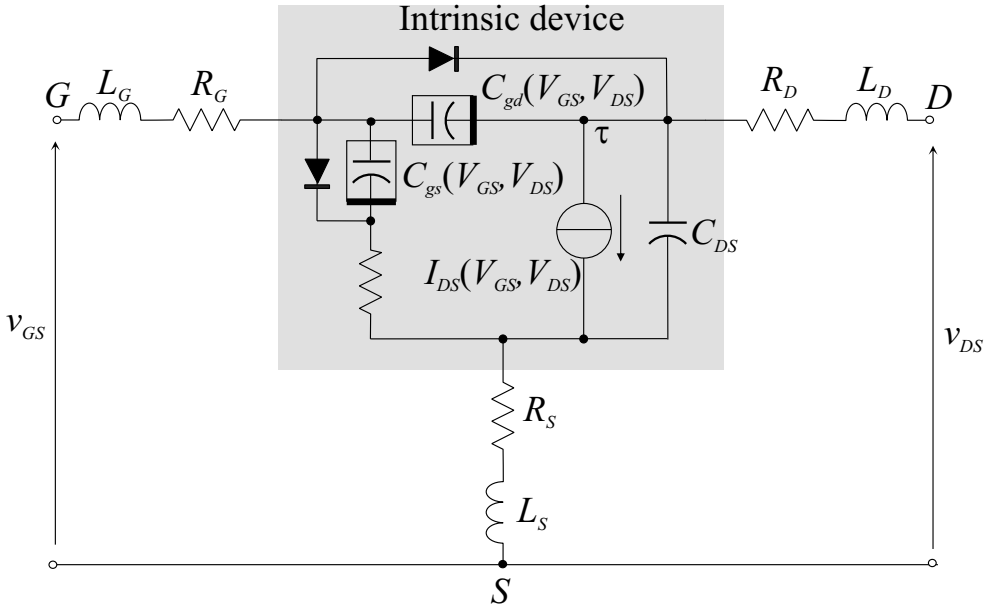

Figure 1: Equivalent circuit scheme of the implemented Chalmers (Angelov) model.

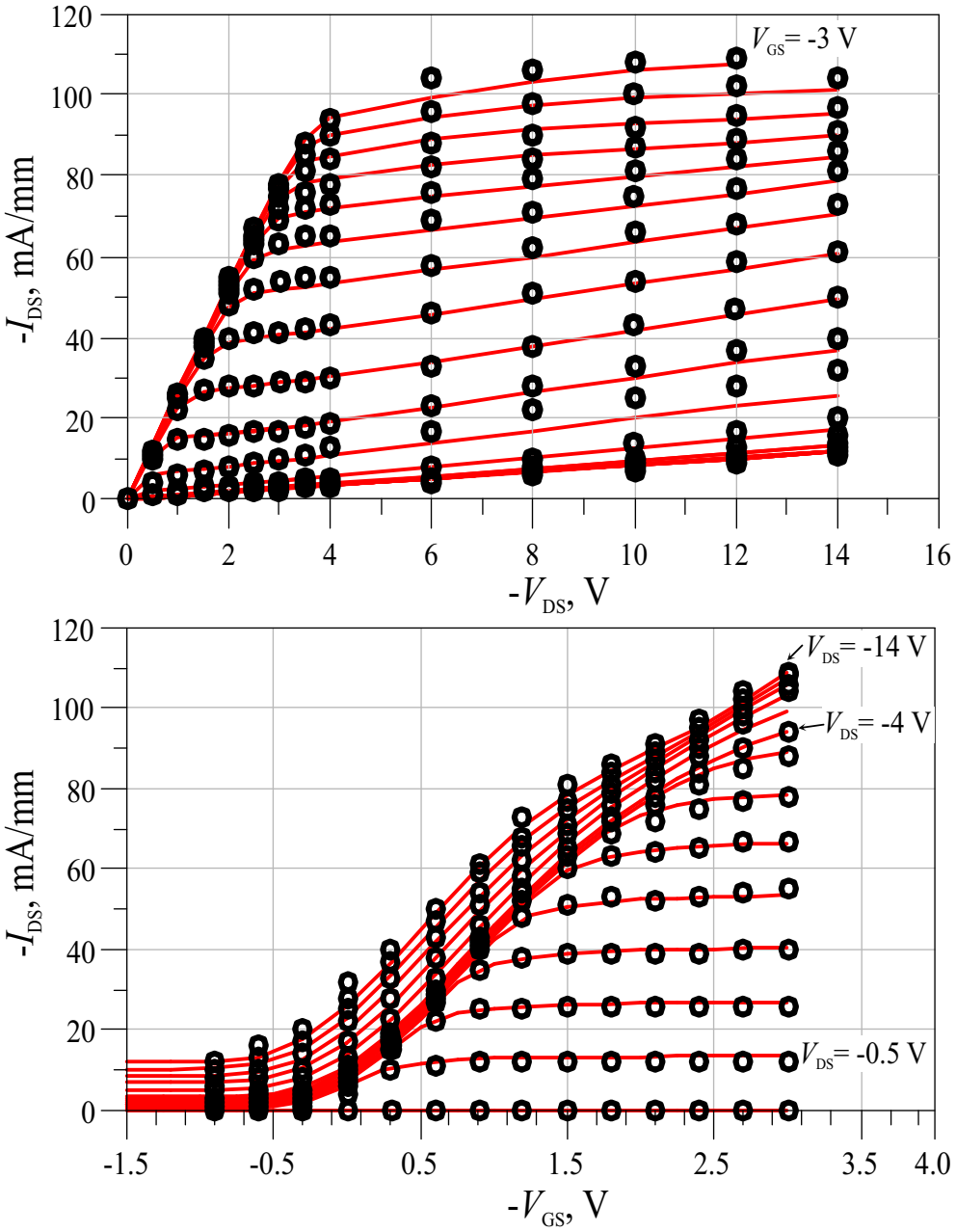

Figure 2: Above: comparison between the measured (symbols) and modeled (solid lines) output characteristics of a first generation device with V_{DS} from 0 V to -14 V, and V_{GS} from 0.9 V to -3 V (upper curve) with -0.3 V step. Below: corresponding measured (symbols) and modeled (solid lines) transcharacteristics for V_{GS} from 1.5 V to -3 V, and V_{DS} from 0 V to -14 V; V_{DS} step is -0.5 V in the range (0, -4 V), and -2 V in the range (-4 V, -14 V).

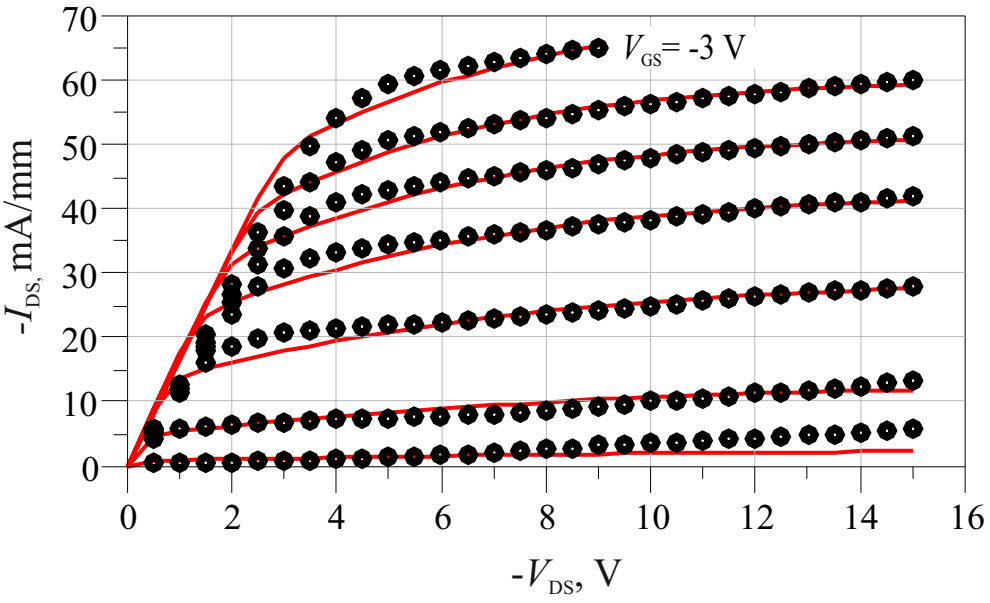

Figure 3: Comparison between the measured (symbols) and modeled (solid lines) output characteristics of a second generation device with V_{DS} from 0 V to -15 V, and V_{GS} from 0 V to -3 V (upper curve) with step of -0.5 V.

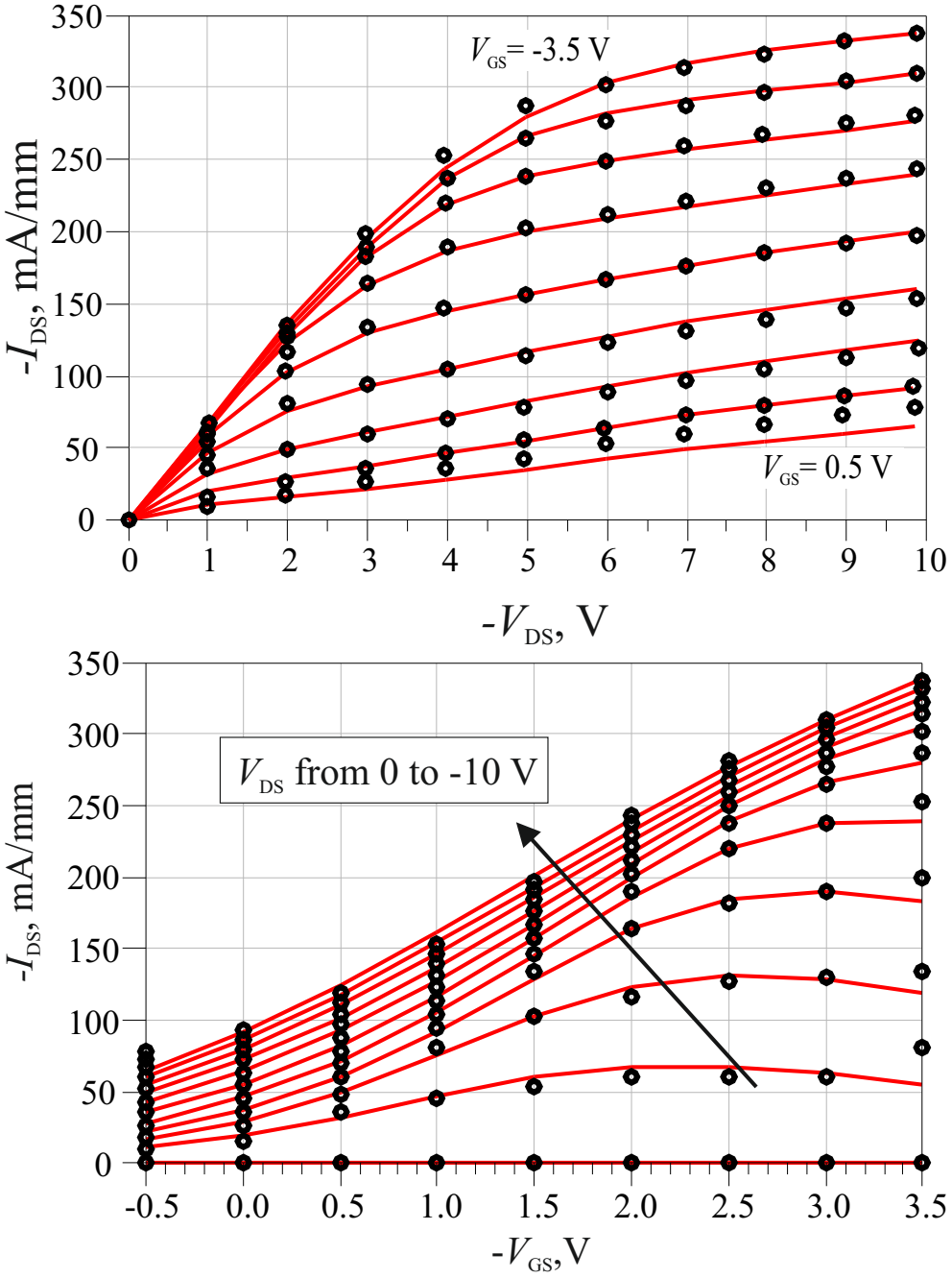

Figure 4: Above: comparison between the measured (symbols) and modeled (solid lines) output characteristics of the single-crystal FET (100 nm and 100 μm gate length and width, respectively) reported in [5] with V_{DS} from 0 V to -10 V, and V_{GS} from 0.5 V to -3.5 V (upper curve) with step of -0.5 V. Below: corresponding measured (symbols) and modeled (solid lines) transcharacteristics.

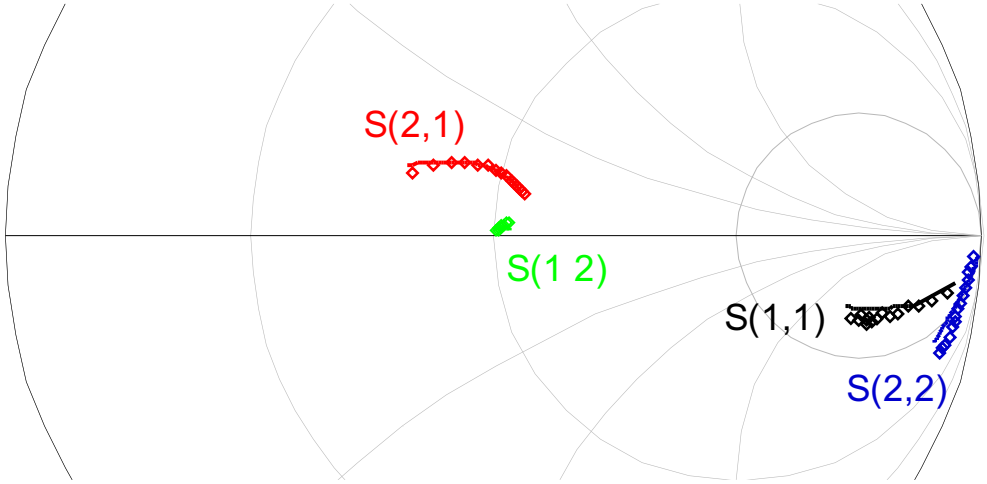

Figure 5: Comparison between measured (symbols) and modeled (solid lines) scattering parameters of a fist generation device at the bias point $V_{\mathrm{DS}} = -14$ V, $V_{\mathrm{GS}} = -0.9$ V.

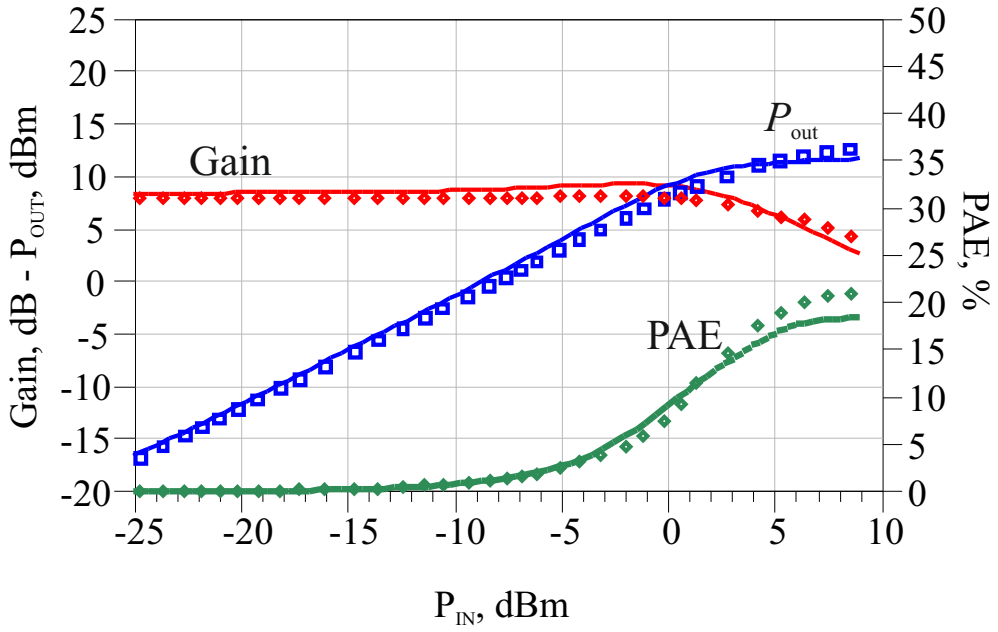

Figure 6: 2 GHz power sweep on the PAE optimum load of a first generation device. Power gain, output power and PAE for $V_{\mathrm{GS}} = -1\,\mathrm{V}$, and $V_{\mathrm{DS}} = -14\,\mathrm{V}$.

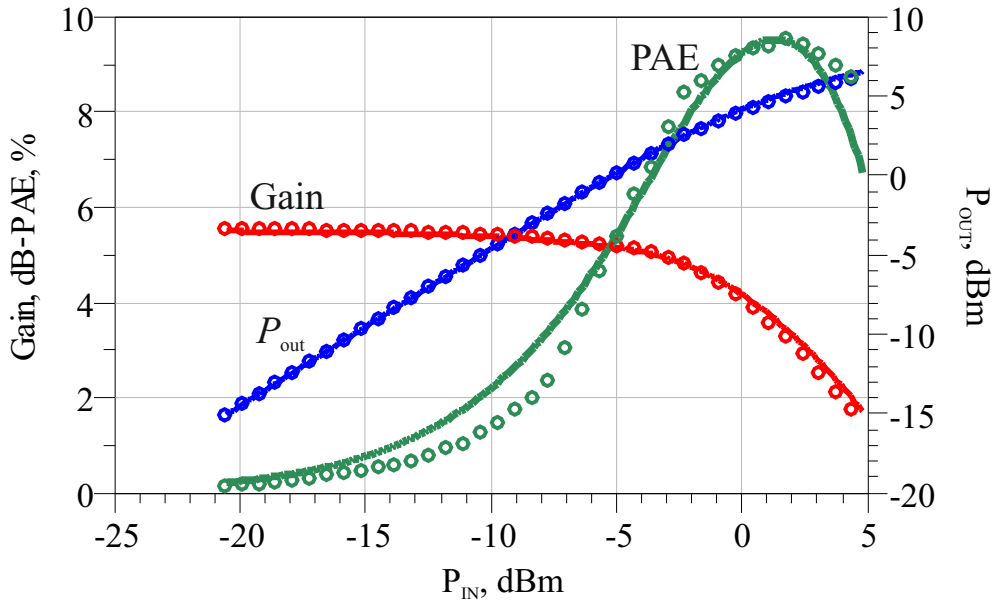

Figure 7: 1 GHz power sweep on the PAE optimum load of a second generation device. Power gain, output power and PAE for $V_{\mathrm{GS}} = -1.15\,\mathrm{V}$, and $V_{\mathrm{DS}} = -14\,\mathrm{V}$.