Use of FRAM memories in spacecrafts

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Use of FRAM Memories in Spacecrafts

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1. Introduction

This chapter shows some applications of commercial ferroelectric memories in the space. The discussion goes through the description of the theory behind their usage in this environment and describes the techniques used to achieve the desired reliability in real designs.
We are focusing on the *low-Earth orbit*, or LEO, the zone surrounding the Earth between $500 \div 800$ km, characterized by many challenging aspects, mainly related to the reduced atmosphere. Indeed the biggest problem of this environment is given by the presence of high-energy particles (not filtered by atmosphere and the Van Allen belts) hitting the active areas of electronic devices. These particles are thus reducing the reliability of the integrated circuits (i.e., their life or the life of information stored in them), affecting the reliability of the complete space-borne mission.
Other issues are related to the reduced cooling effect due to the lack of air convection movements: electronic systems have to reduce at most the power consumption, in order to decrease the power to be dissipated. Both power consumption and heat dissipation can be achieved using commercial low-power devices and low-power techniques (i.e., power cycling, smart power management policies, ...).
We motivate the use of FeRAM memories and propose some architectural solutions which can mitigate the effects of cosmic rays, without using expensive radiation-hardened space components. The choice of using commercial-off-the-shelf components (COTS) improves the overall characteristics of the whole avionic system, since it helps reducing its costs, reducing the power consumption (and so the power to be dissipated in the environment) and increases the re-usability of existing projects and documentation.
We applied our considerations and techniques to some small satellites developed in our research group during the last years. We cover two main projects: the first is a small prototype which was designed few years ago and launched in 2006; the second is a more advanced and challenging project aimed at developing a modular platform for small-sized satellites, which is still on-going. Both of them contain FeRAM devices and we show here how these devices have been introduced and how they can actually increase the global avionic performance and reliability. We discuss which are our constraints on the functional and architectural point of view (memory size, power consumption, latency, reliability) and which are the reasons for using FeRAM memories in our applications. In both designs we have performed simulation of the chip behavior in space through some space simulation environments (i.e., SPENVIS, CREME) to analyze the reliability of our design in this environment.
At the end we draw some conclusions on the work done and on the results we have, tracing further steps and considerations for future applications.

2. Technical background: the FeRAM cell

The idea of using ferroelectric materials to store digital data dates back to 1952, but it was practically implemented only starting from the 80s. The ferroelectric RAM cell, known as FeRAM or FRAM, is conceptually similar to the DRAM cell, in that a single capacitor stores one bit of information and the cell is connected to a memory column via a single pass transistor (1T-1C cell, although 2T cells are also common). The big difference lies in the dielectric of the storage capacitor: while DRAM cells use a layer of standard linear material, the dielectric of a FeRAM cell is made of ferroelectric material, usually PZT (lead zirconate titanate).
Using a ferroelectric dielectric makes the cell behave very differently from a DRAM cell, for several reasons. On one side, the dielectric constant of ferroelectric materials is very high, so that it is possible to create larger capacitors in a small space; on the other, the material exhibits two stable polarization conditions and it is possible to switch between them by means of applying an electric field of different polarity. The polarization will be kept after removing the applied field, so that it is possible to link the polarization state to a logic state and that state will be maintained also in absence of power supply. This means that the FeRAM cell is non volatile and that no refresh is necessary to keep the information in the memory.
Going a bit more into details, while in a DRAM cell the capacitor has one of the electrodes grounded, in the FeRAM cell the corresponding electrode is connected to a so-called driveline. During a write cycle the driveline (dl) is driven to complementary voltage with respect to the bitline (bl): $bl = 0\,\mathrm{V} \rightarrow dl = V_{dd}$; $bl = V_{dd} \rightarrow dl = 0\,\mathrm{V}$. In this way it is possible to provide positive electric field to write a 1 and negative field to write a 0, without need for dual polarity supply voltage.
Like for DRAMs, the reading process is destructive: it is not possible to read the contents of a cell without actually clearing it, because of the way the information is stored in the device. To know which of the two possible polarization states the dielectric holds, the only way consists in writing a new value to the cell with the bitline pre-charged but in high impedance state. Depending on the previous polarization of the cell, this process will or will not produce a voltage pulse out of the bitline.
For our purposes, there is no need to go into further details of the process, the key issue is that the information in the cell is not related to the charge stored in the capacitor but to the polarization of the dielectric.
Read and write cycles require basically the same operations and can both be completed in times in the order of tens of nanoseconds.

3. Technical background: Heavy ions and total dose

When selecting components for space missions, the key issue is reliability. Electronic systems designed for spacecrafts are normally built using space qualified components. These devices undergo special treatment to conform to specs identical or similar to MIL standards.
Regular commercial, military or scientific space missions from national or international space agencies have budgets allowing the designers to work only with space qualified components, but in the last few years many universities successfully completed and launched small satellites built using commercial-off-the-shelf (COTS) components. Their choice was mainly driven by having budgets several orders of magnitude smaller than those of regular spacecrafts.
Special considerations have to be taken when selecting COTS components for space missions. Let's analyze the main point to take care of:

- radiation: at ground level, the atmosphere constitutes an effective shield to incoming space radiations. Outside the atmosphere the radiation levels are much higher and impose severe limitations on electronics. We will evaluate them in details in the following.
- pressure: no atmosphere is present in orbit. This fact creates two main consequences: pressure is very low and power dissipation through convection is impossible. The low pressure limits the use of devices with liquid components (like electrolytic capacitors) and it is necessary to check that the packages of electronic components do not emit dangerous gases and do not break during depressurization phase, so outgassing and offgassing tests are necessary. Power dissipation limitations are not normally of concern for low power devices like memories.
- temperature: even if outside temperature can be extreme in light and in darkness, inside small satellites it can be demonstrated that temperature is not a big concern. Temperature remains in the range $-10\,^{\circ}\mathrm{C}$ to $20\,^{\circ}\mathrm{C}$, so normal devices rated for automotive use are well suited for operation inside a satellite (at least relating to this parameter).
- vibration: heavy vibrations are normal during the launch phase of the mission. Again, automotive devices are normally designed to sustain this vibration level.

At the moment there are no FeRAM devices conforming to space specs, but it is possible to obtain components graded for the automotive market. The main concern in using such devices is the radiation environment, while the other specs are reasonably met.
Radiation in space comes from different sources. The Sun is the main emitting body to be considered, but also background cosmic rays have to be taken into account. The electromagnetic field of the Earth plays a significant role in shielding incoming particles, so that radiation levels will be different depending on the orbital parameters of the spacecraft.
Solar flares and 11 years solar emission cycle have to be carefully considered, but plenty of data was accumulated during years of space activities, so that now we have a good characterization of the radiation environment around the Earth and it is possible to know the exposure levels for a specific space mission with a high level of confidence (see for example SPENVIS).
The damages produced by the incoming radiation can be divided in two categories: cumulative effects of the dose received, known as TID or Total Ionizing Dose, and effects of a single particle hitting the device, named SEE, Single Event Effects (for a more comprehensive introduction see NASA-Gsfc (2000)).
Total dose accounts for a degradation of the performances of the transistors (MOSFETs and BJTs). In particular, on MOSFET devices the main problem comes from a gradual shift in the threshold voltage. Above a certain TID this threshold shift is so high that the transistor cannot switch anymore, causing a functional failure of the circuit. TID is measured in $\mathrm{krad(Si)}$. It is relatively simple to test the behavior of a device for TID. X-ray apparatuses derived from those used in medical applications suitable for the scope are available at a relatively low cost.
Single events create several failures depending on the device involved, the technology and other conditions. The particles responsible for SEE are mainly heavy ions and protons. When a high energy particle hits the surface of a silicon chip, part of its energy is transferred to the chip as electric charge (secondary electrons emission). The amount of energy transferred is called LET (Linear Energy Transfer), measured in $\mathrm{MeV\,cm^2\,mg^{-1}}$.
The main effects are:

- Single Event Upset (SEU): this is a recoverable error that appears in memory devices. The impacting particle hits the sensible area of a storage device, for example the capacitor of a DRAM cell, and transfers an amount of charge sufficient to alter the contents of the

memory. This damage is called a soft error, meaning that the damage is not permanent and it is sufficient to rewrite the memory to restore correct behavior.

- Single Event Latch-up (SEL): this is a potentially destructive error typical of CMOS circuits. The structure of a complementary gate in CMOS logic contains a parasitic PNPN device, similar to an SCR, which is not operated under normal conditions, but can be triggered by a high energy particle hitting the gate of the SCR device. Once triggered, the SCR remains ON until the power supply is switched off. When this device is on, it creates a low resistance path between power supply and ground. The current can be very high, creating an hot spot in the device that can in turn permanently damage it.
- Single Event Functional Interrupt (SEFI): it is defined as erratic behavior of a complex circuit due to the consequences of the impact of a single particle. It is similar to SEU, but the affected area, instead of being a simple memory cell, is a FSM or other sequential circuit which is forced into an unwanted state by the event. The error may persist until the next reset or may be recovered at some time. In the case of a memory device, a SEFI occurring in the control part of the device can lead to reprogramming a big area of the matrix (typically a whole row).
- Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB): these damages occur when a particle hits the active area of a power MOSFET transistor under certain bias conditions, creating a physical damage, such as oxide breakdown for SEGR, overheating due to large currents for SEB, that prevents normal operation of the device. Low power devices such as memories are not subject to SEB, but SEGR has been reported if a particle hits a EEPROM or Flash memory during the erase procedure, due to the relatively high voltages used during such operation.

Testing one device for SEE typically includes exposing it to a precise flux of particles, generally heavy ions, characterized by a specific LET, for a specified amount of time. The number of detected errors allows the determination of the device sensitive area, or cross-section, at the ions' LET. This procedure has to be repeated for different LETs, so that a graph showing the cross-section of the device as a function of the LET can be derived. This process is very expensive because this kind of tests can only be performed in a cyclotron. Alternative lower cost methods include the use of laser pulses or small radioactive sources based on Californium 252 which emits heavy ions of different LET, but in this case it is difficult to relate test results to more rigorous cyclotron methods.
Once a device is characterized for TID and SEE behavior, knowing the expected radiation environment at the programmed orbit, it is possible to predict which errors can be expected during operation and what is the relevant error rate.

4. FeRAM strengths

In the previous sections we have introduced the FeRAM technology and described the challenges posed by the space environment.
What are the advantages of using FeRAM devices in space subsystems? The three main design parameters of the electronic systems of small satellites are power consumption, physical dimensions and radiation environment behavior. Let's evaluate the first two items: the electric power in the satellite comes from solar panels, which are necessarily of small dimensions, leading to few watts of average power to cover all the satellite's functions, so it is necessary to make the best use of any mW of available power. Launch costs are directly proportional to the mass of the system, so it is mandatory to reduce as much as possible dimensions and mass of the electronic systems.

As previously stated, FeRAM memories are RAM devices, meaning that read and write procedures do not differ significantly and random write is possible without the need of a previous erase of a cell, but they are also non volatile, so that information is not lost after removing power supply.
We can therefore compare FeRAM memories both to RAMs and Flash devices. It is possible to note that in principle the structure of the FeRAM memory cell is very similar to the DRAM one, but, not relying on the charge in the capacitor, it does not request the refresh procedure, which is time and power consuming. In fact in DRAM devices most of the power is used by the refresh procedure. FeRAM cells are bigger than DRAMs, so it is not possible to use FeRAM memories to store huge amount of data. Today's top density is 128 Mibit per chip (prototype by Toshiba, Shiga et al. (2010)) but most of the available devices are in the 1 to 8 Mibit range (RAMTRON). This is probably more a problem of amount of financial investments in this technology than of intrinsic limitations of the ferroelectric capacitor used in the cell. In any case, memory requirements of small satellites are normally compatible with the size of available FeRAM devices, except for imaging payloads if local storage of a certain number of images is mandatory.
The most interesting application of our technology is however evident when comparing with Flash or EEPROM devices. Read operations in FeRAM and Flash devices are equivalent both in speed and power requirements. Write operations on a Flash memory are quite complex. The first phase consists in a page erase, which takes a time in the order of tens of milliseconds, followed by a write operation of the new values. Even to rewrite a byte, one full page has to be erased and the unmodified cells have to be rewritten in place. The erase procedure requires a high supply voltage (negative for erase, positive for write) which is internally generated by the device using a charge pump circuit. EEPROM devices can be reprogrammed on a single byte basis, speeding up the write process when a single random byte has to be altered, but the need for high voltages is the same as for Flash devices and the operation can be completed in tens of microseconds. A comparison in power and speed can be found in Sheikholeslami & Gulak (2000), although a bit out of date. Another aspect to be considered is the device endurance. The number of write cycles that can be sustained by a Flash or EEPROM device is in the order of $1 \times 10^4 \div 1 \times 10^5$, while FeRAM memories can be written more that 1×10^{12} times, with 1×10^{16} cycles being claimed by TI and RAMTRON on new devices. The same drawback of lower device density noted above in the comparison with DRAMs is applicable to the comparison with Flash devices.
As a summary, FeRAM devices are attractive for use in small spacecrafts as a replacement for both RAM and Flash memories when the size of the memory is small, because of the ease of use, non volatility (when compared to RAM), the low power requirements, the speed advantage in the write process and the endurance, when comparing with Flash memories.
The last, but not least, point to take into consideration is the radiation behavior. Several tests performed on the FeRAM cells show that the SEU response is very good (Benedetto et al. (1999)), definitely better than the one of most Flash or DRAM devices, indicating that this technology is very appealing for space applications.

5. FeRAM weakness

The biggest obstacle at the moment in using FeRAM devices in spacecrafts is the lack of commercially available radiation hardened components. It is clear from the previous section that the memory cell has several advantages with respect to other non volatile competing technologies, but at the moment the only devices available off the shelf are from Ramtron and Fujitsu. There is almost no literature on heavy ions behavior of these chips, apart from a single

paper reporting SEU tests on Hynix devices (Hynix does not have any FeRAM device in its catalog nowadays) and Ramtron 256 Kibit and 64 Kibit memories (Scheick et al. (2004)). The results of these tests were disappointing: although no SEU was observed in the memory cells, there were errors involving several cells at a time. These errors are compatible with SEUs hitting the CMOS control logic of the array, triggering unwanted writes to the memory. This means that, even if the memory cell itself is immune or very resistant to heavy ions induced errors, this is not true for the surrounding logic built using a standard CMOS process.
It is possible to harden the memory control logic, either by using a rad-hard process or by hardening by design, as demonstrated for example in Kamp et al. (2005), but no such devices are commercially available at the moment.
TID behavior of Ramtron devices was tested by JPL and included in a report by Nguyen & Scheick (2001). The results are compatible with LEO orbit operations.
It is interesting to note that Fujitsu sells radiation resistant RF-ID modules that comprise a FeRAM memory for non volatile storage. Another product from the same manufacturer is a microcontroller featuring FeRAM as a substitute for both RAM and Flash memories. The device is not intended for operation in hostile environment.

6. Possible solutions

The problems highlighted in the previous section can be overcome in two different ways. The first is to design a FeRAM memory specifically for space applications, the second is to use COTS devices taking specific system design measures to prevent the failures due to the CMOS logic surrounding the memory array.
Obviously the first solution is preferable, but it involves high development and production costs and time, so it is not affordable when designing low cost spacecrafts such as university satellites.
In details, to create a rad-hard version of a FeRAM memory it is necessary to use a rad-hard CMOS process to build row and column decoders and the read/write control logic. Rad-hard processes normally use SOI (silicon on insulator) or SOS (silicon on sapphire) techniques. As an alternative, the addition of an epitaxial layer to the substrate of a standard CMOS process can lead to improved performances, at least about SEL sensitivity. Since it is not difficult to add a ferroelectric layer to a rad-hard CMOS process, this way is feasible, but the associated costs are very high.
A variation on this subject is radiation hardening by design. An example of this technique is available in Philpy et al. (2003). Hardening by design does not require special processes but only following special design rules that improve radiation behavior of the device. This way is probably less expensive than using a rad-hard process, but it requires nevertheless the design of special components.
The alternative of using COTS devices is very attractive and is feasible in the case of FeRAM memories because of the characteristics of these devices.
Let us analyze more in details the problems of commercial devices and how to overcome them. As shown from the results of the tests performed by Scheick et al. (2004), the risks of data corruption or physical damage come from the standard CMOS logic surrounding the memory array. We have to improve the device sensitivity to SEL and to soft errors. TID is not a problem because the performance reported in Nguyen & Scheick (2001) is reasonable for LEO missions.
To prevent the risk of loss of the device due to latch-up, it is possible to monitor the supply current and to switch off the chip in case of overload, indicating SEL occurrence. This procedure has to be done very carefully in CMOS logic, because it is not normally sufficient

to remove power supply to be sure to reset the parasitic structure responsible for latch-up. The structure of the input circuitry of CMOS devices always includes clamp diodes, so even removing power supply it is possible to continue to supply the chip via inputs at logic high state.
SEL protection circuitry is mandatory when using COTS devices in space applications, so we developed an hybrid circuit that monitors supply current to a satellite subsystem, switches off power supply when a SEL is detected and sends an interrupt to the associated microcomputer to signal the event. Depending on the subsystem involved, the microcomputer can either cycle power supply to a complete portion of the satellite or insure in other ways that no signals at logic high state are connected to the subsystem affected by the SEL.
Soft errors are the second problem to address. The non volatility of the information stored in the FeRAM is a great help in this respect. Soft errors can only occur when the memory is powered, but our devices need power supply only when it is necessary to read or write information, not to maintain internal data. This suggests a strategy for SEU and SEFI effects mitigation: the device is powered only during read or write operations, switched off otherwise. This strategy is possible only if the memory stores data which are to be seldom read or written, not if the device is used to store the active CPU program. Our use of FeRAM memories falls indeed in the first case: our systems have microcontrollers equipped with internal memory for program and data, external memory is used only to store telemetry, statistics and backup configuration data and program. The duty cycle of power supply is therefore very low, and this ensures a drastic reduction of SEU/SEFI sensitivity. We adopt a second strategy for important data, such as the backup copy of processor program: we store separate copies on multiple devices, furthermore the data are associated with strong error detection CRC codes, so that it is possible to detect if what is stored in a device was corrupted by SEU/SEFI. Corrupted data are regenerated from the other copies so the system integrity can be guaranteed.
In the following sections we will present more details on our application and on the adopted solutions, together with an estimate of the reliability of our approach.

7. Design and analysis of commercial components in the space

After discussing some possible solutions to overcome the problem of using FeRAM components in the space, in the following sections we are detailing two examples of their usage taken from real-life applications developed in our research group. Both examples are using commercially available components and are exploiting some architectural solutions to mitigate the radiation effects on these devices.

7.1 The PiCPoT nano-satellite

In response to industry and academic research interests, in 2004 we started a design activity at Electronics Dept. in tight cooperation with our Aerospace Engineering Dept. and other departments of our University, aimed at developing and manufacturing a low-cost prototype of a fully operational nanosatellite. The design activity lasted three years, gathered about 10 people among professors and PhD students, plus about 20 undergraduate students (the former for the whole period, while the latter stayed for shorted period, between 6 and 12 months each).
After an effort of about 12 man-years (staff+student) for design, manufacturing and testing, we built a flight model and two engineering models of the PiCPoT satellite shown in Fig. 1.
The satellite has been completely designed using COTS devices, with the only exception of solar panels. It contains (see Fig. 2): five solar panels; six battery packs; three cameras

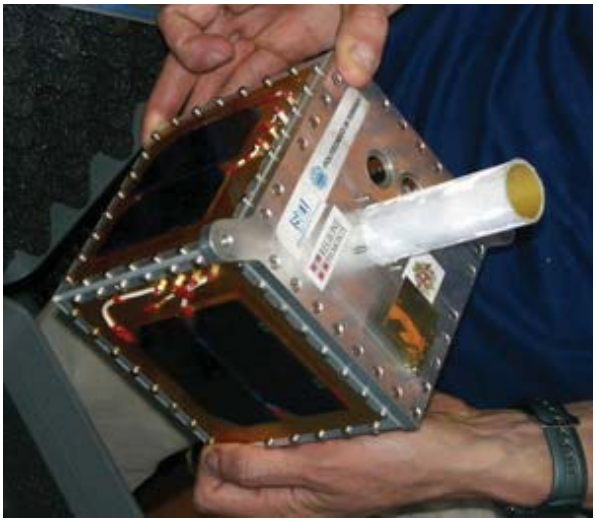

Fig. 1. The engineering model of PiCPoT

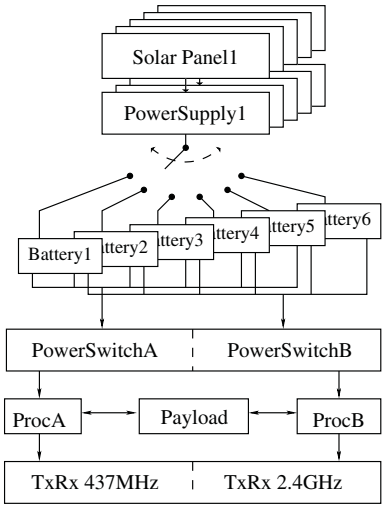

Fig. 2. PiCPoT internal structure

with different focal lengths; five processors in full redundancy; two RX-TX communication modules with antennas operating at 437 MHz and 2.4 GHz, respectively; six PCBs, all of them hosted in a cubic aluminum case, 13 cm in side. The radiation behavior of PiCPoT was carefully considered, because it is a rather complex system containing, as noted, 5 processors, different kind of memories and programmable logic devices.
In particular we divided the soft errors in the memory devices in three categories:

1. errors on dynamic data and/or in code segments resident in volatile memory;
2. errors on data stored in non-volatile memory;

3. errors on program code stored in non-volatile memory.

The outcome of such events may be wrong data, wrong behavior (if the event affects some data dependent control, for instance) or even a crash (i.e., if the upset results in a non-existent op-code for a processor).
There are several solutions to address this problem, each with its own advantages and shortcomings. Some cope with all three kind of errors, others do not address all of them. We applied different techniques in various parts of the satellite, depending on the kind of protection we wanted to provide. The selection was driven by the need to keep the design simple and power consumption and total budget low. Therefore we did not use radiation-hardened devices (too expensive and against the whole philosophy of the project to use COTS components wherever possible), nor memories with error correcting code (ECC), useful only for dynamic data and which do not protect against multiple bit upsets.
Even if no radiation-hardened components were used, the susceptibility of COTS components to radiation can be very different. Careful selection of the best devices for the application allows us to strongly reduce the probability of single event upsets.
We examined several kind of memories in search for the best ones, and in particular we considered:

- *Dynamic RAM* (DRAM): it is the most dense memory and it is used when large amount of memory is required. It is rather sensitive to radiations. Those parts of the satellite that depend on this kind of memory must be protected in some way.
- *Static RAM* (SRAM): it has been shown by Ziegler et al. (1996) that these are more sensitive to radiation than dynamic RAMs, but have the advantage of consuming less power. Processor registers also use the very same technology.
- *Flash*: Although the charge pump mechanism to reprogram a cell has been shown to be susceptible to TID effects, the cell proved to be robust against SEU, Miyahira & Swift (1998), because more energy is required to change the state of a bit compared to conventional RAM devices. For this reason, flash devices are more tolerant to radiation and are a good candidate for vital data and code.
- *Ferroelectric RAM* (FeRAM): Compared to flash memories, writing operations on an FeRAM can operate at lower voltages and are 2 to 3 order of magnitude faster. This allows saving energy and at the same time maintaining the good tolerance to radiation of flash devices. This technology looks promising for space applications but few information about the behavior of FeRAM in space is available in the literature.

We used a mix of all the above memories because strengths and weaknesses were often complementary. When available, data on radiation effects on memories was used to compare similar devices and select the best one. Dynamic and static memories were used for execution, while Flash and FeRAM were used for permanent data and program storage. Being highly experimental and having only a few documentation on their behavior, FeRAM was only used to hold non-vital data, such as the telemetry stream acquired from sensors.

7.2 Operation, timing, fault tolerance

The design of PiCPoT is aimed at high tolerance to faults and radiation effects while using only COTS components.
The whole design has been based on a redundant architecture we developed mixing both *hot* and *cold* redundancy techniques (Shooman (2001)). Architecture and operation are organized around a hot-redundant central *power management and timing unit*, that drives alternatively

two cold-redundant sub-satellites, called processing chain A and B, for housekeeping measurements (temperature, voltage, current), and a single payload board that controls the cameras. The two chains are switched on and off alternatively each minute to reduce the effects due to the presence of radiation.
The two sub-satellites have been developed by two different teams, using different components, in order to avoid the possibility of having the same technological or design issue on the two systems at the same time. One of the chains has been equipped with a ferroelectric RAM chip as main storage memory for telemetry data.

7.3 Design constraints

The design and the assembly of a satellite must abide tighter rules than usual "good and safe design" criteria applied for any electronic system. Moreover, the choice of using COTS components and technology, allowing failures at the device level, makes mandatory the adoption of design techniques which guarantee system operation, even in presence of limited failures.
The design constraints were those already mentioned in Sec. 3.
All mechanical and thermal specifications are easily met by integrated devices. Regarding cosmic rays, the planned orbit is close to the Van Allen belts, where a limited amount of heavy ions is present; these radiations may cause latch-up in CMOS devices and single-event upsets in memories. Due to the low orbit, total dose effects are limited.
As previously discussed, FeRAM devices are able to better cope with all these aspects since:

- This technology reduces the overall amount of energy required in normal operating mode with respect to Flash devices, so that the power to be dissipated is also reduced, allowing wider operating temperature conditions and improving the chip behavior in absence of air.
- The core memory requires lower operative voltages, the electromagnetic emissions are characterized by less energy and thus they are producing less interference in the satellite.
- The FeRAM cell is less radiation sensitive and thus it improves the overall behavior in presence of heavy ions.

7.4 Memory requirements

We selected the memory for the various subsystems of our satellite based on the following considerations.

7.4.1 Size

Knowing the amount of data we have to store is one of the main aspects when selecting a memory, reducing the number of available technologies and forcing several architectural clues in the overall project (as the the number of bit required to address it, the access speed, . . .).
In our case we had different kind of memory usages and thus different sizes required.
As a first issue we can identify two applications in our project: external memory in PiCPoT was used for storing telemetry data and for storing images (Passerone et al. (2008)). Obviously these two usages request different memory sizes and characteristics. Indeed, whilst for pictures we require a fairly big amount of data (usually some hundreds of kilobytes), for storing a telemetry history we only need few kilobytes. On the other hand, while loosing a part of an image can be negligible, or it can be tolerated, loosing telemetry data, thus loosing information on system behavior, can lead to difficult situations, especially in case of troubles. Table 1 is resuming these considerations.

Application	Memory Size	Available Tech.	Data loss
Telemetry	$(1 \div 10)$ kB	Flash, EEPROM, FeRAM	forbidden
Pictures	$(0.1 \div 1)$ MB	Flash, DRAM, SRAM	acceptable

Table 1. Memory size considerations.

7.4.2 Radiation tolerance

At the time we started the development of our satellite, a small number of studies had been published on the tolerance of commercial FeRAM components to the space environment, see Nguyen & Scheick (2001) and Scheick et al. (2004). Thanks to these works we were able to estimate the cross-section for the device chosen in our project. Comparing the cross-section with the data provided by SPENVIS, we verified the usability of such devices in space. Figure 3 provides the output data from the SPENVIS simulation, describing the total radiation dose for one year of activity. The worst case shielding inside our satellite is about 2 mm of aluminum.

Concerning TID, the studies mentioned above classified our devices as able to tolerate an exposure above 10 krad(Si) and the environmental simulation provided by SPENVIS was noting only 1 krad(Si) per year, so we were confident that our project was able to comply with our orbit without troubles.

At the time we developed our design, there was no direct SEU characterization for the device we selected, namely a Ramtron 25L256, 256 Kibit with SPI interface.

Therefore we tried to extrapolate the device cross-section considering the above published data and assuming similar performance from devices built using the same technology. Simulating the satellite orbit in LEO through SPENVIS we obtained the expected heavy ions flux, see Fig. 4. By using the estimated cross-section, we obtained in output an average SEU rate of 0.2 events/day. Moreover, we reduced the actual cross-section by powering off the device when not used. With a duty-cycle of 10 s/min, we are able to achieve an average SEU rate of one event per month, thus giving us a good reliability level for our application target (i.e., minimum mission time of three months).

7.5 Design strategies

Having demonstrated that a FeRAM device can fit our design target, we will now discuss how to improve, by using architectural solutions, the overall behavior of the memory when exposed to the space environment.

7.5.1 Reducing the single event latchup effects

Single event latch-up as exposed in Gray et al. (2001), or simply latch-up (LU), occurs when a parasitic SCR made by the couple of complementary MOS devices is turned on by high input voltages (this is the usual LU in ICs, caused for instance by input over-voltages) or by high energy particles which induce a small current (this is the case for a space device). The effect is a high, self-sustaining current flow, which can bring a high power dissipation and, in turn, device disruption.

LU-free circuits (latch-up cannot occur) can be designed by avoiding CMOS all-together, or by using radiation hardened technology; since one of the goals of PiCPoT is to explore the use of COTS components for space applications, we decided to keep only some critical parts LU-free by proper device selection, and to allow using standard CMOS devices in other circuits. These, however, must be LU-safe (latch-up can occur, but makes no harm), with specific protection circuits.

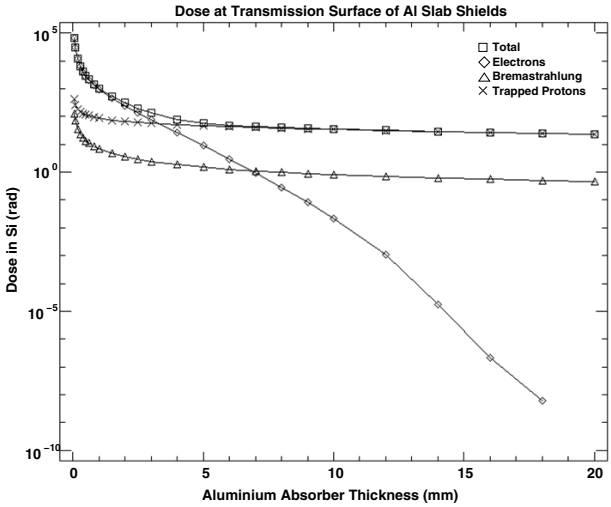

Fig. 3. Total dose radiation diagram with respect to the shield thickness in LEO orbit.

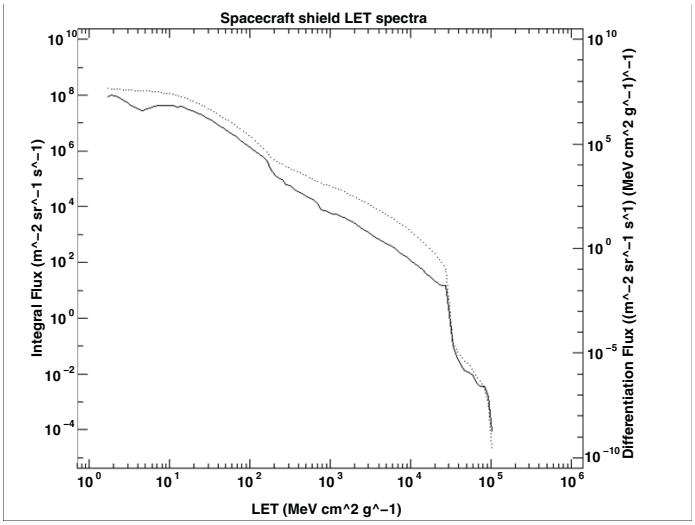

Fig. 4. Heavy ion flux vs. LET in LEO orbit.

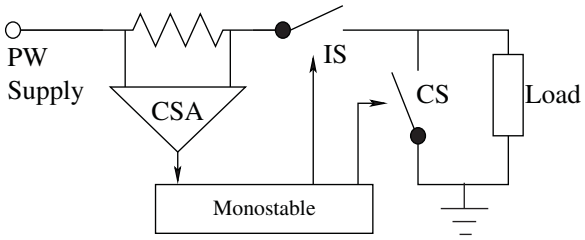

Fig. 5. Block diagram of latchup protection circuit.

The basic idea behind protection is to constantly measure current and to immediately turn the power off as soon as anomalous current consumption is detected. Once the transient event is over, normal operation can be restored. This technique is analogous to a watchdog timer, except that it actively monitors the circuit to be preserved, rather than waiting for the expiration of a deadline. Each supply path should have its own protection circuit, which should itself be LU-free, e.g. using only bipolar technology for its components.
The block diagram of the protection circuit of a single supply path is shown in Fig. 5, and includes:

- a current sense differential amplifier (CSA),
- a mono-stable circuit with threshold input,
- isolating and current-steering switches (IS and CS),

When the current crosses the limit set for anti-latch-up intervention (usually $2\times$ the maximum regular current), the mono-stable is triggered and isolates the load from the power sources for about 100 ms. To fully extinguish the LU, the shunt switch steers residual current away from the load.

7.5.2 Reducing the single event upset effects

One technique to approach the problem of SEU effects mitigation is to use redundancy. In general, at least three replicated units are necessary to implement a voting mechanism, where the majority wins and allows correction of a fault. The replicated unit can be a complete board (processor, memories and peripherals), a physical device on a board (three instances of the same component) or an abstract unit within a device (three memory segments in the same chip, holding identical information). This method potentially allows active identification of an SEU even in RAMs during the execution of a program, and to promptly act to correct it. However, the space available inside the satellite did not allow us to replicate identical boards (except for the system level duplications which are discussed in the remainder of this paper), or even devices within a board. Nonetheless, in some of the processor boards the program stored in Flash memory is maintained in multiple copies and a procedure to search for SEUs can be explicitly activated. Data, such as pictures or telemetry, on the other hand, are not protected and if an SEU occurs, the information downloaded to ground will simply be incorrect.
Since RAMs, both static and dynamic, including registers inside the processors, are the most sensitive devices to SEU, and they are not replicated, other techniques must be used to ensure proper behavior. Our solution is to periodically turn off processor boards and start a complete boot procedure. Given that the program is stored in flash memory (possibly with some duplication) and that RAMs go through a power cycle and reset, the soft error will be

completely eliminated. Clearly, data that have to persist for more than one power cycle have to be stored in some kind of non volatile memory.
Obviously, whatever command was being executed, a SEU will potentially result in wrong data or a crash. This however does not preclude the system to work correctly at the subsequent re-boot. The periodicity that was selected is 60 s: it allows smooth execution of all commands to be executed with a good margin. This technique is similar to a watchdog, but the chosen periodicity is a hard deadline and cannot be extended by the controlled processor boards.
Single event upsets can have different effects depending on the data they are affecting. If the memory contains raw data coming from sensors used for housekeeping or for simple monitoring, they are probably leading only to the invalidation of one or some of these data: the overall system behavior is not changed. But, if the memory involved is containing operating code or parameters used for system configurations, we can have a misbehavior in the operations executed by our satellite, eventually causing damages. Obviously the latter are more troublesome and have to be avoided in all the possible ways.
In particular, the FeRAM device contains some functional parameter and not only housekeeping data, therefore we had to make an extra effort in ensuring the memory tolerance to the harsh environment. As we exposed earlier in this chapter even if the FeRAM memory cell can resist to higher cosmic radiation levels than other technologies, the presence of CMOS elements in the boundary circuitry can cause changes in the stored data (SEFI). The solution we chose was to reduce the power on time, in order to reduce the time window where the memory is sensitive to radiation effects and to replicate in three different portions of the device the functional parameters. Replication of telemetry was not deemed vital and not performed.

7.5.3 Power considerations

PiCPoT is a portable system, even if unconventional. Indeed it is a battery based system and even if it is also powered by solar panels, it has to survive during the Sun eclipse periods (about 40 min per 90 min orbit), thus every part of the system should be optimized for power, as in all the portable devices we deal with everyday.
In Tab. 2 we can see the power budget for each subsystem and in particular for the on-board processors. This small amount of energy available has to be used effectively in all the processor boards, i.e., microcontrollers, analog conditioning, and memories.
In our case the external memory is used for two main purposes:

Configuration The OBC can be configured to select different available choices, thus at the beginning of each power cycle, the processor reads from the outer memory which configurations have been set and reacts accordingly. Typically these selections are changed only during the system programming, or by asking from ground to reconfigure the system in case of damages. Thus, the locations containing such information are mainly read.

Storage of telemetry data When we activate the OBC it acquires all the values of all the sensors available and reads all the event counters, in order to build a snapshot of telemetry data. After completion, telemetry is stored in the external memory, together with running statistics of all the parameters. These data are read when they have to be transmitted to ground. This usage is more focused on both reading and writing operations.

FeRAM devices have the advantage of being more power efficient in writing operations. Since we are accessing this memory in a balanced way for reading and writing, the usage of FeRAM devices helped us in reducing the amount of power required for writing operations. Moreover, being able of completing a writing operation in few tens of nano seconds, instead of tens of milliseconds (as in case of Flash devices), they allow further power saving, since the system can suspend earlier its operation.

Device	Duty Cycle	Peak Power	Avg Power
PowerSwitch	100%	20 mW	20 mW
Proc A & B	6%	200 mW	12 mW
Payload	0.5%	3.84 W	21 mW
TxRx	2.6%	17.2 W	443 mW
Losses in Batteries & switching			1.07 W
Solar Panels			-2.24 W
Margin			-674 mW

Table 2. Power budget

7.5.4 Project remarks

Unfortunately we were not able to test this design in space since the launcher blew up during the launch, causing the destruction of 14 nano-satellites (Malik (2006)). It has been a shame, since operational data from the design in the environment it has been designed for, would have produced a great feed-back on our design techniques and solutions. Luckily the grown experience has been reused in the new project we are working on, that is described in the next section.

7.6 A modular architecture for nano-satellites

Thanks to the experience got by the design of PiCPoT we decided to use again FeRAM devices in our new spaceborne project, called AraMiS, presented in Speretta et al. (2007). The aim of this project is to design, prototype and develop a new architecture for modular small satellites. The most effective way to reduce the cost of a nano- or micro-satellite mission is to reduce as much as possible design and non-recurrent fabrication costs, which usually account for more than 90% of the overall budget. Reducing them can be achieved only by sharing the design among a large number of missions.

Design reuse is the rationale behind the AraMiS project, that is to have a modular architecture based on a small number of flexible and powerful modules which can be reused as much as possible in different missions. Using the same module(s) more times obviously allows to share design, qualification and testing costs and to reduce the time-to-launch.

The first step in the AraMiS project has been to identify the most common and critical subsystems. We have then concentrated our efforts on the following subsystems, which are described in details in Speretta et al. (2007) and in Speretta et al. (2009):

1. mechanical subsystem;
2. power management subsystem;
3. telecommunication subsystem;
4. on-board processing subsystem;
5. payload support.

The basic architecture of AraMiS is based on one or more modular *intelligent tiles*. Most of them are to be regularly placed on the outer surface of the satellite and have a double function: *mechanical* and *functional*. The inner part of the satellite is mostly left empty (except for the on-board processor and payload support tile), to be filled by the user-defined payload, which is the only part to be designed and manufactured ad-hoc for each mission.

The *power management* subsystem aims at managing all the aspects related to energy, i.e., collecting energy from solar cells, storing it on the available batteries, and guaranteeing their correct discharge when modules requires energy to operate. The *telecommunication* subsystem

contains the modems, the transceivers, the radio-frequency components, and the antennas used to communicate with the ground stations. The *on-board processing* subsystem contains the main processors and units devoted to the computation and the high speed communication among the tiles and the modems. At last, the *payload* subsystem is the only part not designed at the moment, since it can vary from mission to mission, thus we only developed the communication and the mechanical interfaces.
Each tile is designed, manufactured and tested in relatively large quantities. Reuse also allows to put an increased design effort to compensate for the lower reliability of COTS devices, therefore achieving a reasonable system reliability at a reduced cost.

7.6.1 Modularity and customization

The aim of our design is to study, develop, and produce a structure, a set of tiles, and a set of interfaces to allow universities and small enterprise to access the space in a easy and affordable way.
Thus the concept of modularity in all part of our design has to be the *leit motif*. Modularity means a set of redundant functions and resources that can be configured and used when needed (both during the pre-launch phase and at run-time). Many of these features have to be changed easily, thus using a configuration memory is the straightforward choice. The number of available selections is pretty limited (i.e., can vary from 10 to hundred in the projects we have foreseen), but they have to be maintained for all the satellite life. For this reasons FeRAM devices are the most suitable to this goal.

7.6.2 Operational conditions

The target environment for our design is again the low-earth orbit, a zone between the 500 km and the 800 km above the sea level. The environment is the same of the PiCPoT satellite we described above, thus the related constraints are the same.

7.6.3 OBC-tile architecture

The OBC-tile architecture is shown in Fig. 6. It is based on a hot redundancy structure relying on FPGAs and CPUs. This OBC relies on the presence of an MSP430 (TI (2010)) microcontroller and an Actel FPGA A3P125. The former is used for handling basic operation of the tile, like the communication through the control bus, sensors acquisition, JTAG interface... The latter is aimed at performing all the *data crunching* related to the image elaboration and the high speed communication with the payload and the radio subsystem.
In order to save power the FPGA is switched on only when needed and the MSP430 is enrolled to manage the power cycling of this device.
Since this module has to be able to work in different cases (e.g., different power cycles, different hardware configurations, different payloads, ...) we need to keep trace of all these choices somewhere. Obviously a memory is a good place to keep it, but due to our power constraints, we need to shut the memory down when it is not accessed. Thus the usage of a non-volatile technology is mandatory and, how we exposed before for the PiCPoT case, FeRAMs is the best choice.
In our case we use multiple smaller chips, even if greater ones are commercially available, for reliability reasons, since in case of physical damages we can have multiple places where to save our configuration data. Moreover having multiple chips allows us to save more energy since we power only the device needed, and not all the memory we have on board.

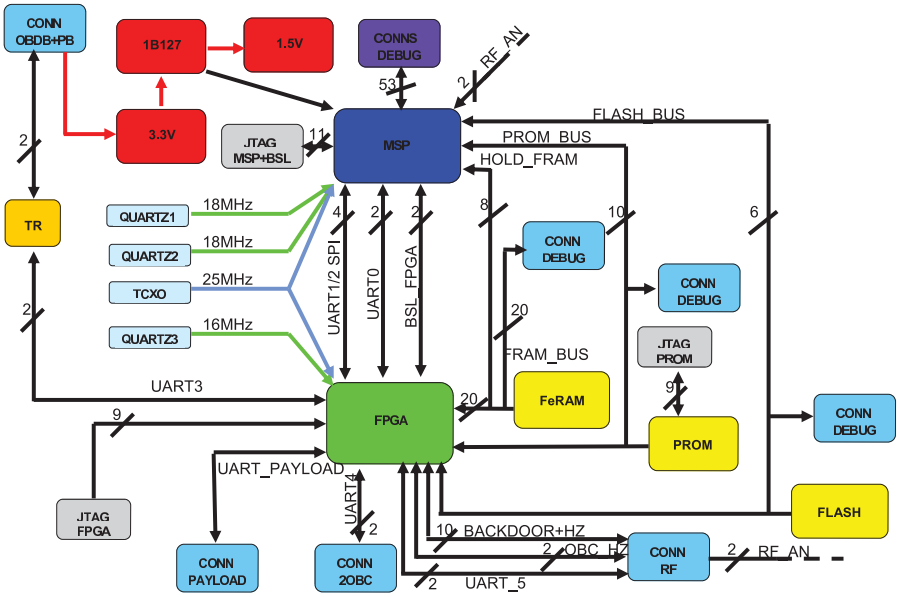

Fig. 6. AraMiS OBC architecture

8. Conclusions

This chapter has shown how commercial-off-the-shelf FeRAM devices can be a good solution for spacecrafts. Indeed we described how the FeRAM memory cell is far less sensitive to the issues we can have in space (i.e., heavy ions and total ionizing dose). Moreover its intrinsic low power consumption allow the devices to be very well suited for battery-based devices and those applications where heat dissipation is difficult.

After this introduction two real designs have been presented, where the usage of FeRAM memories has produced a set of non negligible improvements. Further investigations are ongoing and we plan to use again these devices in our future projects, in order to make our designs safer and more reliable.

Unfortunately we did not collect data from the PiCPoT experiment, since it blew up during the launch due to a failure of the launcher. But the new project will provide us a lot of information from the real application field allowing us to increase our expertise in using these kind of devices in the space and will allow our future designs to be more reliable, robust, and efficient.

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