Self-reported gait unsteadiness in mildly impaired neurological patients: an objective assessment through statistical gait analysis

Designing and Modeling for Power Integrity

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(Invited Paper)

***Abstract*—After providing an overview of the state-of-the-art in power distribution design and modeling, this paper focuses on return path discontinuities (RPDs) for I/O signaling. After briefly describing their importance in the context of simultaneous switching noise, a specific case of RPD based on via discontinuities is discussed in detail in the context of both the frequency- and time-domain waveforms using a test vehicle. The modeling of RPD in practical packages and printed circuit boards is addressed along with substrate coupling due to nonideal reference planes. Finally, a high-impedance power distribution scheme for I/O signaling is presented that can potentially solve a number of RPD-related problems, followed by future challenges.**

***Index Terms*—Macro-modeling, passivity, power distribution, power integrity, return path discontinuity, signal integrity.**

I. Introduction

POWER distribution continues to be a major challenge in electronic systems. With the trend toward system miniaturization, leading to increased reliability, higher performance, and lower cost, power distribution continues to be an important area that is beginning to limit scaling. Though power distribution is often attributed to the noise on the power supply, its effect can be monumental in dictating the signal integrity of a waveform. Therefore, in present and future electronic systems, maintaining signal integrity requires designing the system for power integrity. Unfortunately, the relationship between signal and power integrity is not straightforward and this often leads to increased design cycle time, due to several design respins required.

Power distribution represents the supply of voltage and current to the switching circuits. The voltage regulator module (VRM) consisting of a switching regulator circuit, supplies current to the transistors on the chip while simultaneously managing the ripple across the power supply. The interconnections in the power distribution (strips, planes, bonding wires, C4 bumps, etc.) serve as a conduit for the current to flow from the VRM to the transistors. Since VRMs switch at kilohertz frequencies as compared to modern day chips, which switch at multi-gigahertz frequencies, the VRMs are unable to respond to the transient current surges. In addition, the physical separation between the VRM and the chip increases the time delay for the charge to reach the switching circuits within the available time window. Due to the finite inductance of the interconnections, the difficulty of the VRM to respond quickly to current surges leads to a loss in voltage regulation, causing the voltage at the transistor terminals to vary wildly with time. Since transistors operate well within an allowed ripple around the dc level of the power supply, a voltage surge above the maximum voltage will limit chip reliability, while a voltage droop below the minimum voltage can lead to reduced operating frequency [1]. Both these effects are detrimental to system operation, and therefore, alternate means for supplying clean power at higher frequencies is required. This is possible by using capacitors that serve as a reservoir of charge, supplying current to the chip during the switching cycles and recharging during the remaining cycles. The proximity of the capacitor to the chip and its parasitics (equivalent series resistance and inductance) determine the speed at which the capacitors react to the change in current, leading to a reduced droop or peak in supply voltage, if done correctly.

In the late 1990s, the use of target impedance as a parameter for designing the power distribution network (PDN) was proposed [2]. It was based on the premise that the resistive, inductive, and capacitive behavior of the PDN can be captured through its impedance characteristics and the target impedance can be used as a parameter to control power supply noise. A frequency-domain methodology emerged using target impedance as the design parameter, which completely changed the design methodology for PDNs. Using the target impedance, system components, such as VRMs, capacitors, and chips could be designed individually and their interaction could be assessed by concatenating them together. Detailed procedures for designing the power distribution components are described in [3], along with their effect on the PDN in the frequency domain.

A chip consists of two basic circuit types, namely, core circuits, where the communication between the transistors is contained within a single chip and the I/O circuits, where the communication is between transistors on separate chips, as shown in Fig. 1. Both transistor level circuits require power, which is supplied by the VRMs on the printed circuit board (PCB). For the design of the core PDN, the target impedance parameter has been used by several authors over many years [4]–[6]. These papers cover a diverse range of issues related to core power distribution, which include the modeling and measurement of VRMs, power and ground planes, decoupling capacitors, vias,

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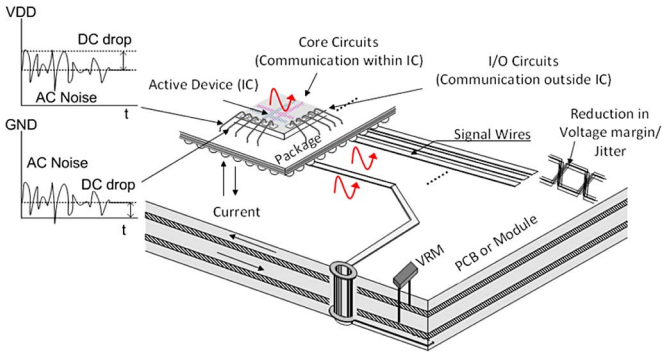


Fig. 1. Core and I/O circuits.

and other interconnect structures. Several advanced computational techniques have also been developed that allow for the automated placement of decoupling capacitors to maintain the target impedance at several chip locations [7]. However, in comparison to the core power distribution, little work has been published on the design of I/O PDNs. The difference between the core and I/O power distribution lies in the behavior of the signal lines as transmission lines (due to their electrical length), causing return current to flow on the reference planes in the package and PCB. The presence of discontinuities in the return current path often leads to noise on the PDN, which can lead to increased insertion loss on the signal lines, coupling between voltage islands, substrate coupling between I/Os and in a common PDN, coupling between the core and I/O circuits. The signature of the noise waveform is a function of the spectrum of the excitation signal; therefore, their impact can be quite different for a clock signal as compared to a pseudorandom bit stream (PRBS). Just like the core power distribution, a low-impedance PDN is required for the I/Os as well, to minimize noise. This is possible by using capacitors, where their value and placement is a function of the signal spectrum and return path discontinuities (RPDs). With the trend toward wide busses and fast signaling speeds in multicore and graphics intensive applications, it is expected that the contribution of power supply noise to simultaneous switching noise (SSN) for I/Os can become very large, causing excessive jitter and reduction in the voltage margin.

Power supply noise has two components, namely, the dc drop caused by the finite conductivity of the interconnections carrying the current, and ac or transient noise caused by the dynamic behavior of the transistors, as shown in Fig. 1. Both effects can increase jitter and reduce the eye opening.

On the computational side, some paper has been published for modeling signal lines in the presence of PDNs that account for the return currents on the reference planes [2] and [8]–[10]. Most of these methods are discussed in detail in [11]. All of these methods are based on the premise that the signal distribution network and PDN can be analyzed separately, and then, concatenated together to be able to capture the interaction between the signal lines, and power and ground planes. One of these methods, which is based on modal decomposition, enables the frequency response of the transmission lines and power/ground planes to be computed separately, which are then connected together using a transformation matrix consisting of coupled

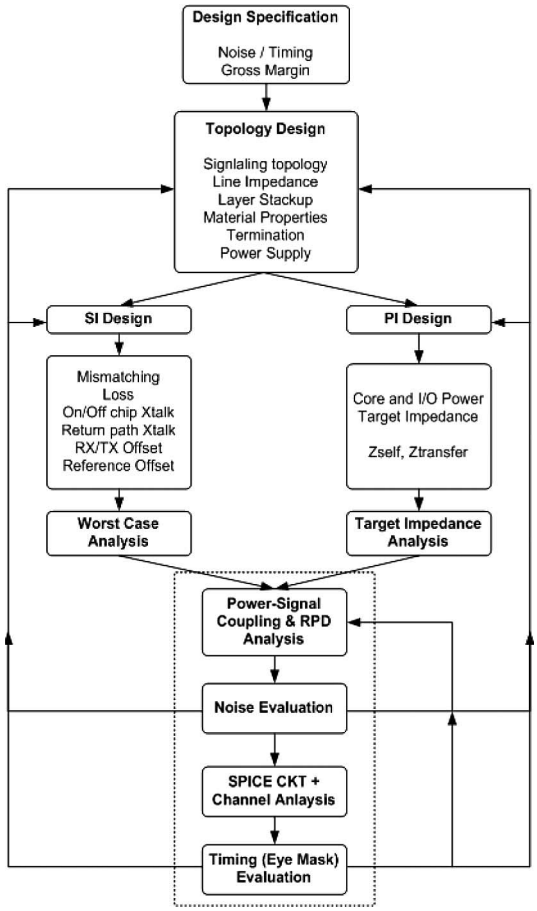


Fig. 2. Design flow.

voltage and current sources [11]. The coupling factor for the voltage and current sources can be analytically derived based on the physical dimensions of some interconnection structures in homogeneous media, such as microstrip line and stripline, while for other structures, such as the coplanar line, they can be computed using a 2-D solver. These methods have also been extended to inhomogeneous media [12].

A possible design flow for maintaining signal and power integrity for I/O circuits is shown in Fig. 2. Based on the design specifications related to timing and noise margin, the layer stack up is defined along with the ground rules, layer assignments, signal topology, and termination schemes. The design is then separated into two parts, namely, signal integrity and power integrity design. For managing signal integrity, reflections, ringing, crosstalk, and other effects related to the signal line are assessed along with a worst-case analysis to ensure suitable waveforms. In this analysis, the PDN consisting of voltage and ground planes is assumed to be ideal, with infinite capacitance between them. In parallel, the power distribution is designed using target impedance as the design parameter to maintain the noise low on the PDN. This is followed by an analysis of the signal lines in the presence of the nonideal reference planes to capture effects related to RPDs and other variations on the PDN. This analysis captures the effect of power supply variations on SSN in addition to crosstalk and reflections to ensure adequate noise margins prior to channel analysis. The channel analysis

involves the estimation of the voltage and timing margins of the design, prior to tape out. The focus of this paper is on part of the design flow indicated by a dashed line in Fig. 2, where the RPDs can affect the quality of the signal waveforms. In Fig. 2, assuming the noise margin is not met, the RPDs can be fixed either by placing decoupling capacitors on the PDN or by other means, such as changing the stack up or the layer assignments.

This paper is organized as follows: After a discussion on the source of RPDs and their effect on time-domain waveforms in Section II, this paper establishes a relationship between the PDN impedance and the signal insertion loss in the frequency domain, and their effect on eye diagrams in the time domain, in Section III. In Section IV, modeling methods are discussed for combined analysis of the signal distribution network and PDN in the frequency and time domain. Modeling results for an industrial PCB are presented in this section. A modeling flow is provided that enables the computation of the frequency response of signal lines in the presence of PDNs, which can then be converted into a simulation program with integrated circuit emphasis (SPICE) subcircuit for time-domain simulation. Substrate coupling between signal lines and coupling between core and I/O are covered in this section. As systems become more complex and as 3-D integration of ICs becomes more prevalent, the effect of RPDs on SSN will become even larger. Some new concepts are discussed in Section V for delivering clean power to such systems along with new challenges that need to be addressed in Section VI, followed by conclusion in Section VII.

II. Return Path Discontinuities

A transmission line carrying a signal will always generate a current on the signal line and the reference plane. These currents are equal and opposite to each other. The forward and return currents will always flow in close proximity to each other and will follow the path of least impedance. Since the transmission line supports a 1-D wave between the signal conductor and reference plane, the forward and return currents are balanced and occur simultaneously. This is in contrast to the loop current, which is dictated by the boundary conditions associated with the driver and receiver circuitry, causing the currents on the signal line and reference plane to connect to each other. Any interruption of the return current or the loop current can cause RPDs, resulting in the degradation of the signal waveform. The presence of RPDs can also cause noise coupling between signal lines far apart that share a common PDN. The noise resulting from RPDs is referred to as SSN in this paper. In this section, the effect of layout and termination on RPDs is discussed briefly.

A. Effect of Layout on RPD

Fig. 3 shows four examples of a microstrip line in the presence of voltage (VDD) and ground (VSS) planes. In Fig. 3(a), a microstrip-to-microstrip transition causes a change in the reference plane, thereby creating an RPD along the return current path in the vicinity of the via. This leads to a buildup of voltage $V_{\rm SSN}$ between the VDD and VSS plane, generating noise in the PDN and degrading the signal waveform. In Fig. 3(b), a split in the VSS plane causes an interruption in the return current,

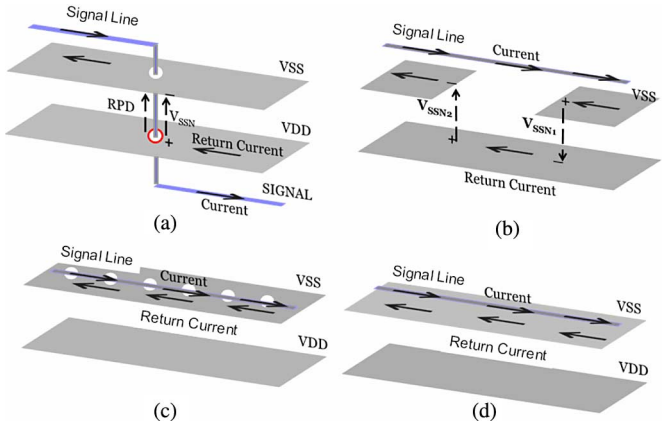


Fig. 3. Layout discontinuities. (a) Microstrip-to-microstrip transition. (b) Microstrip line crossing split plane. (c) Microstrip line above apertures. (d) Microstrip line referenced to top plane.

leading to voltage buildup $V_{\rm SSN1}$ and $V_{\rm SSN2}$ between the two planes on either side of the split, once again leading to PDN noise and deterioration of the signal waveform. In Fig. 3(c), the apertures (holes) on the VSS plane interrupt the flow of return current causing it to flow around the apertures, leading to RPDs. In all of these cases, the RPD is caused due to a defect in the layout and can be fixed by modifying the layout. However, in Fig. 3(d), the return current is continuous on the VSS plane with no apparent RPDs. In such cases, the RPDs are dictated by the loop current flowing through the driver, signal line, and termination circuitry, which can only be fixed either by changing the stack up (in the package and PCB) or by changing the termination conditions. Hence, in estimating SSN, both the electromagnetic effect of the layout and the effect of termination circuitry are equally important, requiring a design methodology that combines electromagnetic and circuit simulation techniques. It is important to note that the RPDs shown in Fig. 3 can also occur in other interconnection structures, such as striplines and coplanar lines. The location of the RPDs can be found by following the return current.

B. Effect of Terminations on RPD

To better illustrate the importance of driver and termination circuitry, consider Fig. 3(d), which has an absence of RPDs, since the signal line is referenced to a continuous VSS plane. This is reproduced in Fig. 4 along with the driver and termination circuitry, with the microstrip line referenced to a solid VDD plane. In Fig. 4, $R_{\rm ON1}$ and $R_{\rm ON2}$ represent the ON-resistance of the PMOS and NMOS transistors in the driver, the reference planes are 1-D (narrow width and 20 in long) and is the same length as the microstrip line. A power supply of 5 V is connected between the VDD and VSS plane at the far end of the driver. The signal line is assumed to have an impedance of 20 Ω and is loss free. The only difference between Fig. 4(a) and (b) is that the microstrip line is unterminated at the far end in Fig. 4(a), while the microstrip line is matched with two resistors in parallel (one connected to VDD and the other to VSS), each with a resistance of 40 Ω in Fig. 4(b). The driver switches from low to high in both cases.

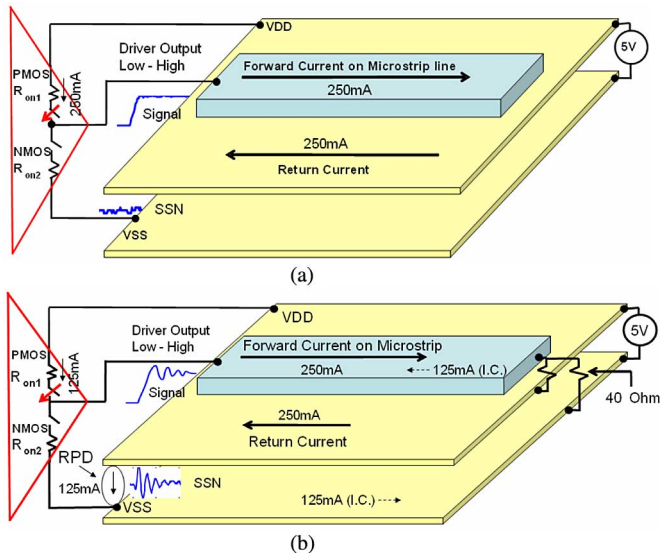


Fig. 4. Microstrip line. (a) Unterminated (no RPD). (b) Terminated showing RPD.

The currents on the microstrip line, VDD and VSS planes soon after switching from low to high is shown in Fig. 4. These currents assume that the ON-resistance of the driver is zero ohms. In Fig. 4(a), since the microstrip line is open circuited, there is zero current on the microstrip line, VDD and VSS planes, prior to switching from low to high. When the PMOS switch closes and the NMOS switch opens, the microstrip line begins to charge to 5 V, causing a forward going wave between the microstrip line and VDD plane. The 250 mA forward and return currents (5 V/20 Ω, where 20 Ω is the signal-line impedance) are connected together through the PMOS driver and are continuous, thereby causing no RPDs in the current flow. Therefore, there is no current flowing directly from VDD to VSS between the voltage and ground planes. An oscilloscope used to measure the SSN between VDD and VSS in the vicinity of the driver will show zero time-varying voltage. Hence, the signal integrity of the waveform will be affected only by the reflected signal at the far end of the microstrip line and not by the power distribution planes. The measured signal waveforms at the output of the driver and the SSN between VDD and VSS nodes of the driver are shown in Fig. 4(a), demonstrating zero SSN.

In contrast, Fig. 4(b) can produce SSN voltage between the VDD and VSS nodes of the driver due to the termination at the far end. Prior to switching states from low to high, the driver is in its low state and due to the presence of the termination resistors, a steady current of 125 mA (5 V/40 Ω, where 40 Ω is the termination resistance) flows in the circuit between the microstrip line and VSS plane. These currents are shown as initial conditions in Fig. 4(b). When the driver switches from low to high, the PMOS switch closes, while the NMOS switch opens, causing the charging of the microstrip line, leading to a forward traveling wave of voltage amplitude 5 V and current amplitude 250 mA on the transmission line. The forward current on the microstrip line and return current on the VDD plane are shown in Fig. 4(b), which are superimposed on the 125 mA current in the circuit prior to changing states, causing a net current of 125 mA. The 125 mA current used to charge the microstrip line is supplied by the VDD plane. The remaining 125 mA of current on the VDD plane jumps directly to the VSS plane, causing an RPD in the vicinity of the driver and leading to SSN voltage that can have a large effect on the signal integrity of the waveform. The amplitude of the SSN voltage is a function of the impedance between the VDD and VSS planes. The measured signal waveform at the output of the driver and SSN between the VDD and VSS nodes of the driver is shown in Fig. 4(b), indicating the effect of SSN on the signal waveforms in spite of the matching at the far end. Details on the test vehicle used to quantify these effects are described in detail in [11].

Based on this section, both the layout and the terminations can have a large effect on SSN generated in the PDN. The SSN in both these cases are caused due to discontinuities in the return current. In the next section, the effect of RPDs caused by via transitions, which is the most common discontinuity, is quantified in the time and frequency domain. After establishing a relationship between the PDN impedance and signal line insertion loss, the effect of RPDs on eye diagrams is analyzed both for clock signals and PRBS.

III. Via Discontinuities

Via discontinuities can cause RPDs due to a change in the reference plane of the signal line due to via transitions. An interconnect path with via discontinuity can induce SSN in the power delivery network. The SSN is proportional to the PDN impedance at the via discontinuity. Since the PDN impedance is a function of frequency, the magnitude of SSN induced in the PDN depends on the frequency of the signal propagating through the interconnection. Since digital signals are comprised of multiple frequencies with significant energy content at harmonic frequencies, the SSN induced noise and jitter on the signal depends both on the PDN impedance and the harmonic content of the signal. The behavior of a signal through an interconnection can be quantified by understanding the network parameters of the interconnection and the harmonic content of the signal. The resulting jitter and noise on the signal can be estimated by: 1) determining the impact of PDN impedance at the RPD on the insertion loss of the signal and 2) determining the impact of signal insertion loss and coupling on the jitter and noise level of the signal. These effects are quantified in this section using a test vehicle.

A test vehicle was designed and fabricated to observe the impact of PDN impedance on the insertion loss of the signal and its effect on voltage amplitude and jitter. The test vehicle consists of four metal layers with microstrip line on the top and bottom layers and ground and voltage planes on the second and third layer, respectively, fabricated as a PCB. The test vehicle contains two via transitions with each transition causing a RPD at the via location, as shown in Fig. 5. Capacitor pads were provided near each via transition, so that suitable capacitors can be soldered to reduce the PDN impedance at the RPD, to evaluate its effect on the signal waveform. The capacitors had $C = 4700$ pF, ESL $= 0.3$ nH, and ESR $= 0.25$ Ω, where ESL

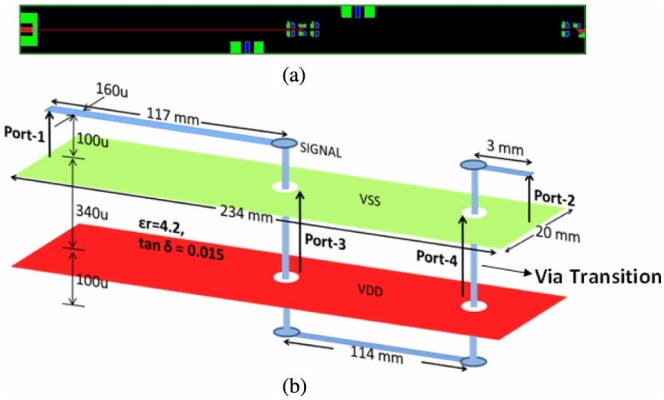


Fig. 5. Test vehicle. (a) Schematic of top view (b) Dimensions and port placement.

and ESR are the equivalent series inductance and resistance, respectively. Details of the test vehicle with dimensions and port placement are provided in Fig. 5 [7].

A. Impact of PDN Impedance on Signal Insertion Loss

As mentioned earlier, the return current on the planes induces SSN between the power and ground planes at the via discontinuity. The SSN voltage is equal to the product of the return current and the PDN impedance at the discontinuity. As the PDN impedance is a function of frequency, the SSN voltage also depends on the frequency of the return current. At the antiresonance frequency of the PDN, the impedance increases, resulting in a large SSN voltage being induced between the planes. A large value of SSN signifies large coupling between the signal line and the PDN, which results in smaller amount of energy propagating through the signal line from port 1 to port 2, in Fig. 5. This manifests itself as an increase in the insertion loss of the signal, which can be measured using a vector network analyzer (VNA). This effect has been captured in this section using the test vehicle. It is important to note that the reference for ports 1 and 2 is the VSS plane in Fig. 5.

The measured PDN impedance at ports 3 and 4 for the test vehicle with and without decoupling capacitors is shown in Fig. 6. In Fig. 6, the measurement ports 3 and 4 are placed in the vicinity of the RPD, and hence, represent the plane impedance at the discontinuity. The difference in the position of the ports reflects in the frequency of the antiresonance, resulting in more antiresonances in Fig. 6(b) as compared to Fig. 6(a). The combined effect of both of these antiresonances reduces the insertion loss of the signal line, as shown in Fig. 7, where the increase in the insertion loss coincides with the frequency of antiresonance between the voltage and ground planes. The placement of the capacitor at the RPD reduces the plane impedance in Fig. 6, which reflects in an improved insertion loss on the signal line, as shown in Fig. 7.

Clearly, there is a strong relationship between the PDN impedance at an antiresonance frequency and the corresponding insertion loss of the signal at the same frequency. This interaction occurs due to the RPD. Elimination of the RPD requires a continuous return path, which can be accomplished by using

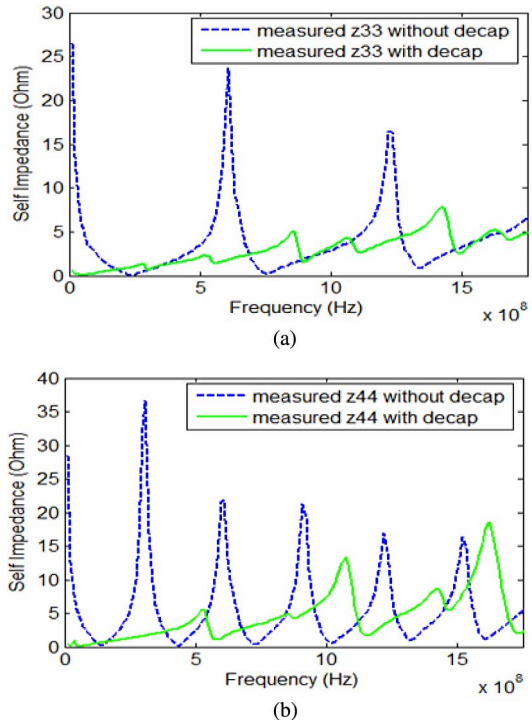


Fig. 6. Comparison of measured PDN impedance of TV with and without decoupling capacitor at (a) port 3 and (b) port 4.

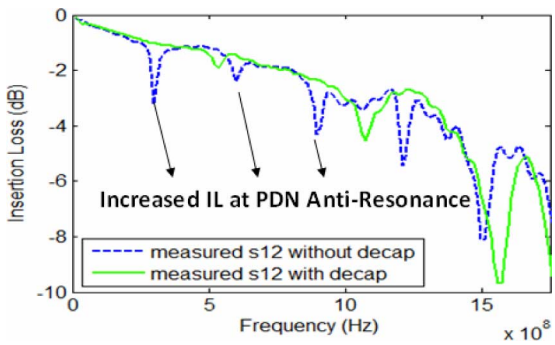


Fig. 7. Comparison of measured insertion loss between port 1 and port 2 with and without decoupling capacitor.

decoupling capacitors at the RPD location. Since decoupling capacitors are nonideal, the goal is to ensure that the impedance of the decoupling capacitor is less than the PDN impedance at the antiresonance frequency. The smallest impedance can be achieved by selecting a capacitor that resonates at the antiresonance frequency of the PDN, resulting in the smallest insertion loss of the signal at this frequency.

B. Impact of Insertion Loss and PDN Impedance on Jitter and Amplitude of Clock Signal

The frequency spectrum of a clock signal consists of the fundamental and harmonics at odd multiples of the clock frequency. Therefore, a significant amount of energy of the clock signal is stored at these frequencies. For example, a 600 MHz clock has significant harmonic components present at 600 MHz, 1800 MHz, etc., as shown in Fig. 8. If the harmonics of the clock

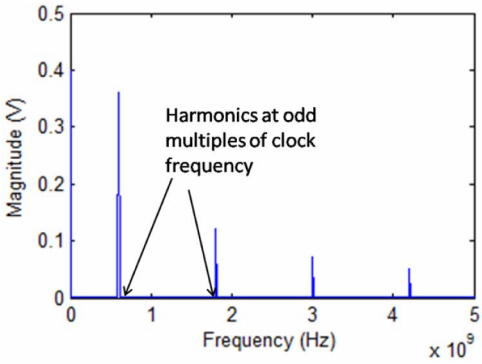
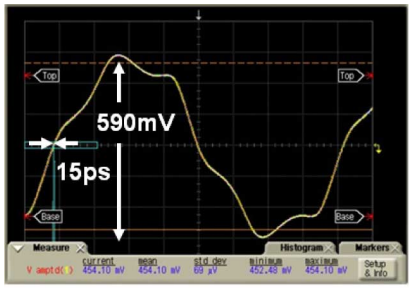
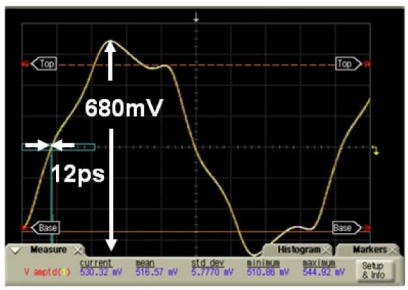


Fig. 8. Spectrum of 0.8 V 600 MHz clock signal.



(a)



(b)

Fig. 9. Comparison of 600 MHz clock waveforms at port 2 (a) without decaps and (b) with decaps.

coincide with the frequencies at which the signal line insertion loss is large, they undergo a large attenuation causing reduction in the amplitude and increase in rise/fall time of the clock signal.

However, since the clock signal is periodic, the increased insertion loss on the signal line at the PDN antiresonance frequencies does not increase jitter of the clock signal. Hence, the RPD's effect is a reduction in the voltage amplitude with little impact on the jitter of the clock signal. This effect has been illustrated in this section using a 0.8 V, 600-MHz clock signal, propagated from port 1 to port 2 on the microstrip line in the test vehicle, so that its fundamental frequency coincides with the increased insertion loss at 600 MHz, as shown in Fig. 7. The attenuation of the fundamental clock frequency due to the insertion loss causes a reduction in the amplitude of the clock signal with amplitude of 590 mV, as shown in Fig. 9(a). With the addition of the decoupling capacitor at the RPD, the insertion loss of the signal line improves, resulting in an increase in the clock amplitude to 680 mV, as shown in Fig. 9(b). However, the

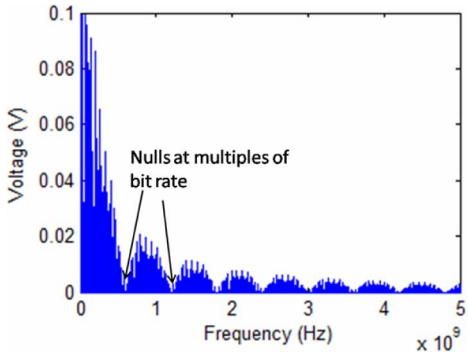


Fig. 10. Spectrum of 0.8 V, 600 Mb/s PRBS signal.

improvement in jitter is insignificant from 15 to 12 ps, which can be attributed to the source waveform uncertainty rather than the signal line insertion loss, since the energy content of the clock signal is concentrated at specific frequencies.

C. Impact of Insertion Loss on Jitter and Noise of PRBS Signal

The frequency spectrum of a PRBS consists of harmonics distributed across multiple frequencies based on the data pattern. The envelope of the spectrum is a "sinc squared" function with nulls at multiples of the bit rate of the PRBS. As an example, the spectrum of a 600 Mb/s PRBS consists of nulls at multiples of 600 MHz and has significant harmonic content at 900 MHz, 1500 MHz, etc., as shown in Fig. 10. If significant harmonics of the PRBS signal coincide with large insertion loss peaks of the signal line, as shown in Fig. 7, they undergo large attenuation reducing the amplitude of the PRBS pulses and increasing their rise/fall times.

However, since most of the energy of the PRBS signal is distributed across multiple frequencies, attenuation at a few discrete frequencies does not cause a large reduction in the amplitude of the PRBS signal. On the other hand, randomness of data pattern and hence the switching sequence changes the SSN induced in the PDN, leading to changing rise/fall time of the signal and uncertainty in the timing of the signal edge. This effect manifests itself as increased jitter on the PRBS signal. To illustrate this effect, a 600-Mb/s PRBS signal was applied to the test vehicle at port 1 with a measurement of the received signal at port 2. A comparison of the eye diagram obtained at port 2 with and without decoupling capacitors is shown in Fig. 11. The addition of the decoupling capacitor reduces the PDN impedance, thereby improving the signal insertion loss, as shown in Fig. 7. Hence, the eye diagram with decoupling capacitors shows an eye height of 475 mV as compared to 400 mV with the decoupling capacitor removed; a result, which is smaller than the improvement of the clock signal in Fig. 9. However, the addition of the decoupling capacitor improves the jitter significantly from 93 to 76 ps, a large effect, which was absent with the clock signal.

In conclusion, the RPDs in the layout generate SSN, which affects the signal amplitude and jitter depending on the nature of the signal being transmitted. This effect needs to be first quantified in the frequency domain by looking at the relationship

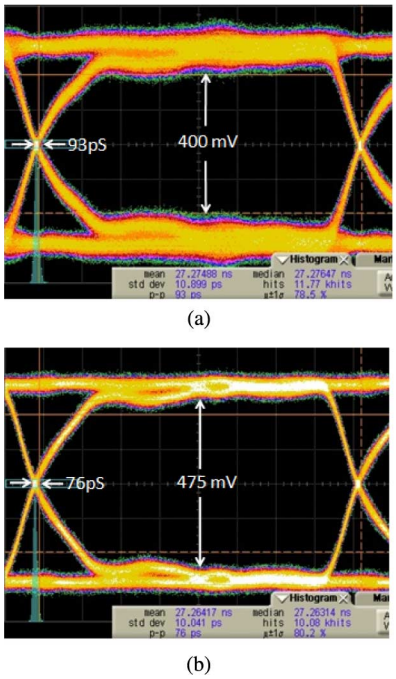


Fig. 11. Measured eye diagram at port 2 (a) without decoupling capacitors and (b) with decoupling capacitors.

between the PDN impedance and signal insertion loss. After applying suitable design methods on the PDN, such as removing RPDs or adding decoupling capacitors at appropriate locations to improve the insertion loss of the signal, the effect of the design change on the time-domain response has to be evaluated both for a periodic clock signal and a PRBS. The time-domain response can change in the presence of nonlinear drivers and terminations, which needs to be evaluated as well. For a complex package or PCB, modeling and simulation methods are required to evaluate these effects, which is the subject of the next section.

IV. Modeling

Supporting a design flow requires extensive and repeated analysis. Any modeling approach that supports analysis has to be accurate, computationally fast, and should enable fast design closure. In the case of PDNs, this can be challenging, since they are electrically large. The complexity is magnified when the signals have to be analyzed in the presence of the PDN to account for the effects of RPDs. Since interconnections far apart can couple energy through the substrate during an SSN event, the PDN cannot be cut into smaller regions around the signal lines for modeling. Hence, a scheme needs to be devised that models the electromagnetic effects pertinent to SSN on the entire layout of the package and PCB. Both a frequency- and time-domain technique is required to capture the interconnection loss, antiresonances, substrate coupling, and nonlinearity of the driver. Focusing on frequency-domain analysis enables the identification of potential discontinuities in the layout, while time-domain analysis captures the effect of driver and receiver circuits on SSN, thereby ensuring accuracy and confidence in the computed eye diagrams while estimating timing and voltage

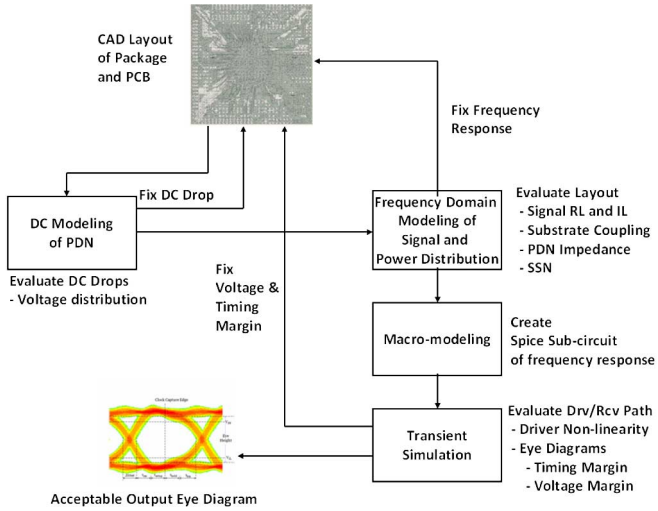


Fig. 12. Modeling flow.

margins. A possible modeling flow is shown in Fig. 12, where the layout is first analyzed for dc drops to ensure that the drivers have the appropriate voltage level prior to frequency-domain analysis. The frequency-domain analysis consists of modeling the package and PCB layout consisting of the signal lines and PDN simultaneously, to detect frequencies and regions of the layout, where the insertion loss, PDN impedance, or coupling due to SSN is problematic. The frequency response is then converted to a SPICE subcircuit for simulation with the driver, receiver, and other termination circuits to compute eye diagrams and evaluate the timing and voltage margins. Needless to say, every step in Fig. 12 has a feedback loop, where the design is optimized to mitigate any problems with the design. In general, the number of iterations in the feedback loop is much higher for dc and frequency-domain modeling as compared to time-domain analysis. This is partly because of the need for design fixes in the layout and also due to the simulation complexity involved in the time domain as compared to frequency domain. In Fig. 12, both dc and frequency-domain modeling require electromagnetic analysis, while time-domain analysis is done using circuit simulators.

The electromagnetic modeling of a layout is possible by either using differential or integral equation-based solvers. Though each has its own advantages and disadvantages, the differential equation-based solvers have been more popular for analyzing power-integrity-related problems. This can be attributed to the formulation, leading to a sparse matrix that can be solved efficiently, and to the ease of implementation. Such solvers are capable of analyzing large and complex layouts on a 32-bit laptop in a relatively short time. Two types of differential equation-based solvers, namely, the multilayered finite-difference method (M-FDM) and multilayered finite-element method (M-FEM) are discussed in this section.

Macromodeling approaches have evolved in the past five years, where issues related to passivity and causality have been solved, resulting in the ability to approximate frequency responses of signal lines in the presence of PDN over broad

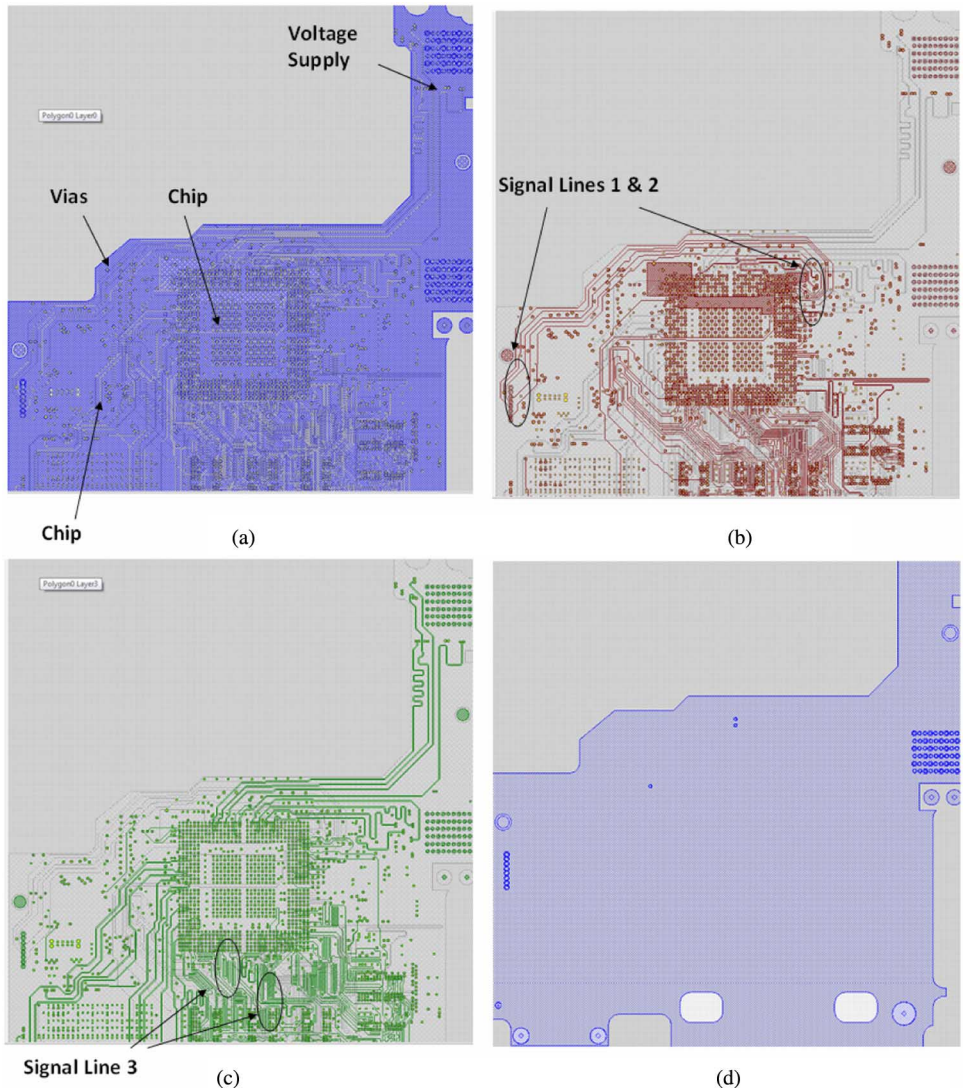


Fig. 13. (a) Metal M_1 voltage plane. (b) Metal M_2 signal layer. (c) Metal M_3 signal layer. (d) Metal M_4 ground plane.

frequency ranges without comprising accuracy or having any limitations on the number of I/O terminals. As a result, the effect of power distribution on signal integrity can be assessed in the presence of nonlinear drivers, using a circuit simulator, such as SPICE.

In this section, details on dc modeling, frequency-domain modeling, and macromodeling are discussed, and applied to a complex layout for assessing the effect of RPDs on signal waveforms, in both the frequency and time domain.

A four layer PCB example of size 6.2 in $\times$ 4.85 in, as shown in Fig. 13 has been used in this section to demonstrate the use of modeling for estimating dc drops, insertion loss, substrate coupling, and eye diagrams. The PCB consists of a voltage plane (M_1), signal layers (M_2 and M_3), and a ground plane (M_4). Metal layers M_1, M_2, and M_3 have a thickness of 0.7 mil with the thickness for M_4 being 1.2 mils. All the metal layers were fabricated using copper with a conductivity of 5.9×10^7 S/m. The dielectric material used was FR-4 with a relative permittivity and loss tangent of 3.7 and 0.035, respectively. The dielectric thickness used was 2.8, 6, and 3.6 mils between metal layers M_1–M_2, M_2–M_3, and M_3–M_4, respectively. The linewidth used for the signal lines was 5 mils, resulting in a characteristic impedance of approximately 50 Ω.

A. DC Modeling

The purpose of dc modeling is to compute voltage drops in a package or PCB in the presence of voltage supply (battery) and current sources (chip). At dc, the current flowing through a conductor is defined using Ohm's law in the form

$$\vec{J} = \sigma \vec{E} \tag{1}$$

where $\vec{J}$ is the current density and σ is the electrical conductivity of the conductor, respectively. From the equation of continuity of electric charge

$$\nabla \cdot \vec{J} = 0. \tag{2}$$

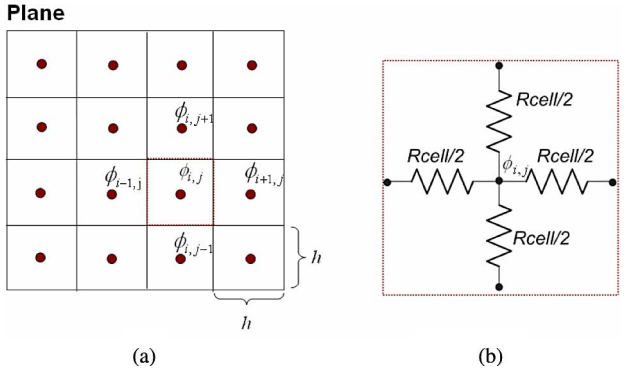


Fig. 14. (a) Finite-difference discretization of the plane. (b) Cell equivalent circuit model.

Since the electric field $\vec{E}$ can be expressed as a function of electric potential ϕ as follows:

$$\vec{E} = -\nabla\phi. \tag{3}$$

Equations (1)–(3) can be combined, leading to Laplace's equation in the form

$$-\sigma(\nabla^2\phi) = 0. \tag{4}$$

By solving (4) in the presence of boundary conditions

$\phi|_{\Gamma_1} = V_{\text{input}}$, where Γ_1 represents the voltage supply nodes,

$\dfrac{\partial\phi}{\partial n}|_{\Gamma_2} = I_{\text{output}}$, where Γ_2 represents the current source nodes, and

$\dfrac{\partial\phi}{\partial n}|_{\Gamma_2'} = 0$, where Γ_2' are all the other boundaries in the structure (5)

the voltage distribution of the PDN can be computed.

The FDM can be employed for discretizing Laplace's equation on the power and ground planes of the PDN subject to the boundary conditions described in (5). Since the thickness of the plane "t" is much smaller than its lateral dimensions, it can be assumed that the electric field and potential gradient do not vary along the vertical (z) direction. Hence, $\partial\phi/\partial z = 0$ and the governing equation for voltage distribution reduces to the 2-D scalar Laplace's equation in the form

$$-\sigma_s\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right)\phi = 0 \tag{6}$$

where $\sigma_s = t\sigma$ is the sheet conductivity of the conductor. By applying the FDM on a uniform square mesh, the 2-D Laplace's equation can be approximated as follows:

$$t\sigma\frac{\phi_{i,j-1} + \phi_{i,j+1} + \phi_{i-1,j} + \phi_{i+1,j} - 4\phi_{i,j}}{h^2} = 0 \tag{7}$$

where the discretization error is of $O(h^2)$. In (7), "h" is the cell size and $\phi_{i,j}$ is the voltage at node (i,j), as shown in Fig. 14(a).

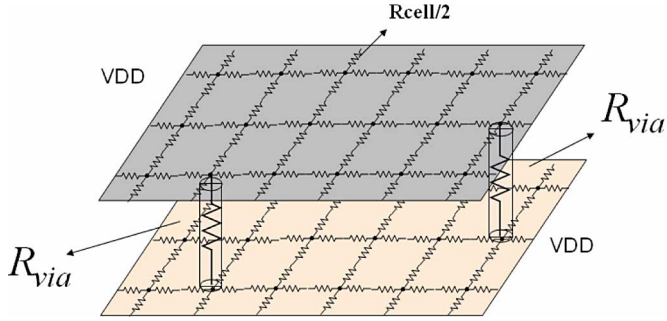


Fig. 15. Equivalent resistor network for two planes together with vias.

Equation (7) can be converted to the form as follows:

$$\frac{\phi_{i,j-1} - \phi_{i,j}}{R_{\text{cell}}} + \frac{\phi_{i,j+1} - \phi_{i,j}}{R_{\text{cell}}} + \frac{\phi_{i-1,j} - \phi_{i,j}}{R_{\text{cell}}} + \frac{\phi_{i+1,j} - \phi_{i,j}}{R_{\text{cell}}} = 0 \tag{8}$$

where

$$R_{\text{cell}} = \frac{1}{t\sigma}. \tag{9}$$

Based on (8), the dc equivalent circuit model for cell (i,j) can be represented, as shown in Fig. 14(b). The dc model for representing the plane can be obtained by connecting the dc circuit model for each cell to each other at the nodes of the equivalent circuit.

In a multilayered power delivery network, the planes are shorted together through vias. To reduce the number of unknowns in the equivalent resistance network, the vias can be modeled as a single resistor connected between the corresponding nodes of the planes. The via resistance can be expressed as follows:

$$R_{\text{via}} = \frac{l}{\sigma\pi r^2} \tag{10}$$

where "r" is the radius of a circular via and "l" is the length of the via. Fig. 15 shows the equivalent resistance network for two planes shorted together using vias.

In dc modeling two kinds of ports are important, namely, 1) voltage port for the power supply, where the voltage is maintained constant and 2) current port to mimic the chip, where the current is maintained constant. The voltage and current ports are excitations in the power delivery network. The voltage port can be modeled as a Thevenin equivalent circuit, while a Norton equivalent circuit can be used to model the current port. The direction of the current can be adjusted by controlling its polarity.

After constructing the equivalent circuit network for the entire power delivery network that includes voltage and current excitations, KCL can be applied, resulting in a linear system of equations, which in matrix form can be written as follows:

$$\overline{\overline{Y}}\,\overline{\Phi} = \overline{I} \tag{11}$$

where "$\overline{\Phi}$" and "$\overline{I}$" are the node voltage and branch current, respectively and $\overline{\overline{Y}}$ is an admittance matrix. Assuming the plane

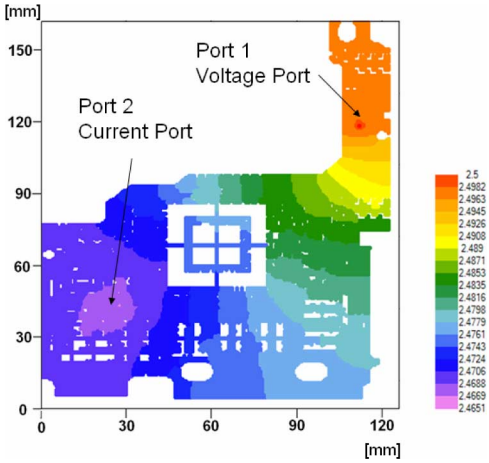


Fig. 16. PCB plane with ports and voltage distribution.

in Fig. 14(a) is discretized into $M_1 \times M_2$ square cells, the matrix $\overline{\overline{Y}}$ has dimensions $N \times N$, where $N = M_1 \times M_2$. In (11), $\overline{\overline{Y}}$ matrix has the form as follows:

$$\overline{\overline{Y}} = \begin{bmatrix} \overline{\overline{A}} & \overline{\overline{B}} & & & \\ \overline{\overline{B}} & \overline{\overline{A}} - \overline{\overline{B}} & \overline{\overline{B}} & & \\ & \overline{\overline{B}} & \ddots & \ddots & \\ & \ddots & \ddots & \overline{\overline{B}} & \\ & & \overline{\overline{B}} & \overline{\overline{A}} - \overline{\overline{B}} & \overline{\overline{B}} \\ & & & \overline{\overline{B}} & \overline{\overline{A}} \end{bmatrix} \tag{12}$$

where $\overline{\overline{A}}$ is the same form as (18) with frequency equal to zero, $Z = R_{\text{cell}}$ and $\overline{\overline{B}} = -1/\overline{\overline{Z}}$. In (12), $\overline{\overline{Y}}$ is a sparse matrix that can be solved efficiently using sparse matrix solvers. For planes with nonrectangular boundaries and containing holes, a similar procedure can be used, where the nonmetal areas can be represented by removing the resistor. In addition, a fine square mesh can be used to approximate the hole geometry.

The PCB voltage plane (M_1) in Fig. 13(a) was modeled to estimate the dc drop. As shown in Fig. 13, the plane contains via holes and other cut outs. The voltage plane was discretized with a uniform mesh of cell size 0.6 mm, resulting in 206 × 263 cells. A 2.5 V voltage port (port 1) and 10 A current port (port 2) were assigned to the plane to mimic the ideal voltage supply and the switching chip, respectively. The resulting voltage drop across the plane is shown as a contour plot in Fig. 16, where the axes represent the position along the horizontal and vertical directions in millimeter. In Fig. 16, the voltage at the current port is 2.4651 V, resulting in a voltage drop of 34.9 mV from the power supply to the chip. A chip at port 2 drawing 10 A current will have a 34.9 mV drop in the dc voltage level. It is important to note that the nodal voltages are calculated with respect to an ideal ground for dc modeling, and hence, dc voltages for a single plane can be computed. This is not possible for frequency-domain modeling, which is the subject of the next section.

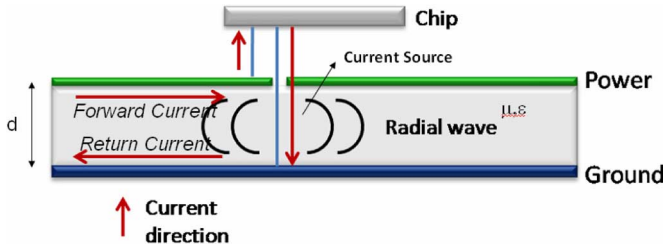


Fig. 17. Single plane pair.

B. Frequency-Domain Modeling

The objective of this section is to obtain the frequency response of the interconnections in the presence of the PDN consisting of voltage and ground planes. As described earlier, presence of RPDs along the signal path manifest themselves as increased insertion loss, crosstalk, and substrate coupling. All of these effects contribute to SSN. In this section, two methods are discussed for extracting the frequency response of the interconnections in the presence of RPDs, namely, the M-FDM and M-FEM. Both these methods are differential equation-based solutions, where the generated matrix is sparse, and therefore, can be applied to complex package and PCB designs. These two methods differ primarily in the meshing schemes used and the manner in which the equations are generated, though the underlying Maxwell's equations being solved are similar. M-FEM method finds application in structures with multiscale dimensions, where mesh refinement techniques can be applied to reduce the number of unknowns. In comparison, the M-FDM scheme uses a uniform grid, but is easy to implement and provides very accurate results. In both these methods, the PDN and signal interconnections are modeled separately and combined together using equivalent circuits. Two formulations that are available in literature for combining the PDN and interconnection models are discussed in this section. Both formulations have been applied to canonical examples and compared with other solvers or measurements to demonstrate accuracy and computational speed. In addition, the M-FDM method has been applied to the PCB example to demonstrate SSN effects in the frequency domain.

1) Single Plane Pair: The formulation for the PDN starts with the solution for a single plane pair consisting of a voltage (VDD) and ground plane (VSS) separated by a dielectric, as shown in Fig. 17. The cavity formed by the planes can be excited by the chip current, which acts as a current source causing the generation and propagation of an electromagnetic wave between the voltage and ground planes. The source of chip current is the driver circuitry. The objective is to compute the voltage disturbance between the planes due to the current source excitation, which can be obtained by solving Helmholtz equation. The underlying elliptic partial differential equation to be solved is of the form as follows:

$$(\nabla_t^2 + k^2)u = -j\omega\mu d J_z \tag{13}$$

where ∇_t^2 is the transverse Laplace operator parallel to the planar structure, k is the wave number, u is the voltage (different from

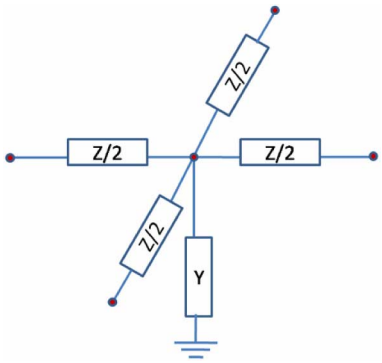


Fig. 18. Unit cell model.

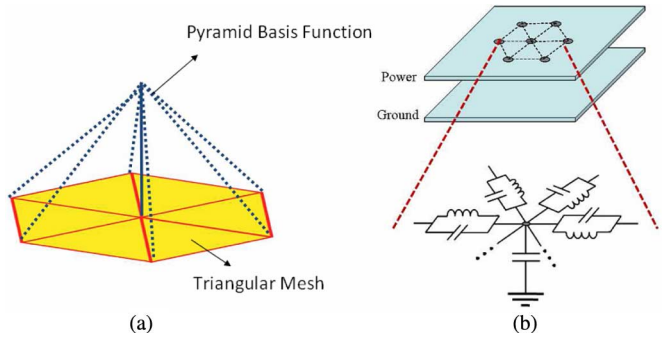


Fig. 19. (a) Triangular mesh and pyramid basis function. (b) Equivalent circuit.

the dc potential ϕ described for dc modeling), ω is the angular frequency, μ is the permeability, d is the distance between the planes, and J_z is the current density injected normal to the plane pair [13]. The transverse operator is a good approximation due to the small dimension d between the planes, and hence, the lateral mode of electromagnetic propagation dominates the frequency response of the parallel plate structure. The resulting electromagnetic wave is a radial wave that propagates away from the current excitation. The electric field is assumed to have only a vertical component, leading to a unique computation of voltage. The currents on the planes are shown in Fig. 17 as a forward and return current, based on the direction of the current source excitation. Since the periphery of the plane pair is open, the homogenous Neumann boundary conditions can be applied at the edges, which correspond to assuming a magnetic wall, or an open circuit, on the periphery of the planes.

a) Finite-Difference Method: The Helmholtz equation in (13) can be solved using the finite-difference scheme, similar to the solution to Laplace's equation for dc modeling described earlier. Using a five-point stencil function, the 2-D Laplace operator can be approximated as follows:

$$\nabla_t^2 u_{i,j} = \frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{h^2} \tag{14}$$

where h is the uniform mesh size and $u_{i,j}$ is the voltage at node (i, j) for the cell-centered discretization, as shown in Fig. 14, with a perfect magnetic conductor (PMC) boundary at the edges of the planes. In Fig. 14, the dc potential ϕ is replaced with the potential u, as described in (14). The PMC boundary can be implemented as follows:

$$u_{i,j} = u_{i+1,j} \tag{15}$$

where $u_{i,j}$ is the voltage on a boundary cell and $u_{i+1,j}$ is outside of the plane boundary.

Equation (14) can be converted into an equivalent circuit model representation [11] within a unit cell of dimension $h \times h$ of the form shown in Fig. 18. In Fig. 18, the unit-cell impedance and admittance parameters are given by

$$Z = 2\sqrt{\frac{j\omega\mu}{\sigma}} + \frac{2}{\sigma t} + j\omega L$$
$$L = \mu d$$
$$Y = \omega C \tan\delta + j\omega C$$
$$C = \frac{\varepsilon h^2}{d} \tag{16}$$

where ω is the angular frequency and t is the metal thickness. In (16), the impedance equation Z contains contributions due to dc and skin-effect resistance and inductance, while the admittance equation Y includes the contribution due to capacitance and frequency-dependent dielectric losses.

The equivalent circuit in Fig. 18 in each unit cell can be cascaded to generate a bed-spring model, similar to dc modeling, as described in [14]. The resulting matrix to be solved is of the form as follows:

$$\overline{\overline{Y}}\,\overline{U} = \overline{I} \tag{17}$$

where matrix $\overline{\overline{Y}}$ has a form similar to (12) with

$$\overline{\overline{A}} = \begin{bmatrix} Y+2/Z & -1/Z & & & \\ -1/Z & Y+3/Z & -1/Z & & \\ & -1/Z & \ddots & \ddots & \\ \ddots & \ddots & -1/Z & & \\ & & -1/Z & Y+3/Z & -1/Z \\ & & & -1/Z & Y+2/Z \end{bmatrix}. \tag{18}$$

The purpose of separating dc and frequency-domain modeling in this paper is because the governing equations for these two cases are different, although the unit cells appear to be similar.

b) Finite-Element Method: The Helmholtz equation in (13) can also be solved using the finite-element approximation with triangular mesh elements and linear pyramid or hat-basis functions [15]. The weak form of the partial differential equation in (13) can be written in variational form as follows:

$$\sum_{j=1}^{N} \iint_{\Omega} [\nabla u_j \cdot \nabla u_i + \omega^2 \mu\varepsilon u_j u_i + j\omega\mu d J_z u_i] dxdy = 0 \tag{19}$$

where Ω represents the 2-D problem domain. The triangular mesh and hat function u are shown in Fig. 19.

Equation (19) can be rewritten in matrix form as follows:

$$(\overline{\overline{K}} + \overline{\overline{M}})\overline{U} = \overline{F} \tag{20}$$

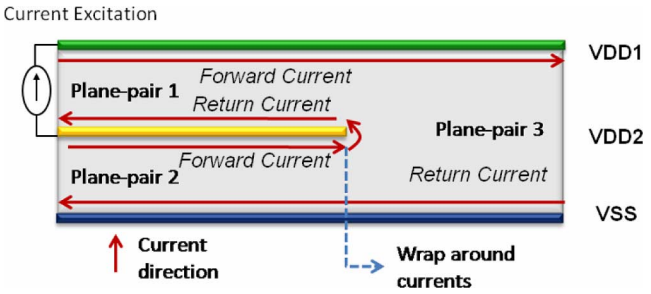


Fig. 20. Three planes.

where $\overline{\overline{K}}$ and $\overline{\overline{M}}$ represent the stiffness and mass matrices, respectively, $\overline{U}$ is the unknown potential, and $\overline{F}$ contains the contributions from the current source excitation [16]. In (20), $\overline{\overline{K}}$ and $\overline{\overline{M}}$ represent the admittance matrices of frequency-independent inductive and capacitive components, respectively, where $\overline{\overline{K}}$ contains inductors connected between triangle vertices (i.e., along the triangle edges), and $\overline{\overline{M}}$ contains capacitors connected between triangle vertices and to ground, as shown in Fig. 19. Both conductor and dielectric losses can be added to the structure, similar to the finite-difference formulation explained earlier. In the FEM, an adaptive mesh generation scheme can be used to create nonuniform triangular cells to better approximate the structure, while simultaneously reducing the number of unknowns. This is described through an example in a later section.

2) Multiple Plane Pair: Though the solution for a single plane pair is relatively straightforward using the FDM or FEM, extension to multiple plane pairs can be tricky due to the need for a common reference for all the planes. A blind application of either the FDM or FEM described earlier will lead to incorrect results for multiple planes, since this would completely eliminate any coupling between the plane pairs. This effect is especially important when planes have apertures in them, since this can cause electromagnetic coupling between the plane pairs. An example of a structure to illustrate this effect is shown in Fig. 20, where the center plane only covers half the length of the top and bottom plane. When the top plane (VDD1) is excited with reference to the center plane (VDD2) through a current source, currents on the two planes will be balanced through the forward and return currents, as shown in Fig. 20. The forward current on VDD1 plane will continue to flow past the VDD2 plane generating a return current on the bottom VSS plane, which in turn, will generate a forward current on the bottom side of the center plane. The return current on the top and bottom side of the center plane have to be continuous, leading to a wrap around current at the edge of VDD2 plane, as shown in Fig. 20. Capturing the wrap around current effect is important, since it contains information on the coupling between the two plane pairs (VDD1–VDD2 and VDD2–VSS). This effect can be extended to planes containing apertures as well.

For a multiple plane-pair structure containing more than two layers, it is possible to construct an equivalent circuit for each plane pair. However, the equivalent circuits of the different plane

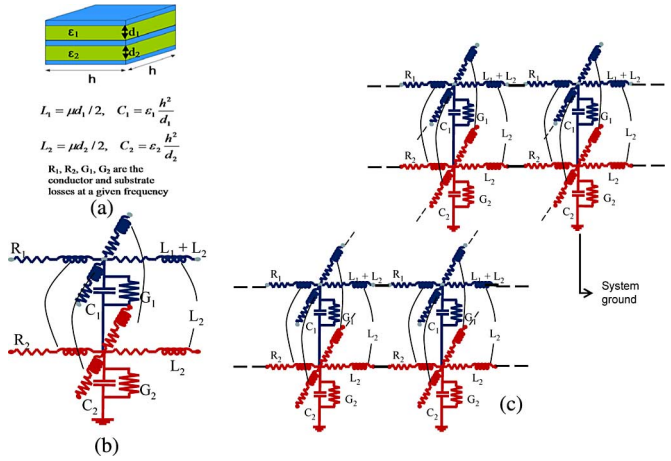


Fig. 21. Three planes. (a) Geometry and parameters. (b) Combined unit cell model. (c) Plane model consisting of multilayer unit cells.

pairs assign their respective ground reference node to the adjacent metal layer. Therefore, to obtain the model for the multilayered plane requires shifting the different reference nodes to one common ground. This shifting of ground reference nodes can be done using the indefinite admittance matrix approach, as described in [14] and [17].

For an M + 1-layer (M plane-pair) package or PCB with voltage/ground planes on each layer, the system matrix, $\overline{\overline{Y}}$ can be obtained as follows:

$$\overline{\overline{Y}} = \begin{bmatrix} \overline{\overline{Y}}_1 & -\overline{\overline{Y}}_1 & & & & \\ -\overline{\overline{Y}}_1 & \overline{\overline{Y}}_1 + \overline{\overline{Y}}_2 & -\overline{\overline{Y}}_2 & & & \\ & \ddots & \ddots & \ddots & & \\ & & \ddots & \ddots & & \\ & & & & -\overline{\overline{Y}}_{M+1} & \\ & & & -\overline{\overline{Y}}_{M+1} & \overline{\overline{Y}}_{M-1} + \overline{\overline{Y}}_M & \end{bmatrix} \tag{21}$$

where $\overline{\overline{Y}}_{i,i=1,2,..,M}$ are admittance matrices obtained for the ith plane pair counting from the top of the stack up.

The formulation related to the generation of the matrix in (17) using FDM is called as the M-FDM. Likewise, when the individual admittance matrices are obtained using the FEM, the resultant method is called as the M-FEM. These methods are described briefly in the following sections.

a) Multilayered Finite-Difference Method: Consider a three metal layer structure consisting of planes with dielectric thicknesses d_1 and d_2 for the first and second plane pairs, respectively, as shown in Fig. 21(a). This structure can be discretized into unit cells of size $h \times h$ as described earlier, with the equivalent circuit for each unit cell and each plane pair, as described in Fig. 18. The L and C parameters for each unit cell are as shown in Fig. 21(a). The unit cells for the two plane pairs can be combined using the indefinite admittance matrix, as shown in Fig. 21(b), where the bottom plane is chosen as the voltage reference plane. The equivalent circuit in Fig. 21(b) can be cascaded to derive the equivalent model for the entire structure, as in Fig. 21(c). In Fig. 21, the resistance and conductance

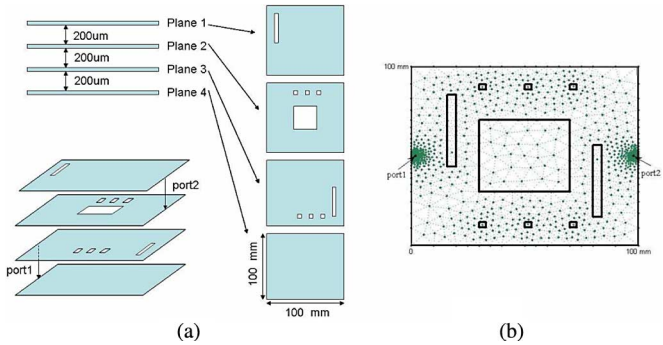


Fig. 22. (a) Multilayered planes with apertures. (b) M-FEM mesh.

terms have also been added to include conductor and dielectric losses. Details of the M-FDM formulation is described in detail in [14], [18], and [19] along with accuracy enhancement techniques by incorporating the effect of fringing- and gap-coupling fields [20], [21].

For a package or PCB geometry composed of $k+1$ layers, discretized using M_1-by-M_2 cells in the lateral directions, the computational complexity of M-FDM is $O(N^2)$ where $N = kM_1M_2$. Using nested dissection [22] improves the flop count to $O(N^{1.5})$ and memory to $O(N\log N)$.

b) Multilayered Finite-Element Method: The FEM described earlier is based on the application of an adaptive triangular mesh to a single pair. To extend this method to multiple layers requires the generation of the system admittance matrix in (17) under the condition that the triangle vertices on different layers lie at the same (x, y) coordinates. This is possible by flattening or collapsing the features on each metal layer on to a single layer on which the triangulation scheme can be applied to obtain the mesh. The mesh thus obtained is used to discretize all the layers simultaneously to generate the system matrix, as described in (17). Further details on the application of the method is described later in this paper and in [23].

3) Results for PDN: As an example, consider the case of a four metal layer structure consisting of planes, with dimensions of 100 mm $\times$ 100 mm, as shown in Fig. 22. The planes contain apertures, as shown in Fig. 22. The difference in dimensions of each aperture was maximized to emphasize the difference in using a uniform mesh and a nonuniform mesh. Hence, the largest aperture size used was 40 $\times$ 40 mm with a smallest aperture size of 3 $\times$ 3 mm. The minimum aperture size was chosen such that it still influenced the response of the structure at the maximum simulation frequency of 1 GHz. Two ports were placed between the bottom plane (ground) and the second plane, and between the third plane and the top plane, respectively, as shown in Fig. 22. The dielectric used was FR-4 with $\varepsilon_r = 4.4$.

The uniform meshing scheme consists of generating the matrix $\overline{\overline{Y}}$ with a cell size based on the smallest feature size, where the cell size has to be smaller or equal to the smallest feature size. The uniform mesh was used with the M-FDM to compute the system matrix. For the M-FEM, the multiple layers were flattened into one layer, with the resulting 2-D structure containing information on all the apertures and planes. The 2-D geometry

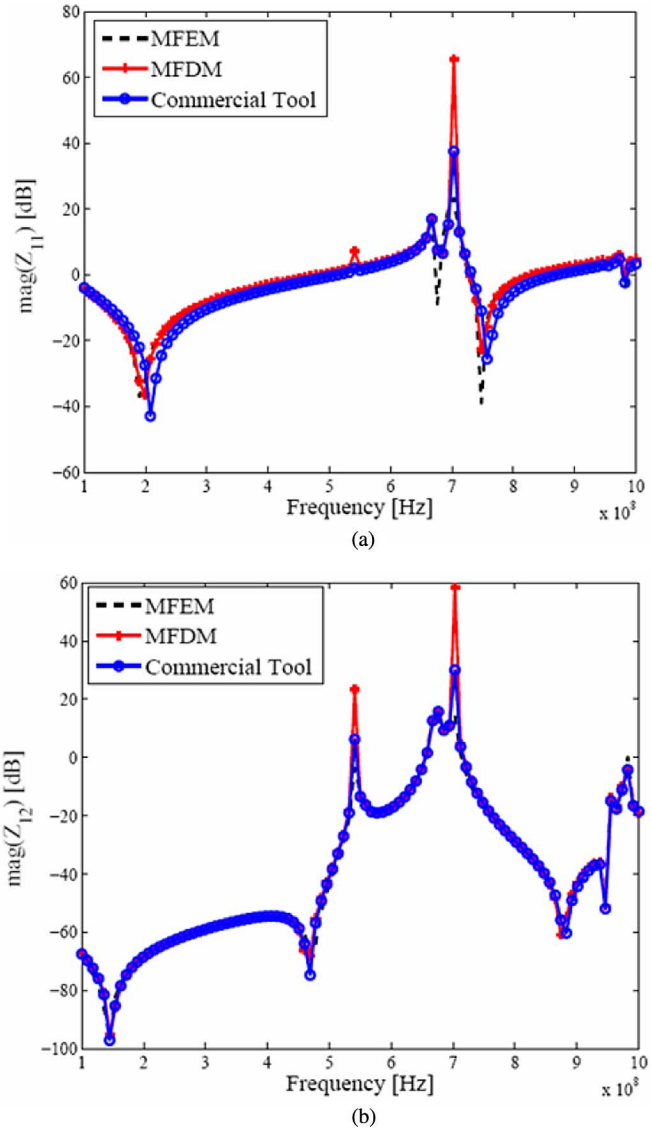


Fig. 23. (a) Self-impedance. (b) Transfer impedance.

was then discretized using a nonuniform triangular mesh, as shown in Fig. 22(b), and M-FEM was applied to generate the system matrix (21).

The self and transfer impedance results using M-FDM and M-FEM have been plotted in Fig. 23(a) and (b), respectively and compared to a commercial power integrity analysis tool. As can be seen, M-FDM and M-FEM agree with each other. Since, the loss was not included in M-FEM, the impedance magnitude at antiresonance is larger. The commercial tool has a shift in the resonance frequency for the self-impedance, which can be attributed to discretization error. M-FEM required 3594 unknowns as compared to 122 411 unknowns with M-FDM. The reduction in unknowns reduced the solution time per frequency point to 0.35 s with M-FEM as compared to 5.6 s with M-FDM. In comparison, the commercial tool required 71 204 unknowns with 2 s per frequency point.

4) Signal lines in the Presence of PDN: Signal lines on package and PCBs are electrically long, and hence, behave

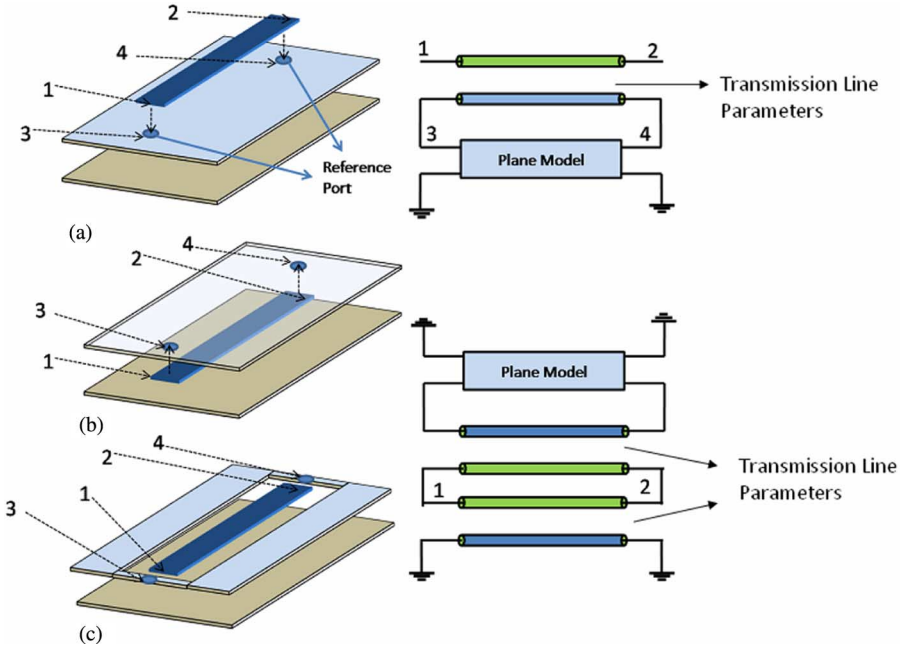


Fig. 24. Transmission-line models with nonideal reference planes. (a) Microstrip line. (b) Stripline. (c) Conductor-backed CPW.

as transmission lines. Hence, distributed effects, such as delay and impedance characteristics of the transmission lines have to be included during modeling. In addition, the return currents of the transmission lines on nonideal reference planes play an important role especially for discontinuities along the return path.

An intuitive understanding of the return currents can be used to obtain equivalent circuit models that integrate the response of the package and the transmission line [10], [24], [25]. These circuit models rely on a four-port model of the transmission line, where the I/O terminals are referenced to the corresponding nodes on the planes. The impedance of the transmission lines can be adjusted to correctly represent the current flowing on each plane based on the physical dimensions of the structure or by using a 2-D solver. The admittance matrix representation for the combined system, which consists of transmission lines referenced to power and ground planes can then be obtained as described in [19] and [25].

Examples of models for typical signal lines referenced to nonideal power and ground planes are shown in Fig. 24. The simplest case is that of the microstrip line, shown in Fig. 24(a). All of the return currents of the microstrip line flow on the plane immediately beneath it. Thus, the reference ports of the transmission-line model of the microstrip line are connected to the nodes on the plane beneath the line, as shown in Fig. 24. In Fig. 24, ports 1 and 2 represent the I/O terminals of the signal line with the corresponding reference ports at 3 and 4, respectively. The signal transmission-line parameters, such as characteristic impedance (Z_0) and propagation constant (γ) can be obtained using a field solver. Similarly, for the stripline in Fig. 24(b), part of the return currents flow on the top reference plane, while the rest flows on the bottom plane. Thus, the equivalent circuit representation is constructed by modeling the stripline by two transmission lines, whose I/O signal ports are shorted together. The reference nodes for the transmission lines are connected to nodes on the top and bottom plane, where the characteristic impedance of each transmission line determines the return current through each plane. The characteristic impedance varies as a function of the proximity of the transmission line to the reference plane, and hence, this approach can be used to model asymmetric transmission lines in the presence of nonideal voltage and ground planes. In both M-FDM and M-FEM, the voltages are always computed between metal layers. To implement these methods, the last metal (plane) layer is set to ideal ground, as shown in Fig. 24(b), without changing the voltages between the metal layers. Finally, a conductor backed coplanar waveguide (CPW) line with shorted side conductors, as shown in Fig. 24(c), can be modeled similar to the stripline model. The frequency response of the transmission lines can be obtained using analytical solutions or by using a 2-D field solver [26].

A more rigorous model can be derived for connecting the signal lines to the reference planes by using modal decomposition. For a three conductor system consisting of two parallel plates (voltage/ground) and a signal conductor, there are two possible quasi-TEM modes, which are the parallel-plate-waveguide mode between the power/ground planes and the transmission-line mode between the signal conductor and ideal reference planes. Details on developing modal decomposition-based models are described in [11]. Modal decomposition is a method to decouple multiconductor transmission-line equations into uncoupled single transmission-line equations. This is done through the transformation of line voltages and currents into modal voltages and currents, where each mode is decoupled from the other. Using modal decomposition, the combined admittance matrix $\overline{\overline{Y}}_{\mathrm{sys}}$ of a transmission line referenced to nonideal reference

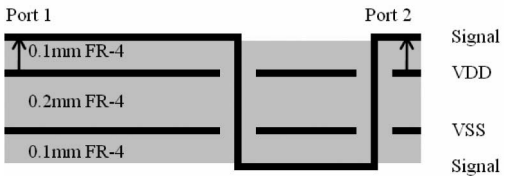


Fig. 25. Test vehicle.

planes can be expressed as follows [11]:

$$\overline{\overline{Y}}_{\rm sys} = \begin{bmatrix} k^2\overline{\overline{Y}}_{\rm sig} + \overline{\overline{Y}}_{\rm par} & k\overline{\overline{Y}}_{\rm sig} \\ k\overline{\overline{Y}}_{\rm sig} & \overline{\overline{Y}}_{\rm sig} \end{bmatrix} \tag{22}$$

where the admittance matrix of the planes $\overline{\overline{Y}}_{\rm par}$ is obtained using M-FDM or M-FEM, the admittance matrix $\overline{\overline{Y}}_{\rm sig}$ is obtained analytically or by using a 2-D field solver and the parameter k can be obtained based on the transmission-line structure.

Equivalent circuit models of vias and other discontinuities can be connected to the models derived for the signal lines referenced to nonideal reference planes in addition to components, such as decoupling capacitors.

The accuracy of the signal-line models coupled to nonideal reference planes can be verified through measurements using test vehicles. As an example, consider the microstrip-to-microstrip via-transition test vehicle shown in Fig. 25. The signal line was designed to be 0.17-mm-wide with a characteristic impedance of 50 Ω, with a total length of 30 mm. Since the two planes have different dc potential, they are not shorted together. The top plane is a voltage plane (VDD), while the bottom plane is a ground plane (VSS). The equivalent circuit model for the microstrip-to-microstrip transition involves a π model representation for the vias connected to the corresponding planes [11]. While constructing the model, parameter $k = -1$ in (22) for the microstrip line referenced to the nonideal voltage reference plane [11]. The two via transitions cause RPDs, the effects of which can be seen in the insertion loss and the return loss of the line. The parameters of the signal line was measured between port 1 (near end) and port 2 (far end) using cascade coplanar probes up to 10 GHz and was compared to a commercial 3-D full wave tool and M-FDM. The results of the insertion loss are shown in Fig. 26, where the small discrepancy between model and measurements at higher frequencies can be attributed to calibration, deembedding, frequency-dependent material properties, and manufacturing variation-related issues. The resonance frequencies in Fig. 26 correlate well between M-FDM and the commercial 3-D full wave solver indicating that all important effects in signal to power coupling have been captured in the M-FDM formulation. In Fig. 26, the commercial tool has lower loss compared to measurements, while M-FDM captures the losses well.

5) Frequency Response of PCB: To demonstrate the application of M-FDM to an industrial example, the four layer PCB in Fig. 13 was modeled to obtain the frequency response of the signal lines in the presence of the voltage and ground planes. Since the signal lines form an asymmetric stripline structure, both planes carry current, which can lead to RPDs, which get amplified when the driver and termination circuits are connected. Sphinx [27], a software tool based on M-FDM was used to model the signal lines in the presence of the power and ground plane. The structure was discretized into 473 × 603 cells, resulting in ∼736 K unknowns in the matrix (17). Thirteen current excitation ports were specified of which 11 consisted of excitation on signal lines, while the remaining two were defined between the voltage and ground plane, in the vicinity of the chip, as shown in Fig. 13. Eleven signal lines were located on layers M_2 and M_3 and were separated from each other to ensure minimum crosstalk. These signal lines were all excited with reference to the ground plane.

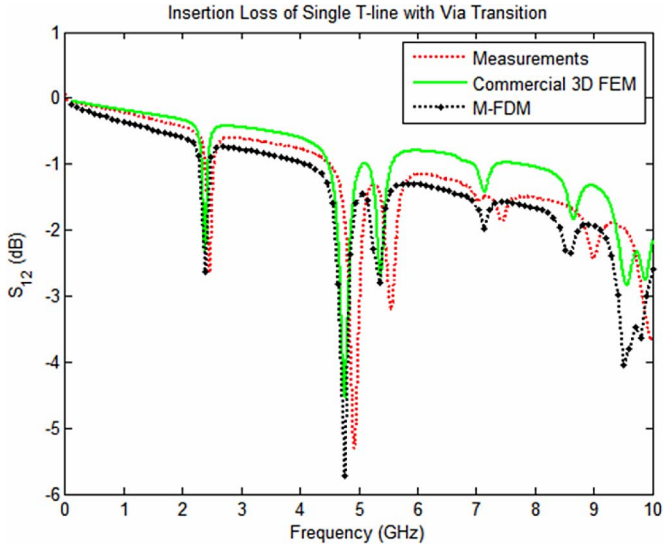


Fig. 26. Measurement of test vehicle.

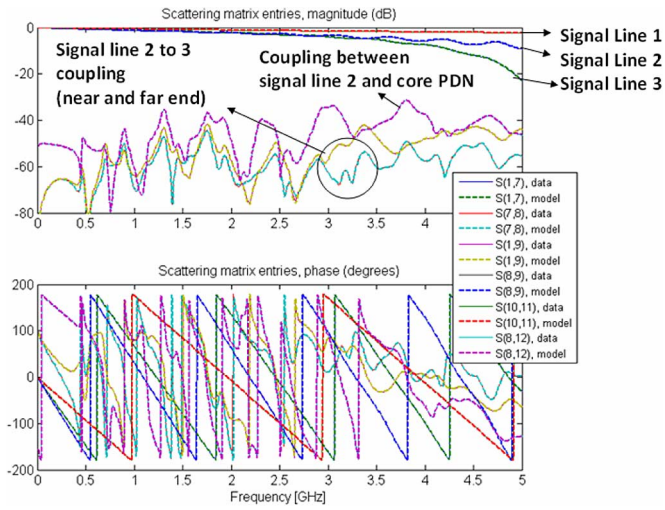


Fig. 27. Frequency-domain response of PCB and correlation with macromodel.

The frequency response of the signal lines and power distribution were modeled from 1 MHz to 5 GHz. The insertion loss of three signal lines is shown in Fig. 27. The positions of the signal lines along with their I/O terminal positions are shown in Fig. 13, where signal lines 1 and 2 are present on layer M_2,

while signal line 3 is present on layer 3. As can be seen from the figure, the insertion loss of the signal lines start deviating from each other beyond 3 GHz with signal lines 2 and 3 having insertion loss >20 dB and 10 dB at 5 GHz, respectively. This effect can be attributed to the RPD for the stripline structure. The coupling between signal line 2 and 3 (both near end and far end) are also shown in Fig. 27, where the maximum coupling is ∼40 dB. Since the signal lines are far apart, this coupling is due to the substrate through the voltage and ground planes. Since core and I/O circuits share a common PDN in this example, there can be substantial coupling between the two, which is shown in Fig. 27 between signal line 2 and the core. This coupling, which is ∼–30 dB, can cause distortion of the signals propagating on signal line 2 when the core is switching, as demonstrated in a later section.

The 13 × 13 scattering parameter matrix representing the frequency response of the 11 signal ports and the two cores from 1 MHz to 5 GHz provide information on the behavior of these structures over a large bandwidth. The effect of RPDs is contained in the port response represented by the scattering parameter matrix. With a suitable change in the layout, the scattering matrix can be changed to meet specifications. Hence, frequency-domain modeling can be applied repeatedly until the response at all frequencies of interest meets the desired specifications. At this juncture, the frequency response needs to be converted into a SPICE netlist to which nonlinear drivers and other termination circuitry can be attached to compute eye diagrams. This is accomplished through macromodeling, which is the subject of the next section.

C. Macromodeling

The results of the modeling flow described in Sections IV-A and B can be combined into a unique frequency-domain characterization of the PDN and signal distribution networks. This characterization is available in terms of frequency samples of the fully coupled transfer matrix of the system, from dc up to the highest frequency of interest. One has the choice of the particular I/O representation for further processing steps. Although admittance and impedance formulations are common, a scattering representation has been used here for both voltage and signal ports. The global-scattering matrix at any frequency is readily computed from other representations using standard network transformations. There are three main advantages with this choice: 1) the scattering matrix is always defined, whereas impedance and admittance can be ill-defined even for simple configurations; 2) admittance and impedance matrices may have elements with a high-dynamic range, whereas the scattering matrix has always bounded elements; and 3) as a consequence, numerical processing of data in scattering form is inherently better conditioned and more reliable with respect to other forms. Throughout this section, we therefore consider as "raw" data the finite set of scattering matrices $\hat{S}(j\omega_k)$ corresponding to frequencies $\omega_k, k = 1, \ldots K$.

The main purpose of this section is to provide a strategy for converting the frequency samples $\hat{S}(j\omega_k)$ into a form that can be processed in time-domain analyses using standard circuit simulators. This is a crucial step in coupled signal-power modeling, since nonlinear effects of drivers/receivers and termination networks on signal and power quality need to be accurately captured. Two main approaches are available for this task. A first class of methods translates the frequency-domain samples into time-domain samples using standard discrete Fourier transform (DFT) methods [28]. This process results in a set of sampled impulse responses, which can be solved in time domain using convolution methods. This technique has several major drawbacks when applied to coupled signal-power delivery networks. First, special care needs to be taken in DFT application, including suitable windowing, in order to avoid aliasing effects [29]. Second, time-domain convolution is applicable directly only to the linear part of the overall structure, and a dedicated formulation is required to link the convolution kernel to the nonlinear solver required by the terminations. This functionality is usually not available in standard SPICE kernels. Third, the computational cost is extremely high, hence not compatible with the requirements of a fast design flow. These drawbacks inevitably lead to the adoption of a second strategy, based on macromodeling.

Macromodeling amounts to extracting a SPICE-compatible equivalent circuit, whose frequency responses match within some small tolerance the available frequency-domain samples [30]–[51]. This approach is possible through the following steps. First, a rational curve-fitting process is performed on the available frequency samples. This is purely numerical procedure, leading to a closed-form approximation of the frequency responses in terms of rational functions of the Laplace-domain variable s. Besides accuracy, the stability, causality, and passivity of the rational model must be guaranteed during this phase for ensuring model robustness and reliability during transient simulation [28], [29], [52]–[54]. A second step processes these rational functions and synthesizes a lumped circuit in terms of standard circuit elements. This is possible, since Laplace-domain rational functions correspond to systems of ordinary differential equations (ODE) in time domain, and any lumped circuit is also governed by ODEs. The translation of rational functions into equivalent circuits is a fully automated and well-documented process, which does not require special care [29]. Therefore, the focus of this section is on the passivity-constrained rational fitting only.

Rational macromodeling has been known since many decades [38], [39]. Wide applicability has however become feasible only in the most recent years, due to a number of key results. The first important milestone was the introduction of the vector-fitting (VF) algorithm [44]–[46]. VF formulates the rational curve fitting into an iterative linear least-squares process applied to a partial fraction expansion form. More precisely, if $\hat{H}(j\omega)$ denotes a generic single element of the scattering matrix, the rational approximation can be written in the form as follows:

$$\hat{H}(j\omega) \approx \frac{a_0 + \sum_{m=1}^{n} a_m \varphi_m(j\omega)}{b_0 + \sum_{m=1}^{n} b_m \varphi_m(j\omega)} \tag{23}$$

where the "basis functions" are defined as $\varphi_m(s) = (s - q_m)^{-1}$ via a set of arbitrary (different) constants q_m, which are the "starting poles". The unknown constants $\{a_m, b_m\}$ are

determined by rewriting (23) at each available frequency ω_k as follows:

$$\left(b_0 + \sum_{m=1}^{n} b_m \varphi_m(j\omega_k)\right) \hat{H}(j\omega_k) \approx a_0 + \sum_{m=1}^{n} a_m \varphi_m(j\omega_k) \tag{24}$$

and by solving the resulting overdetermined linear system in least-squares form. Once the coefficients $\{b_m\}$ are known, the zeros $\{q'_m\}$ of the denominator in (23) are computed using standard methods [55], [56], and the process is repeated by iteratively replacing the starting poles $\{q_m\} \leftarrow \{q'_m\}$ in the definition of the basis functions $\varphi_m(s)$. The iterative process converges rapidly, providing a set of stabilized poles $\{q_m^{\infty}\}$. A final linear least-squares system is formed to estimate the associated residues

$$\hat{H}(j\omega_k) \approx r_0 + \sum_{m=1}^{n} \frac{r_m}{j\omega_k - q_m^{\infty}}. \tag{25}$$

The aforementioned process was outlined for a scalar response. In case of several tens of ports, as required by a coupled signal-power integrity analysis, poles, and residues must be computed for all responses, possibly requiring large computing time and memory. A good solution to this problem is to split the entire set of responses into disjoint subsets, which are processed separately [50]. Another solution was introduced in [51], where the feasibility of a global fitting with a common set of poles was demonstrated. Essentially, an incomplete QR decomposition is applied to all individual subsystems (24), and only the coefficients $\{b_m\}$ are retained as global unknowns. In this section, the focus is on a column-based splitting of the scattering responses (i.e., each column is processed independently). Within each column, the QR decomposition is applied to minimize the computational cost. This "compressed" hybrid VF formulation is applicable to systems exceeding 100 ports, thus providing excellent scalability. Finally, the implementation of (24) and (25) includes an explicit constraint for enforcing the dc response of the model to match exactly the dc point in the raw data. This is essential for achieving correct bias levels during transient simulations, including nonlinear devices.

While models obtained with VF or derived algorithms are stable and causal by construction, they may not be passive, and in turn, may lead to unstable transient results even when connected to other stable and passive models [28], [29], [52]. It is important to note that a passive macromodel $S(s)$ must fulfill the following three conditions [53], [54]:

$$S(s) \text{ analytic in } \Re\{s\} > 0 \tag{26a}$$

$$S^*(s) = S(s^*) \tag{26b}$$

$$I - S^H(s)S(s) \geq 0, \Re\{s\} > 0 \tag{26c}$$

where superscript H denotes Hermitian transpose. Condition (26a) is satisfied for all stable models, implying causality as well [53], [54]. Condition (26b) is verified if the model poles and residues are real or appear in complex conjugate pairs. This is usually structurally enforced in the model formulation (23). Condition (26c), which can be safely restricted to the imaginary axis $s = j\omega$, states that the model has no energy gain at any frequency, or, equivalently, that the frequency-dependent trajectories of the singluar values $\sigma_\nu\{S(j\omega)\}$ are uniformly bounded by one [56]. This condition may be challenging, since the entire continuous frequency axis (from dc to infinity) needs to be checked, using a condition that involves all scattering matrix entries of the model at the same time. Fortunately, purely algebraic methods for checking (26c) are available, by means of the Hamiltonian matrix M associated with the model [57], [58]. If M has no imaginary eigenvalues, the model is already passive. Conversely, the presence of imaginary eigenvalues indicates passivity violations, i.e., energy gain at some frequencies, which need to be taken care of. When present, passivity violations may be of different nature. In-band violations are usually very small, since models obtained by VF closely match the raw input frequency samples, which usually satisfy (26c). Conversely, out-of-band violations may be severe, since the true response of the system is not known, and there is no easy way to constrain the energy gain of the system during the fitting stage [59].

This issue motivated the development of several algorithms for the *a posteriori* enforcement of passivity via perturbational approaches [58]–[71]. Most common formulations aim at correcting the model residues by small amounts, so that the corrected model is passive. A review of these techniques is available in [59], where the computational complexity is also compared. Convex optimization approaches based on linear matrix inequality (LMI) of the Kalman–Yakubovich–Popov (KYP) [63]–[65] type are here ruled out due to their high-computational cost imposed by the large-scale nature of the models of interest. Two other suboptimal algorithms are available, namely 1) passivity enforcement at discrete frequency points via linear or quadratic programming [59], [61], [62], [66]–[70], or 2) iterative perturbation of the imaginary eigenvalues of the Hamiltonian matrix associated to the model [58]–[62], [71]. Denoting with x, the array containing all the residue perturbations, these two schemes can be formulated, respectively, as follows:

$$I\text{: } \begin{cases} \min x^T P x \\ Rx \leq g \end{cases} \quad \text{and } II\text{: } \begin{cases} \min x^T P x \\ Qx = r \end{cases} \tag{27}$$

where the symmetric and positive definite matrix P, related to a weighted controllability Gramian of the model [56], [58], [62], ensures accuracy preservation during perturbation via a suitable norm weighting. The inequality constraint $Rx \leq g$ states in compact form the requirement that the residue perfurbations should displace the energy gain of the model below the unit threshold [66], [69]. Conversely, the equality constraint $Qx = r$ forces the purely imaginary Hamiltonian eigenvalues to collapse and move off the imaginary axis, hence reaching passivity [58]. Scheme I is typically more robust than II when passivity violations are large. Conversely, scheme II is more effective for small and well-localized passivity violations, since it requires less iterations. In this section, a hybrid method that combines the main advantages of these two approaches is used [49]. The passivity violations are first localized using a fast Hamiltonian eigenvalue solver [60], [61]. Then, two successive iteration loops are started. Scheme I is first applied, in order to remove the possibly

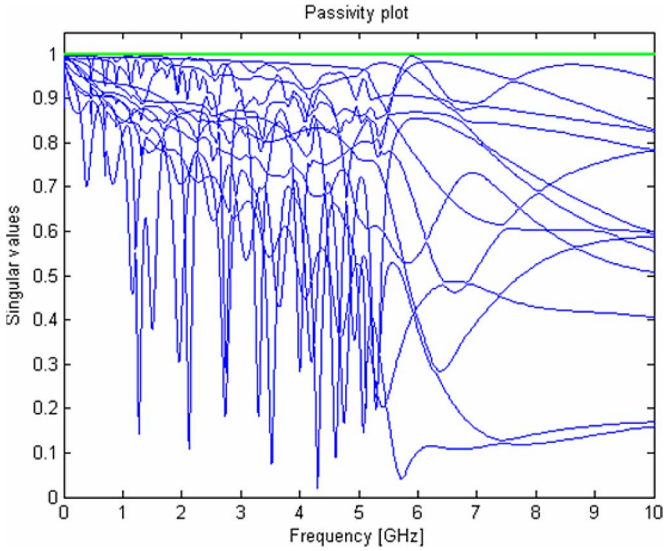


Fig. 28. PCB example. Frequency-dependent singular values after passivity enforcement.

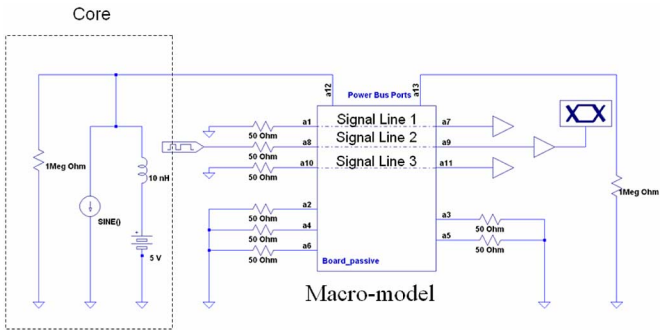


Fig. 29. SPICE setup with macromodel.

large out-of-band passivity violations, followed by scheme II, in order to remove any small residual passivity violations.

The excellent numerical performance of the proposed passive macromodeling scheme is illustrated on the PCB example of Fig. 13. In Fig. 27, the frequency response obtained from M-FDM has been compared with the passive model constructed using the macromodeling process described in this section. There is no visual difference between model and data for all curves, including the sensitive crosstalk and signal-power couplings. These results confirm the reliability of macromodeling techniques for coupled signal-power integrity analysis. Fig. 28 depicts the frequency-dependent singular values of the model after passivity enforcement. Since all singular values are less than one at any frequency, the model is passive. The overall CPU time required for rational curve fitting and passivity enforcement was 2 min 31 s on a 2 GHz PC with 2 GB RAM.

D. Eye Diagrams

The macromodel derived from the previous section can be converted into a SPICE subcircuit and incorporated into a SPICE circuit for simulation, as shown in Fig. 29. The macromodel

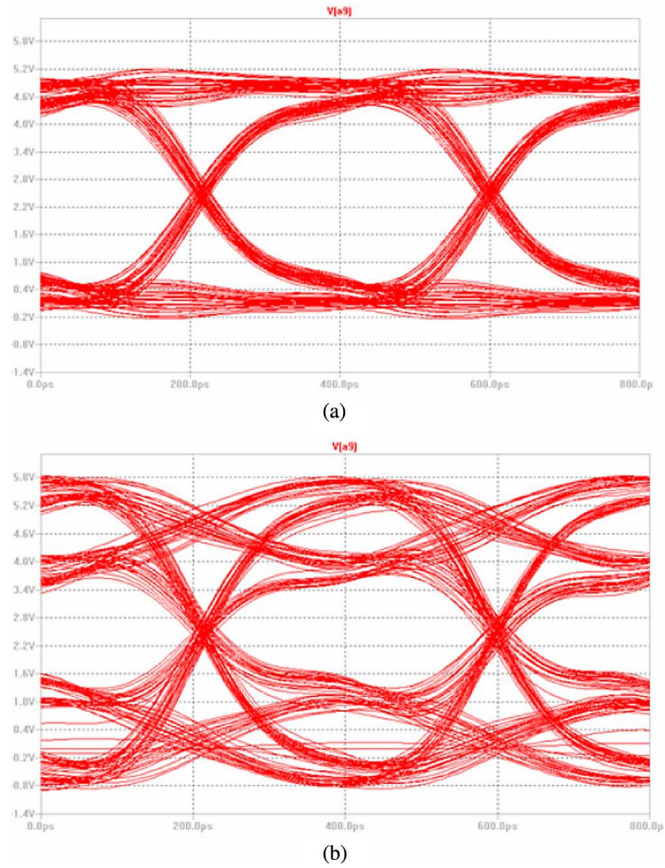


Fig. 30. Eye diagram with (a) core turned OFF and (b) core turned ON.

represents a black box representation of the frequency response of the system at the 13 port locations. These are shown in Fig. 29, where the macromodel contains all of the coupling information from the PCB layout between all the ports. Signal lines 1, 2, and 3 and the port connected to the core, described in Fig. 13, are also shown in Fig. 29. The macromodel can now be connected to drivers and termination circuitry, as shown in Fig. 29, to compute eye diagrams. In Fig. 29, the core power distribution ports are terminated with a 1 MΩ resistor indicating an open circuit. A VRM with a supply voltage of 5 V and 10 nH is connected to one of the ports corresponding to the core power distribution.

The input end of signal line 2 was excited with a 500-bit PRBS at a bit rate of 2.6 Gb/s and the output was simulated to compute the eye diagram using SPICE, with the circuit in Fig. 29. All the other lines were terminated in an impedance of 50 Ω with no switching activity. The two ports corresponding to the core were initially assumed to be idle indicating no switching activity. The resulting eye diagram is shown in Fig. 30(a), which shows a reasonably good eye.

This example was then repeated with core switching, where a 1 A sinusoidal current source was used to mimic the core switching activity, using the circuit in Fig. 29, with all other conditions remaining the same as the previous example. The resulting eye diagram is shown in Fig. 30(b), where the eye is distorted due to coupling between the core and signal line 2. This

coupling results in excessive jitter and eye closure, as shown in Fig. 30(b).

Such an eye diagram can be fixed by analyzing the response in the frequency domain. In this example, the design change requires adding decoupling capacitors to the PDN to improve the isolation between signal line 2 and the core power distribution.

V. New Paradigm for Power Distribution

Designing for power integrity described in the previous sections require the identification of discontinuities along the return path and mitigating these discontinuities using decoupling capacitors or other means. As discussed earlier, the source of the RPDs can occur in the layout or after attaching the driver, receiver, and termination circuitry to the package and PCB. This can be difficult for complex layouts, and hence, the end result is to develop a power distribution scheme that has low impedance. This can be accomplished both for the core and I/O circuits by using several decoupling capacitors on the PDN to reduce its impedance. Such a design process can be supported through modeling methods both in the frequency and time domain, as described in the earlier sections. Such a design and modeling methodology still requires an understanding of the source waveforms, where a designer needs to asses whether a specific resonance on the PDN needs to be mitigated or not using decoupling capacitors. Such an iterative scheme often can lead to long design cycles.

A possible solution to RPDs could be the development of an alternate power distribution scheme that eliminates RPDs along the signal paths. Such a scheme could potentially lead to a structure that requires a high-impedance power distribution, thereby eliminating several decoupling capacitors on the board, reducing the layers required for power distribution and reducing long design cycles. The required modeling tools to support such a signal and power distribution scheme can be simplified as well. Such an approach can be implemented using power transmission lines (PTL) [72], [73].

In the methods described for power distribution in the previous sections, the goal was always to use voltage (VDD) and ground (VSS) planes with the signal lines referenced to them. As was discussed in Section II, irrespective of the stack up, the voltage and ground planes always lead to RPDs. This was shown for a microstrip line over voltage and ground planes, where even with termination resistors, an RPD was formed during the transitioning of the driver. A possible method for eliminating RPDs for the microstrip line is by replacing the voltage plane using a PTL, as shown in Fig. 31(a). The PTL is a transmission line with characteristic impedance that is matched at the source end to the power supply and to the rest of the circuitry in the signaling path, as illustrated in Fig. 31(a). Since the signal line and the PTL share a common ground plane, no RPDs are generated during both the low-to-high and high-to-low transition of the driver. An advantage of this scheme is that since the PTL has impedance in the 25–50 Ω range based on the matching conditions required, the implementation of this approach requires high impedance for the power distribution, which is in direct contrast to the methods being pursued today.

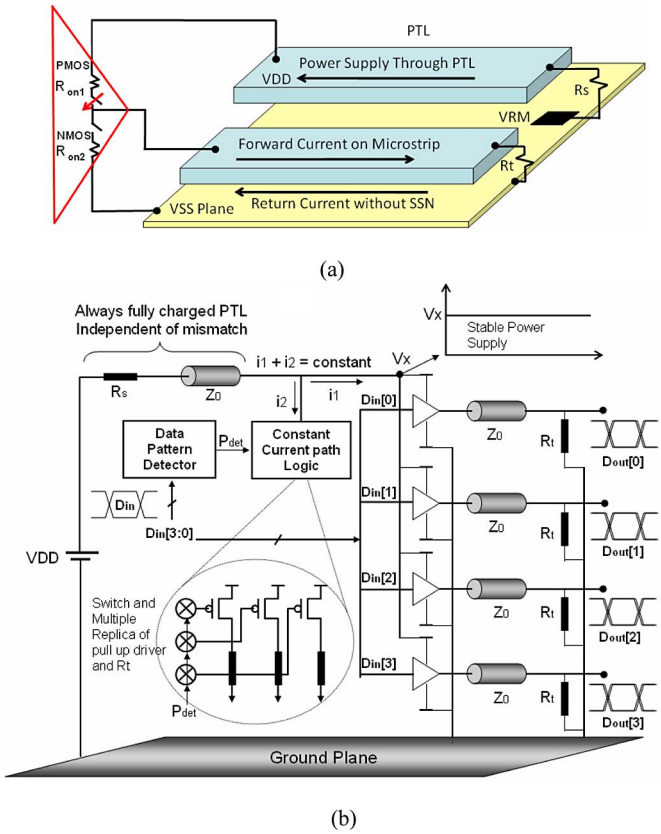


Fig. 31. (a) PTL concept. (b) CC-PTL signaling.

For the PTL scheme to be feasible, several critical issues need to be solved for adopting such a method in a practical signaling environment. First, the dynamic dc drop on the power supply network caused by dc resistance and data pattern should be considered. Second, the mismatch in the PTL impedance due to manufacturing variations needs to be considered as well, since the topology in Fig. 31(a) is developed under the premise that all of the transmission lines are suitably matched to each other. Thirdly, the power consumed needs to be assessed carefully. Assuming these three issues are resolved, the PTL concept can potentially be applied in real designs, where such a scheme can lead to major cost savings in the solution for I/O PDNs by eliminating capacitors, reducing the layer count, and simplifying the design process.

A possible approach for solving two of the three problems stated earlier is by using the constant current PTL (CC-PTL). Fig. 31(b) shows the basic conceptual diagram of the CC-PTL scheme, where a PTL is used to feed VDD voltage to four I/O drivers, each connected to a signal transmission line. In this scheme, the PTL is always fully charged with CC, so that there is no charging and discharging of the PTL during signal transitions. This is possible by using a current control knob connected to the PTL. The current control knob has variable resistive paths, which can be changed according to the input data pattern, thereby always maintaining a CC in the PTL. By using the CC-PTL scheme, two of the three issues mentioned earlier can be resolved. First, the voltage node of the driver will not

generate any noise due to the PTL always being fully charged during both the signal transitions. Second, the characteristic impedance of the PTL no longer has an effect on power supply path, thereby eliminating any mismatch-related issues. The CC-PTL scheme can be used to achieve near zero SSN due to the power supply noise being near zero, thereby leading to near zero jitter and a large eye opening. Details on the CC-PTL scheme along with a comparison with conventional signaling schemes are available in [73].

One disadvantage of the CC-PTL scheme is the increased power consumption caused by CC flowing from VDD to ground through the PTL. This issue can be addressed by adjusting the voltage swing level leading to low-voltage signaling with near zero jitter.

Such alternate power distribution schemes are still in their infancy, and therefore, require years of research before they find application in products.

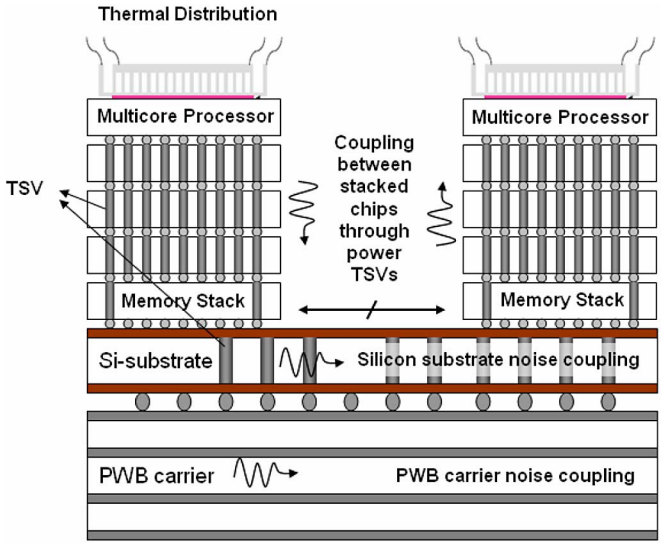


Fig. 32. Power distribution challenges for 3-D system.

VI. Future Challenges

As is well known, the semiconductor industry has been driven by Moore's law, where the scaling of the transistor from one generation to the next has led to higher performance, higher functionality, and higher levels of integration. However, device speed is no longer scaling well below the 65 nm node with leakage currents becoming a major impediment beyond the 45 nm node. With lithographic solutions becoming a barrier beyond the 32 nm node, the semiconductor industry is looking to alternate solutions [74]. One possible solution being investigated by companies and academia across the world is 3-D integration, where chips can be connected to each other along the vertical dimension as well. This is being made possible through the development of through silicon via (TSV) technology, where chips can be stacked and connected to each other using vias that provide connections from the top to the bottom surface of the chip. This along with advancements in copper-to-copper bonding technologies is allowing the stacking of a large number of chips on top of each other with vertical interconnections between them. Since, the wire length between the devices can be reduced, 3-D integration has the potential of improving performance while simultaneously reducing leakage and providing an alternative to expensive lithographic solutions. In addition, heterogeneous integration is possible, where dissimilar chips can be bonded together resulting in a 3-D stack consisting of sensors, RF, optical, logic, memory, and power supply regulator ICs. Packaging can be a daunting task for 3-D chips due to the large number of I/Os that need to be supported. Methods based on silicon interposer or silicon substrate provide possible solutions, where these packages provide connectivity between the top to bottom silicon surface using TSVs as well. A schematic of a digital subsystem consisting of 3-D stacks with logic and memory mounted on a silicon package is shown in Fig. 32, where the 3-D stacks are connected to each other through a switch fabric on the silicon package. The switch fabric enables the processor chips to communicate with the memory on any of the 3-D stacks leading to a distributed memory environment. The TSVs in the 3-D stack and the silicon substrate are also shown in Fig. 32.

From a power integrity standpoint, 3-D integration can be very challenging and also help in certain areas. Providing dc power to the chips requires a good handle on the voltage drops, which can be large, especially if several chips are stacked on each other. This combined with joule heating can lead to power dissipation and localized heating, resulting in thermal hot spots across the 3-D stack. Hence, power delivery requires a careful assessment of thermal management solutions as well. The TSV parasitic inductance and resistance are typically small, and therefore, can help power delivery. With a large number of TSVs providing power to the chips, the TSV capacitance can be used to design a low-impedance PDN, whose capacitance can be controlled by varying the substrate bias voltage. However, with the semiconducting silicon substrate surrounding the TSVs, signal propagation can be attenuated with substantial coupling to the neighboring TSVs. This loss of energy can be a problem if not compensated adequately. Clearly, signal and power I/O density can be very large at the package level due to the large number of TSVs that need to be serviced from the package into the 3-D stack, leading to increased SSN at the package level. This can cause signal integrity problems with increased jitter and a reduced eye mask. From Fig. 32, 3-D integration poses some unique challenges and opportunities that may require alternate methods for power delivery that has not been looked at so far.

VII. Conclusion

RPDs are a major source of SSN in modern packages and PCBs. This has been discussed in detail in this paper with emphasis on design-related issues and modeling methods, which have been supported by simulation and measurements. Through frequency- and time-domain results, the importance of RPDs in the context of signal to power coupling was discussed. A

possible scheme for eliminating RPDs using PTLs was proposed along with future challenges in 3-D integration.

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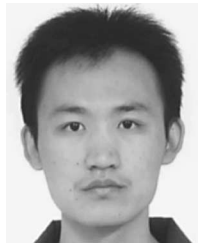

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