Behavioral modeling of IC core power-delivery networks from measured data

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***Abstract*—The modeling of the core power-delivery network of digital ICs is addressed by a black-box approach, leading to an n-port equivalent of the IC. The model parameters are estimated from external measurements carried out at the IC ports. The modeling procedure is demonstrated for a commercial NOR Flash Memory in 90 nm technology housed by a specifically-designed test fixture.**

***Index Terms*—Digital integrated circuits, I/O ports, power delivery network, circuit modeling, macromodeling, power integrity.**

I. Introduction

High-performance applications, as those occurring in converging technologies where the coexistence of analog blocks, high-density memories and digital processing units leads to complex and critical systems, grow in importance in the recently-proposed multichip architectures. One of the challenges of these modern systems solutions is the prediction of the switching noise generated by the current absorption of digital circuits, that can interfere on the stable functioning of the entire multichip system. Hence, reliable models of the core power delivery networks of integrated circuits (ICs) are highly desirable.

Behavioral models of the IC core power delivery networks have already been proposed and exploited in [1], [2], where simplified and physically-inspired circuit equivalents attempt to describe the different blocks involved in the power delivery network of the digital IC. Efforts are made to define and improve the basic circuit equivalents and to provide a set of general guidelines for the computation of model parameters from both numerical simulation and real measurements. However, the estimation of model parameters from measured data and the inherent multiport nature of the power delivery structures of ICs, are scarcely addressed by the current literature.

In this paper, the behavioral modeling of the IC core power networks is addressed by a black-box approach. This approach amounts to characterizing the device being modeled as an n-port element defined by a set of network functions, *e.g.*, by the admittance parameters, without using information on the internal structure of the device. The model parameters are obtained from the port responses of the power delivery network, only. The modeling procedure benefits from simple relationships between the model parameters and the measured responses and allows for multiport models. The test vehicle by which we demonstrate the proposed approach is a commercial IC Flash memory designed for stacked System-in-Package (SiP) applications. This is a 512Mb NOR device in 90nm technology produced by Numonyx.

Manuscript received …; revised …

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II. Statement of the Problem

In order to discuss the modeling of IC core power delivery networks, we focus on stacked SiP devices. These devices are composed of a number of silicon dies encapsulated within the same package and connected through bonding wires to the package pads as shown in the example structure of Fig. 1. For these structures, a single model accounting for the combined effects of the power delivery network and of the package interconnects as seen from the VDD-VSS balls of the package is scarcely useful for the designer, who is looking for the maximum flexibility in combining different modules and assessing the impact of several available packages. In addition, package models, possibly including the mutual effects among the balls, are customarily available from suppliers or can be obtained via 3D-EM simulations or measurements. Therefore, in this paper, we decompose the stacked device into elementary units and we separately model each element.

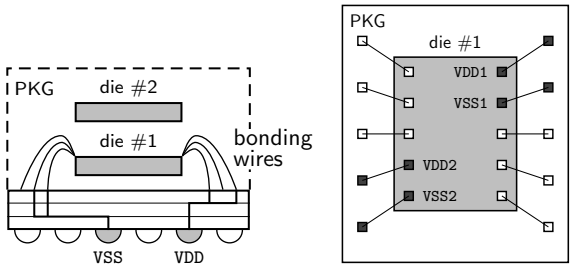

Fig. 1. Typical structure of a stacked system encapsulated in a single package (left panel: side view; right panel; top view). The core power delivery network of the die #1 is represented by the multiport structure defined by the VDD1 − VSS1 and VDD2 − VSS2 pairs of pads.

The generation of a model for the power delivery network of die #1 of Fig. 1 amounts to defining a suitable relation between the voltages and currents at the two ports defined by terminals VDD1 − VSS1 and VDD2 − VSS2. Under the assumption that the power delivery network being modeled behaves linearly, the relation can be expressed by a set of network functions. We adopt an admittance representation, relating voltages and currents as follows:

$$\begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} = \mathbf{Y}(s) \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} + \begin{bmatrix} A_1(s) \\ A_2(s) \end{bmatrix} \quad (1)$$

where $\mathbf{Y}(s)$ is the admittance matrix in the Laplace s-domain; $A_1(s)$ and $A_2(s)$ represent the non-autonomous responses of the system and account for the switching activity of the system itself. The circuit equivalent of (1) is shown in Fig. 2 and is used to represent the modeled power delivery network.

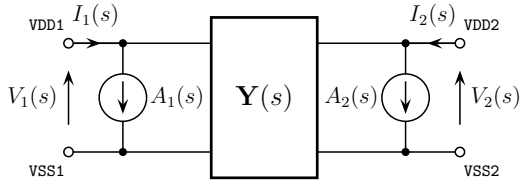

Fig. 2. Multiport Norton equivalent of the power supply network of the die #1 of Fig. 1.

III. Modeling Procedure

This Section summarizes the procedure for the estimation of the Norton model of the core power supply network of a digital circuit like the die #1 of Fig. 1 and addresses possible difficulties in the computation of model parameters.

A. Short-circuit admittance matrix $\mathbf{Y}(s)$

The estimation of the admittance matrix $\mathbf{Y}(s)$ is obtained from the scattering frequency-domain measurements of the multiport structure of Fig. 1. It is worth noticing that the on-chip probing, when available, is the best option to collect measured data that can be readily converted into the admittance representation (an example of such test strategy is available in [3], where partial results are available for the same test vehicle considered in this study). On the other hand, when the spacing of the supply pads does not allow for the on-chip probing or the number of ports exceeds the number of RF probes that can be used simultaneously with a probing station (generally limited to a few units), the off-chip measurement is the only available option. In the latter case, the die must be encapsulated in a custom package or directly mounted on a board with the bonding wires connecting the die pads to the board traces. In this case, however, the computation of the admittance matrix of the power network of the die requires special care to de-embed the effects of the test fixture.

It goes without saying that the measurements do not directly provide a computational model that can be used in a simulation environment like SPICE. Experience, supported also by the evidence that the die is electrically small, teach us that the interpretation of (1) and its conversion into an equivalent circuit is rather straightforward. As an example, the results collected in [3] confirm a smooth behavior of the entries of the admittance matrix $\mathbf{Y}$ in a frequency range up to 10GHz, that covers the next generation ICs and justifies the modeling via lumped simplified equivalents.

B. Short-circuit current sources

The computation of the current sources A_1 and A_2 of Fig. 2 is the most critical step of the modeling process and special care must be taken in collecting, interpretating and processing the measured data.

From a theoretical point of view, the determination of the A_k terms would require the measurement of the currents flowing through ideal short-circuits terminating the die pads (e.g., the `VDD1` and `VSS1` pads on the right panel of Fig. 1). However, in practice, the pads cannot be shorted and the circuit operation of the die must be ensured with the device mounted on a test board. Hence, the activity current can be measured on the board only, *i.e.*, after it has gone through the bonding wires and some board wiring. Figure 3 shows the equivalent circuit of the setup for the measurement of the activity current $i_{ss}(t)$. This setup is representative for a die mounted on a board with the bonding wires connecting the die pads with the PCB traces on the board. For the sake of simplicity, the die is described by a two-terminal Norton equivalent and the external power supply provided by a voltage regulator and a possible shunt capacitance is simply represented by the ideal battery V_{dd}. For the example memory chip of this study, typical values of C (representing the capacitive behavior of the power network) are in the range [1-10] nF, as outlined in [3]. On the other hand, the dominant inductive effects of the two adjacent bonding wires is represented by the loop inductance L conventionally attributed in half to each of the bonding wires (see Fig. 3) [4], [5]. In the simulations of the following Sections, we adopt $C = 3\,\text{nF}$ and $L = 4\,\text{nH}$.

The transient current $i_{ss}(t)$ is obtained via an indirect measurement of the voltage drop across the $R = 1\,\Omega$ resistor of Fig. 3. This method, following the standard for the measurement of the conducted emission of ICs in the range from dc to 1GHz [6], has been selected among a limited number of possible alternative techniques, since it is simple to implement and leads to accurate results in practical applications [7].

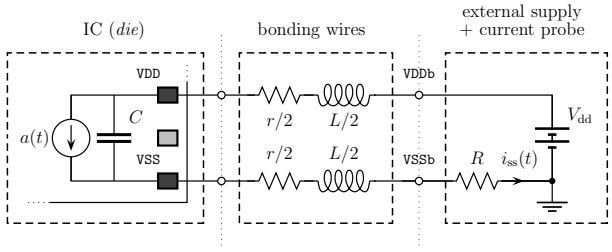

Fig. 3. Simplified equivalent of the setup used for the measurement of the core power supply current of a digital IC. Current is indirectly measured through the voltage drop on the series resistor $R = 1\,\Omega$.

The reconstruction of the source term $a(t)$ from the transient current measurement $i_{ss}(t)$ is theoretically obtained in the Laplace-domain by means of the backward application of the current division rule (see Fig. 3):

$$\begin{aligned} A(s) &= I_{ss}(s)H^{-1}(s) = \\ &= I_{ss}(s)(LC)(s^2 + s(r+R)/L + 1/LC). \end{aligned} \quad (2)$$

This operation, however, is ill-conditioned because of the high-pass filtering behavior of the network external to the die, as evidenced by the H^{-1} plot of Fig. 4. Thus, the net effect is an amplification of the high-frequency noise of the measured $i_{ss}(t)$ signal, leading to an $a(t)$ waveshape severely plagued by the noise. A detailed discussion of the inherent limitations of the inversion procedure of (2) is presented in Appendix A, where this argument is supported by a set of numerical simulations based on the ideal structure of Fig. 3.

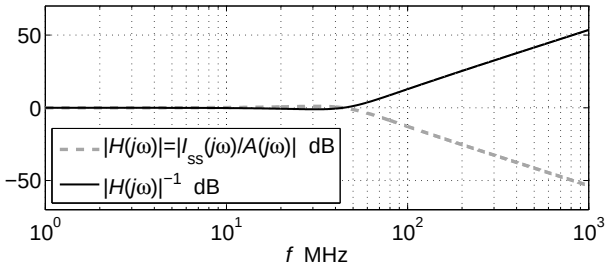

Fig. 4. Bode plots (magnitude) of the transfer functions $H(s) = I_{\rm ss}(s)/A(s)$ and its inverse $H^{-1}(s)$.

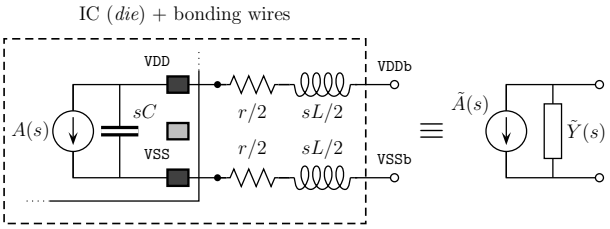

Fig. 5. Proposed Norton equivalent that accounts for the effects of both the die and the bonding wires.

In order to overcome this problem, we propose a new model for the device, including the effect of the bonding wires. This amounts to build a Norton equivalent of the part of the circuit to the left of port VDDb-VSSb in Fig. 3. As shown in the scheme of Fig. 5, the two elements of this new equivalent are the parallel admittance $\tilde{Y}(s) = (1/sC + r + sL)^{-1}$ and the short-circuit current $\tilde{A}(s) = A(s)\tilde{H}(s) = (A(s)/sC)/(1/sC + r + sL)$, that corresponds to the current flowing through an ideal short-circuit connecting the terminals VDDb and VSSb. With the help of (2), we can readily express the new Norton source in terms of the measured current, *i.e.*,

$$\begin{aligned}\tilde{A}(s) &= A(s)\tilde{H}(s) = (I_{ss}(s)H^{-1}(s))\tilde{H}(s) = \\ &\quad I_{ss}(s)\frac{s^2 + s(r+R)/L + 1/LC}{s^2 + sr/L + 1/LC} \end{aligned} \tag{3}$$

where $\tilde{H}(s) = \tilde{A}(s)/A(s)$.

Equation (3) turns out to be much more robust to measurement noise, since the combined transfer function $H^{-1}(s)\tilde{H}(s)$ is unitary at high-frequency and does not amplify the measurement noise. The reader is referred to Appendix A for additional details and for a quantitative justification of the previous claim. It is worth noticing that this solution does not limit the application of the extracted model, since, for any practical application, the die will be connected to the package traces via bonding wires as shown in Fig. 1

The proposed procedure can be easily extended to the multiterminal case, like the two-port structure in Fig. 2, by means of current measurements at the terminal pads, as shown in Appendix B. Briefly speaking, this can be achieved as follows: the test setup of Fig. 3 is suitably modified by replacing the two terminal Norton equivalent of the IC core with a multiterminal equivalent obtained by replicating at each port the SMD probing resistor (see Fig. 13). With this modification, the matrix equation obtained form the computation of the measured port currents turns out to be an extension of (2-3), thus allowing the reconstruction of the different source terms with the same robustness to high frequency noise of the scalar case.

C. Model generalization

In a real application, the bonding wires might be different from those used for the measurement of the switching current. Hence, the device model needs to be rescaled with respect to the parameters of the actual case in use. In analogy with (3), the actual Norton equivalent becomes:

$$\begin{cases} \tilde{A}(s) = I_{ss}(s)(L/\tilde{L})\dfrac{s^2 + s(r+R)/L + 1/LC}{s^2 + s\tilde{r}/\tilde{L} + 1/\tilde{L}C} \\ \tilde{Y}(s) = (1/sC + \tilde{r} + s\tilde{L})^{-1} \end{cases} \tag{4}$$

where the series resistance $\tilde{r}$ and inductance $\tilde{L}$ of the actual bonding wires need to be known independently. In general, the designer is able to estimate these parasitics by means of empirical considerations or via EM simulation. Model (4) represents a useful building block for a designer needing to assess integration scenarios for the device or conduct performance analyses at multichip level.

IV. Measurements results

This Section collects the results of the real measurements carried out on the example memory chip mentioned at the end of Sec. I. The Norton equivalent of the die power network, including standard bonding, is also identified.

In order to implement the ideal setup of Fig. 3, a test board has been suitably designed. The board, shown in Fig. 6, is composed of a general-purpose control circuitry for the operation of the device under test, and of a measurement board holding the IC under test and the measurement fixture. The measurement board is connected to the control board via a pair of 40-pin QTE connectors, and can be replaced to test different ICs. The memory controller has been designed to allow the memory to operate at 66MHz and perform repeatedly the basic cycles (*Program, Erase, Read*).

The ad-hoc measurement board contains also a female SMA connector close to the VSS reference pads (see Fig. 6). Such connector is used for the inclusion of the 1-Ω probe, mounted on a male SMA connector and designed according to the guidelines of [6]. The indirect measurement of the switching current via the voltage drop on the series resistor was carried

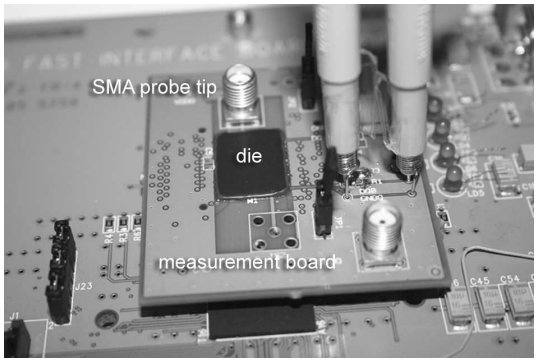

Fig. 6. Measurement board for recording the core switching activity current for the example IC.

out with a LeCroy WavePro 7300A scope (3GHz bandwidth, 10GS/s). Preliminary measurement results can be found in [8].

Figure 7 shows a slice of the measured transient current $i_{\rm ss}(t)$ observed during the erase operation phase and its frequency-domain spectrum, thus confirming the same behavior observed in the simplified analysis of Appendix A.

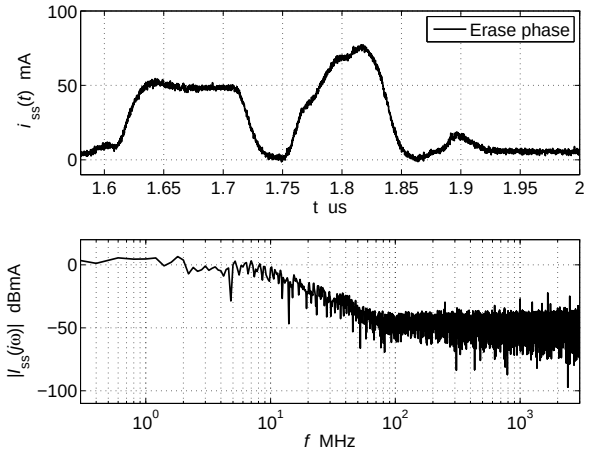

Fig. 7. Measured transient current $i_{\rm ss}(t)$ carried out on the example commercial memory chip (top panel) and its related spectrum (bottom panel).

The SMA connector of Fig. 6 has also been used to measure the S_{11} scattering parameter needed for the computation of the equivalent admittance seen from the terminals of the resistor and therefore for the estimation of the setup capacitance C and inductance L (see Fig. 3). Figure 8 shows the measured frequency-domain admittance compared with the response predicted by the LC circuit equivalent of Fig. 3. The values of the circuit equivalent were estimated via simple fitting.

As outlined in Sec. III, the measured current response $i_{ss}(t)$ of Fig. 7 is used to compute the Norton current source $\tilde{a}(t)$ via equation (3). The measured response and the estimated short-circuit current are shown in Fig. 9, that confirms the feasibility and robustness of the proposed approach.

It is worth noticing that the test board specifically designed in this study allowed the estimation of one transient current only, and therefore the estimation of a single-port Norton equivalent. However, the advocated processing technique can

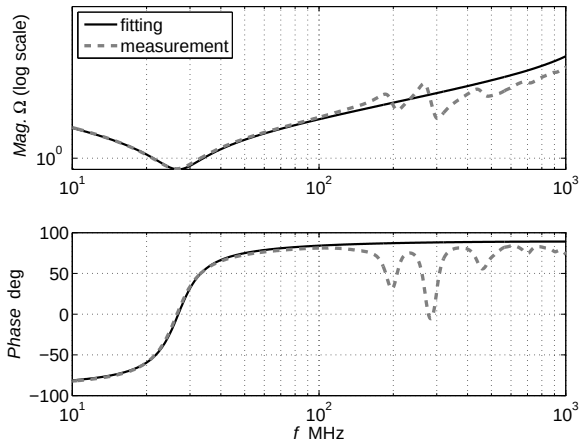

Fig. 8. Impedance seen from the terminals of the $1\,\Omega$ resistor of Fig. 3. Dashed lines: real measurement carried out on the test board of Fig. 6; solid lines: prediction obtained via a lumped LC equivalent like the one of Fig. 3 ($L = 7nH$, $C = 3.5\,nH$).

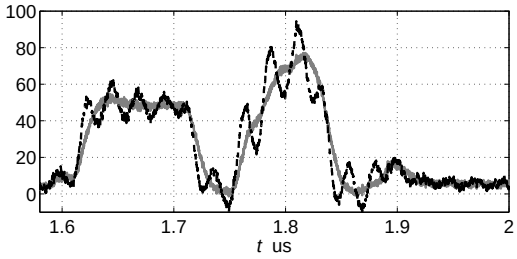

Fig. 9. Measured transient current $i_{\rm ss}(t)$ of Fig. 7 (solid gray curve) and short-circuit current $\tilde{a}(t)$ of the Norton equivalent computed via equation (3) (dashed black curve)

be extended to an arbitrary number of ports and is consequently suited for the estimation of a multiport Norton equivalent.

V. Conclusions

This paper addresses the generation of a black-box model of the core power delivery network of a digital IC. The proposed model, that is defined by a multiport Norton equivalent, can be obtained from measurements carried out at the IC ports. The effects of the measurement noise, that introduces practical constraints in the computation of the source terms of the equivalent, has been demonstrated. A systematic procedure enabling the estimation of a simplified yet representative model including the bonding wires of the device, has been proposed. The feasibility of the advocated approach has been demonstrated through the modeling of a commercial IC memory from data measured by means of a specifically-designed test board.

Acknowledgements

This paper provides a systematic and unified interpretation of several activities carried out under the MOCHA (MOdeling and CHAracterization for SiP - Signal and Power Integrity Analysis) grant no. 216732 of the European Communitys Seventh Framework Programme. A. Girardi, R. Izzi, A. Vigilante and F. Vitale (Numonyx,

Italy) are gratefully acknowledged for providing the example test chip and the support for the design of the test board used in this study.

APPENDIX A

The aim of this appendix is twofold, *i.e.*, to clarify via numerical simulation the difficulties in the reconstruction of the short-circuit current $a(t)$ from the measured current activity of the chip (see eq. (2)); also, to demonstrate the robustness of (3) and (4) for the prediction of the short-circuit current of a new Norton model of the IC supply network, built including standard bonding wires.

Experience teaches us that the power supply current drawn by a digital memory is a superposition of a fast switching activity of the internal gates and of a slower current absorption corresponding to the enable/disable function of internal macro-blocks [8]. Therefore, the signal $a(t)$ of Fig. 3 can be idealized by a square wave modulating a combination of current spikes (please refer to the dark curve of the top panel of Fig. 10).

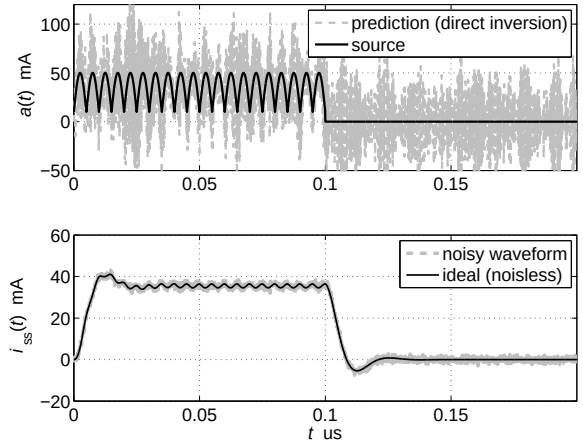

Fig. 10. Transient waveform of the current source $a(t)$ defining the switching activity of the example test (top panel) and the corresponding supply current $i_{\rm ss}(t)$ that is possibly corrupted by a superimposed simulated *measurement noise* (the standard deviation of the white noise disturbance is $\sigma = 1\,\mathrm{mA}$) (bottom panel).

The lower panel of Fig. 10 shows the *virtually measured* current response $i_{\rm ss}(t)$, corresponding to $a(t)$ in the upper panel. The "measured" current is contaminated by a white gaussian noise to mimic a real measurement situation. The top panel of Fig. 10, in addition, includes the reconstructed short-circuit current obtained from the direct application of (2) to the noisy response of $i_{ss}(t)$, thus highlighting the severe degradation of the predicted waveform through the processing of noisy data. This phenomenon is described from a different point of view in Fig. 11, where the spectrum of the transient current $i_{\rm ss}(t)$ is shown for both the noiseless and the noisy case. The two plots of Fig. 11 clearly highlight that the noise in a real measurement modifies the behavior of the spectrum in the high-frequency region, *i.e.*, from about 100 MHz. The application of (2) means to multiply the noisy spectrum of Fig. 11 by the inverse transfer function $H^{-1}(s)$ (see its Bode plot in Fig. 4), and this operation unavoidably leads to the amplification of the measurement noise, preventing the direct computation of the current source $a(t)$.

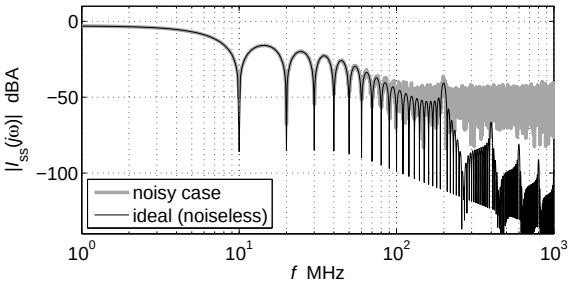

Fig. 11. Frequency-domain spectrum of the $i_{\rm ss}(t)$ current.

In order to overcome this problem, as already anticipated in Sec. III, we propose the generation of a new Norton equivalent including the effects of the bonding wires. As an example, the top panel of Fig. 12 shows the predicted short-circuit current of the new Norton equivalent of the die including the bonding of Fig. 3. In this case, the noisy signal $i_{ss}(t)$ is processed by means of (3), *i.e.*, it is transformed by the network function $H^{-1}(s)\tilde{H}(s)$ shown in the bottom panel of Fig. 12, featuring a flat response in the high-frequency region.

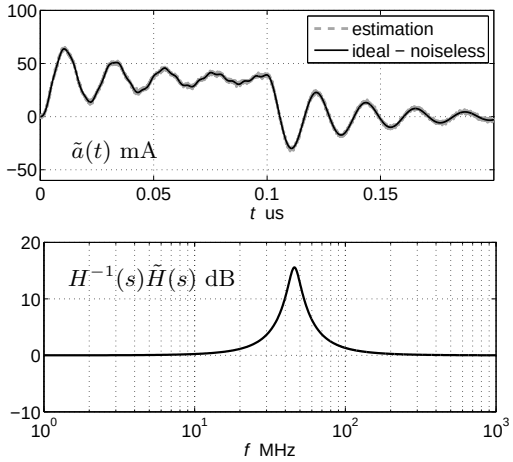

Fig. 12. Top panel: short-circuit current $\tilde{a}(t)$ of the new Norton equivalent including standard bonding ($r = 100\,\mathrm{m\Omega}$, $L = 4\,\mathrm{nH}$); bottom panel: Bode plot (magnitude) of the transfer functions $H^{-1}(s)\tilde{H}(s)$ defined in (3).

In the above assessment, no filtering has been applied to the noisy signal $i_{ss}(t)$, in order to demonstrate the robustness of the estimation via (3). Also, it is ought to note that typical values of the bonding inductance L are always within the range $1 \div 10\,\mathrm{nH}$, leading to a transfer function (3) that modifies the measured current $i_{ss}(t)$ in a frequency region where the signal-to-noise ratio of the measurements is certainly larger than one. This demonstrates the general validity of the inversion procedure and confirms that similar results are obtained when (4) is used with different values of the bonding parameters

As a final remark, we wish to point out that a careful design or characterization of the current probe (*i.e.*, of the $1\,\Omega$ resistor R in Fig. 3) is not required, since the bandwidth of the measured current is relatively small with respect to

frequencies where SMD parasitics can have effects; hence, the SMD resistor can be assumed as an ideal component.

APPENDIX B

This Appendix shows the extension of the proposed methodology for the multiport case. A two-port case is considered for the sake of simplicity, and the equivalent of Fig. 3 is generalized to the equivalent of Fig. 13, where the bonding resistances have been omitted for simplicity and I_{ss1}, I_{ss2} represent the currents flowing out of the power supply terminals of a die with two VDD-VSS supply pairs.

The measured currents can be obtained from

$$\begin{cases} \begin{bmatrix} I_{ss1}(s) \\ I_{ss2}(s) \end{bmatrix} &= \mathbf{Y}(s) \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} + \begin{bmatrix} A_1(s) \\ A_2(s) \end{bmatrix} \\ \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} &= -\begin{bmatrix} R+sL & 0 \\ 0 & R+sL \end{bmatrix} \begin{bmatrix} I_{ss1}(s) \\ I_{ss2}(s) \end{bmatrix} \\ &= -\mathrm{diag}(R+sL) \begin{bmatrix} I_{ss1}(s) \\ I_{ss2}(s) \end{bmatrix} \end{cases} \tag{5}$$

where the first equation represents the die and the second equation is the series connection of the bonding impedances with the two-terminal probing elements.

Equations (5) can be rewritten as

$$\begin{bmatrix} I_{ss1}(s) \\ I_{ss2}(s) \end{bmatrix} (\mathbf{I} + \mathbf{Y}(s)\mathrm{diag}(R+sL)) = \begin{bmatrix} A_1(s) \\ A_2(s) \end{bmatrix}. \tag{6}$$

A similar equation arises when the two-terminal probing elements of Fig. 13 are replaced by ideal short circuits. In the latter case, the short circuit currents write

$$\begin{bmatrix} \tilde{A}_1(s) \\ \tilde{A}_2(s) \end{bmatrix} (\mathbf{I} + \mathbf{Y}(s)\mathrm{diag}(sL)) = \begin{bmatrix} A_1(s) \\ A_2(s) \end{bmatrix}. \tag{7}$$

Finally, the combination of (6) with (7) allows to compute the short circuit currents $\tilde{A}_1$ and $\tilde{A}_2$ of the multiport equivalent of the IC (see Fig. 13), including the bonding wires. The equivalent source currents are determined as functions of the measured currents I_{ss1} and I_{ss2}. As already outlined in Sec. III-B, the obtained equation turns out to be robust to measurement noise and can be effectively used to process measured data.

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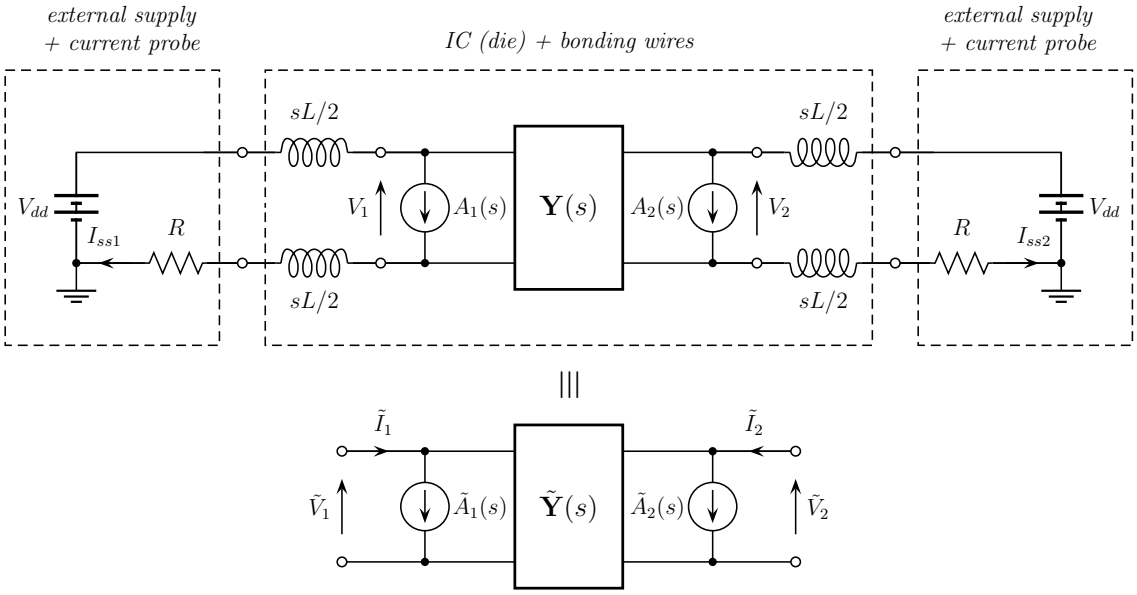

Fig. 13. Simplified equivalent of the setup for the measurement of the core power supply currents of a digital IC with two VDD-VSS power supply pairs. Currents are indirectly measured through the voltage drop on the series resistors $R = 1\,\Omega$.