A New Filtering Technique for Increasing the Immunity of Power Transistors to RFI

A New Filtering Technique for Increasing the Immunity of Power Transistors to RFI

Calogero Bona #, Franco Fiori *

EMC Competence Center ,Istituto Superiore M. Boella, Via P. C. Boggio, Turin, Italy
* *Microelectronics EMC Group, Eln. Dpt., Politecnico di Torino C.so Duca degli Abruzzi 24, Turin, Italy*
bona@ismb.it, franco.fiori@polito.it

***Abstract*—The paper deals with the susceptibility of MOS power transistors to electromagnetic interference. The case of providing electric energy to a power load by means of a MOS power transistor connected in the low-side configuration is considered and radio-frequency interference is superimposed to the drain-source nominal voltage.**
The causes that lead to switch-on a power transistor driven to be switched-off (and viceversa) are highlighted and a new filtering circuit, which is inserted in the power transistor input loop, is shown. The effectiveness of the proposed filtering technique is proved by computer simulations and experimental test results.

I. INTRODUCTION

In the last decades, the wide diffusion of wireless systems in almost any field of human life has strongly increased the level of electromagnetic pollution and as a consequence, the concern to make electronic modules immune to such electromagnetic interference has constantly grown with time. Although such kind of problems are usually solved using proper EMI filters and shields, the constant need for reducing costs has boosted the researches to make integrated circuits intrinsically immune to EMI [1]. Some investigations have been focused on the susceptibility to EMI of analog circuits like operational amplifiers [2] and some other have dealt with EMI-induced upset in digital front-ends and in single transistors [3] [4] [5]. Recently, the effect of RFI on the operation of an high-side power transistors have been discussed in [6] while a similar analysis has been carried out in [7] for the low-side configuration with RFI superimposed to the drain-source nominal voltage. In fact, the operation of switching power transistors can be affected by EMI because cables, that connect transistors to the power loads, behave like unintentional antennas conveying EM disturbance to the drain and source terminals. As a result, a transistor, which is driven at the gate-source port to be switched-off, can be switched-on by RFI, resulting in unexpected failures. Such unwanted effects can be experienced when RFI added to the gate-source voltage through the drain-to-gate parasitic coupling takes amplitude such that the transistor can be alternatively switched-on and switched-off. Due to this phenomenon a DC current is made flowing through the power load even if the power transistor is driven to be switched-off. This unwanted effect can lead to operation failures, that would be extremely dangerous if it take place in safety-related electronic units like those of automotive, avionic and industrial applications.

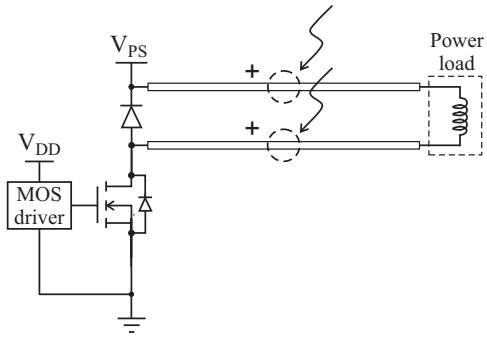

Fig. 1. Low side topology with power trasistor and inductive load connected through cables

In this work the causes leading to the RFI-driven power MOS switching are investigated and, based on that, a new filtering technique that involves the power transistor input port is proposed. To this purpose, Section II introduces a small-signal equivalent circuit of the power transistor, which leads to identify the parameters that influence the power transistor susceptibility to RFI. On the basis of this analysis a new method for filtering the RFI added to the drain source terminals of the power transistor is proposed in Section III. Finally, some concluding remarks are drawn in Section IV.

II. ANALYSIS OF THE MOS POWER TRANSISTOR SUSCEPTIBILITY TO EMI

As mentioned in the introduction, EM disturbance conveyed by harnesses and affecting the output port of a power MOS transistor can leads to potential failures. The considered problem can be investigated by means of Bulk Current Injection (BCI) test, measuring the induced common mode current in the cables connecting the switching transistor to the power load, which causes such a failure. Alternatively the EM susceptibility of the device can be analyzed by means of Direct Power Injection (DPI) test, directly injecting a disturbance into the violated drain terminal and characterizing the susceptibility in terms of the incident power of the EM disturbance causing the failure.

Hence, in this work the standardized IEC 62132-4 DPI test method [8] has been considered; the power transistor has

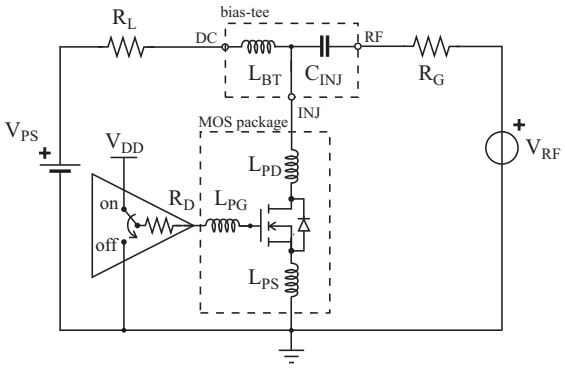

Fig. 2. Direct Power Injection test circuit

been connected in the low-side (LS) configuration and the RFI has been superimposed to the drain-to-source nominal voltage through a bias tee as shown in Fig.2.

In what follows, analyses are carried out referring to the cases of the power transistor steadily switched-off or switched-on while the effect of RFI on the power transistor while switching has not been considered and it will be investigated in the future.

The problem of analyzing RFI-induced transistor switching involves non-linear phenomena hence, in principle, such investigations cannot be based on the small-signal assumption. Actually, as long as the magnitude of the gate-source induced fluctuation voltage is lower than the transistor threshold ($V_{\rm TH}$) the output state transition does not take place, hence the constant-parameter small-signal equivalent circuit of power transistors can be used. In [7] the use of the small-signal analysis to find out the frequency ranges in which the transistor is switched-on (off) by RFI has been proved to be effective.

As a consequence, in the remainder of the paper susceptibility analyses are carried out referring to small-signal equivalent circuits. In particular, the magnitude of the RFI that potentially make the power-transistor switching can be evaluated referring to small-signal equivalent circuits and looking for the magnitude of the drain-source RF voltage that gives rise to gate-source RF voltage with magnitude equal or greater to the transistor threshold ($V_{\rm TH}$). To this purpose, the small-signal equivalent circuit of the power transistor switched-off (Fig.3.a) and switched-on (Fig.3.b) have been considered, and they have been employed in the small signal analysis of the circuit in Fig.2. To this purpose, the simplified package model including only the dominant components (bonding wire parasitic elements) are considered by means of the series inductances $L_{\rm PX}$. Then, the gate driver is described by its Thevenin equivalent circuit while the drain DC bias network (biasing inductor and loading resistance ($R_{\rm L}$)) has been modeled referring to the small-signal equivalent circuit of each component over a wide frequency range.

Once defined the small signal equivalent circuits of the power transistor and the equivalent circuit of the Direct Power Injection test setup including the package parasitics, the transfer function $V_{\rm GS}(s)/V_{\rm RF}(s)$ (see Fig. 2) has been

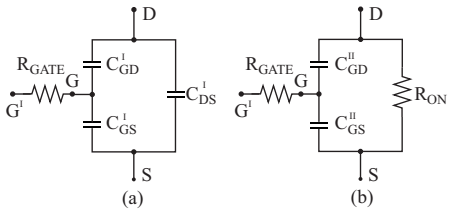

Fig. 3. Power MOS small signal models in the *off* region (a) and in the *triode* region (b)

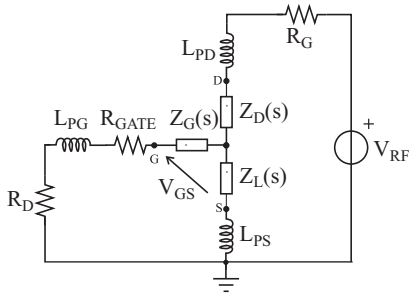

Fig. 4. Small signal equivalent circuit of the test setup circuits shown in Fig. 2

obtained in order to investigate the parasitic coupling between the drain-source and the gate-source ports. To this purpose, the small signal equivalent circuit depicted in Fig. 4 has been considered. In such circuit the Y-Δ transform has been applied to the power MOS model of Fig. 3 and the expression of the impedances $Z_{\rm G}(s)$, $Z_{\rm D}(s)$ and $Z_{\rm S}(s)$ will be given in the following since they depend on the considered operating region of the power transistor. Finally the obtained transfer function is:

$$\frac{V_{\rm GS}(s)}{V_{\rm RF}(s)} = \frac{Z_{\rm S}(s)A(s) - Z_{\rm G}(s)B(s)}{[Z_{\rm G}(s)+A(s)]\,[Z_{\rm S}(s)+B(s)] + \\ + [Z_{\rm G}(s)+Z_{\rm S}(s)+C(s)]\,[Z_{\rm D}(s)+D(s)]} \quad (1)$$

where

$$A(s) = sL_{\rm PG} + (R_{\rm D} + R_{\rm GATE})$$
$$B(s) = sL_{\rm PS}$$
$$C(s) = s(L_{\rm PG} + L_{\rm PS}) + (R_{\rm D} + R_{\rm GATE})$$
$$D(s) = sL_{\rm PD} + R_{\rm G}$$

A. Power MOS driven in the off-state

In order to analyze the susceptibility of the switched-off power MOS transistor the transfer function of the gate to source voltage with respect to the drain injected RF disturbance has been found referring to the power transistor driven in the off-state. To this purpose the Y-Δ transform has been applied to the small-signal equivalent model in Fig.3.(a) obtaining the impedance expressions of Fig.4 and referred in (1):

$$Z_{\rm G}(s) = \frac{1}{sC_{\rm G}}; \quad C_{\rm G} = \frac{C_{\rm GD}C_{\rm DS} + C_{\rm GD}C_{\rm GS} + C_{\rm GS}C_{\rm DS}}{C_{\rm DS}} \tag{2}$$

$$Z_{\rm D}(s) = \frac{1}{sC_{\rm D}}; \quad C_{\rm D} = \frac{C_{\rm GD}C_{\rm DS} + C_{\rm GD}C_{\rm GS} + C_{\rm GS}C_{\rm DS}}{C_{\rm GS}} \tag{3}$$

$$Z_{\rm S}(s) = \frac{1}{sC_{\rm S}}; \quad C_{\rm S} = \frac{C_{\rm GD}C_{\rm DS} + C_{\rm GD}C_{\rm GS} + C_{\rm GS}C_{\rm DS}}{C_{\rm GD}} \tag{4}$$

From the expression of the transfer function in (1) it turns out that a proper combination of the complex impedances $A(s)$ and $B(s)$ could neglect the function numerator making the switched-off transistor immune to the drain injected RFI. In fact the numerator of (1) can be written in function of the real parts ($A_{\rm R}$ and $B_{\rm R}$) and the imaginary parts ($A_{\rm I}$ and $B_{\rm I}$) of the impedances $A(s)$ and $B(s)$, and substituting the expressions (2) and (4) it is obtained:

$$\begin{aligned} &Z_{\rm S}(s)A(s) - Z_{\rm G}(s)B(s) = \\ &= \frac{1}{j\omega C_{\rm S}}\left(A_{\rm R} + jA_{\rm I}\right) - \frac{1}{j\omega C_{\rm G}}\left(B_{\rm R} + jB_{\rm I}\right) = \\ &= \left(\frac{A_{\rm I}}{\omega C_{\rm S}} - \frac{B_{\rm I}}{\omega C_{\rm G}}\right) - j\left(\frac{A_{\rm R}}{\omega C_{\rm S}} - \frac{B_{\rm R}}{\omega C_{\rm G}}\right) \end{aligned}$$

It follows that the numerator transfer function is neglected if the following conditions are satisfied:

$$B_{\rm R} = A_{\rm R}\frac{C_{\rm G}}{C_{\rm S}}; \quad B_{\rm I} = A_{\rm I}\frac{C_{\rm G}}{C_{\rm S}}; \tag{5}$$

Hence in turns out that in order to reduce as much as possible the RF gate-source voltage magnitude both the gate and source series impedances need an imaginary part (inductive component) and a real part (resistive component). This solution is synthesized in Fig.5, where external inductances ($L_{\rm G}$ and $L_{\rm S}$) and resistor ($R_{\rm S}$) have been added to meet the constraints (5). The inductor $L_{\rm BP}$ has been inserted to shunt the DC current avoiding it to flow through the resistor $R_{\rm S}$ and the inductor $L_{\rm S}$.

Applying (5), (2) and (4) the design rules for the added passive components are found to be:

$$R_{\rm S} = \left(R_{\rm D} + R_{\rm GATE}\right)\frac{C_{\rm GD}}{C_{\rm DS}} \tag{6}$$

$$L_{\rm S} = \left(L_{\rm G} + L_{\rm PG}\right)\frac{C_{\rm GD}}{C_{\rm DS}} - L_{\rm PS} \tag{7}$$

$$L_{\rm BP} = \frac{R_{\rm S}}{2\pi f_{\rm ps}} - L_{\rm S} \tag{8}$$

where $f_{\rm ps}$ is the pole frequency of the impedance constituted by the series $R_{\rm S}$ and $L_{\rm S}$ parallel connected with $L_{\rm BP}$. It has to be noticed that $L_{\rm BP}$ makes the proposed solution frequency dependent and in particular applying (6), (7) and (8) the constraints (5) are satisfied in the frequency band above $f_{\rm ps}$.

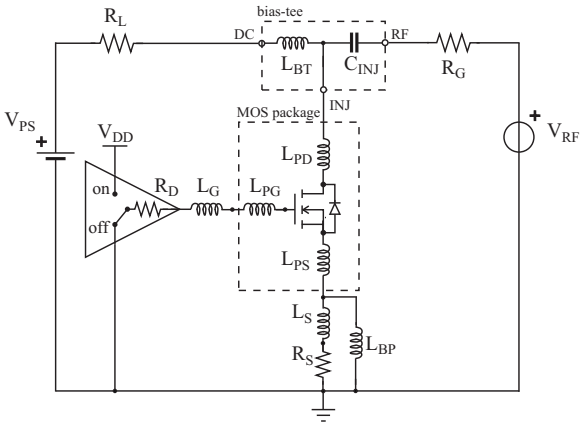

Fig. 5. Proposed circuital solution immune to the RFI added to the drain-source terminals

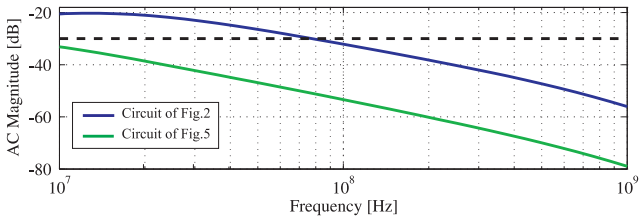

Fig. 6. AC simulation results with the power MOS biased in the *off* region. Transfer functions $\frac{V_{\rm GS}(f)}{V_{\rm RF}(f)}$

The susceptibility of the switched-off MOS transistor of circuit in Fig. 2 and the effectiveness of rules (6), (7) and (8) has been initially verified by mean of AC simulations which results are shown in Fig. 6. In particular the $V_{\rm GS}/V_{\rm RF}$ transfer function referring to the circuit in Fig.2, obtained switching-off the power transistor by means of $R_{\rm D} = 22\Omega$ and considering the parasitic inductances $L_{\rm PX} = 2nH$, are compared with the transfer function of the proposed circuit of Fig. 5. In the considered example the parasitic gate impedance $R_{\rm GATE}$ is 1.7Ω and the $C_{\rm GD}/C_{\rm DS}$ ratio is 0.75; hence the values of the passive components has been found rounding the results of (6), (7) and (8) to the nearest discrete standard value obtaining $L_{\rm G} = 22nH$, $L_{\rm S} = 15nH$, $R_{\rm S} = 15\Omega$, and $L_{\rm BP} = 1\mu H$ for $f_{\rm ps} = 2.5MHz$. In the same figure, the simulation results can be compared with the reference level of -30dB, that comes out for an input RFI with amplitude of 25V and transistor conduction threshold of 0.75V.

From such small-signal analysis comparison it turns out that, in the considered frequency band, the proposed solution results immune to the injected RF disturbance while the circuit in Fig. 2 is susceptible in the frequency band up to 70MHz.

B. Power MOS driven in the triode region

Once verified by means of the proposed small-signal analysis that the switched-off power transistor in Fig. 2 is susceptible to the drain injected disturbances, and once proposed an immune circuital solution (Fig. 5), the susceptibility of the switched-on transistor in both circuits has been analyzed. To this purpose AC simulations has been performed on the

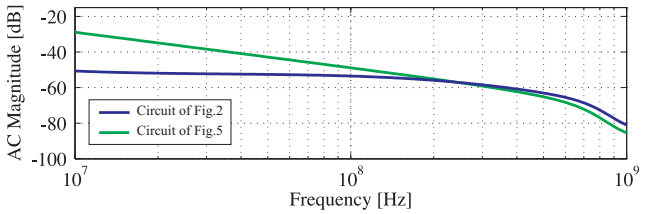

Fig. 7. AC simulation results with the power MOS biased in the *triode* region. Transfer functions $\frac{V_{\rm GS}(f)}{V_{\rm RF}(f)}$

considered circuits and the obtained $V_{\rm GS}$ transfer functions with respect to the injected signal $V_{\rm RF}$ are compared in Fig. 7.

From such comparison it turns out that, when the LS driver is biased in the triode region, a much greater gate-source voltage fluctuation is experimented in the proposed circuit of Fig. 5, but the maximum magnitude of the referring transfer function is -29dB meaning that an injected disturbance of 20V involves a $V_{\rm GS}$ fluctuation of $700mV$. Considering the worst case of a driver maximum output voltage of $3.3V$ the $0.75V$ conduction threshold will not be crossed by the voltage fluctuations. Overall, it can be concluded that a switched-on MOS power transistor can be difficultly switched-off by RFI, even in the proposed solution.

III. Validation

The proposed small-signal analysis method applied to the power transistor susceptibility and the circuital solution based on the obtained results, which makes the power MOS transistor immune to the drain injected RFI, have been validated by means of time domain simulations and experimental tests. Such tests have been performed referring to the schematic shown in Fig. 5 and the obtained susceptibility profiles are illustrated in Fig. 8, where simulation and experimental results are compared with those obtained referring to the susceptible circuit depicted in Fig. 2. In particular simulations has been performed using the Spectre simulator while the transistor model provided by the manufacturer and based on the MOS model Level 1 has been exploited.

Tests have been carried out in this way: once defined the frequency of the interfering signal, its amplitude has been increased step by step until a DC drain current of 1mA has been made flowing (susceptibility criterion). This procedure has been repeated for a set of interference frequency in the rage 10MHz-1GHz obtaining the results reported in Fig. 8. Furthermore, a maximum level of 32dBm for the incident power has been considered.

Time domain simulations and measurement results are in good agreement with the small-signal analysis confirming the validity of the proposed solution. In fact whereas both computer simulation and experimental results show the power transistor of the circuit in Fig.2 to be susceptible to the injected signal in the frequency band up to 70MHz, simulation results show that the solution proposed in Fig. 5 is immune to drain injected disturbances of power up to 32dBm and frequency band up to 1GHz. The mismatch between simulations and

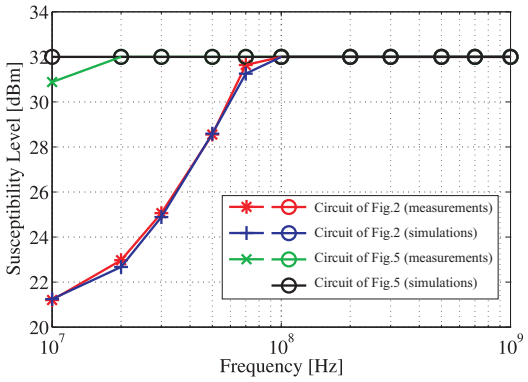

Fig. 8. Susceptibility. Level (ID = 1mA) obtained by simulations. The "o" markers point out that no failure occurred.

measurement results of the circuit in Fig. 5 which occurs at 10MHz is due to the tolerance of the discrete components; in fact increasing the nominal value of the inductance $L_{\rm BP}$ from $1\mu H$ to $1.5\mu H$ the proposed solution results to be immune in the frequency band from 10MHz to 1GHz even from experimental tests.

Finally similar simulations have been performed with the MOS biased in the *deep triode* region but no failure has been never observed, confirming the conclusions reported in Section II-B.

IV. Conclusions

In this paper a new filtering technique to increase the immunity of low-side power transistors to RFI superimposed to the drain-source port has been proposed. This filtering solution, which involves the power transistor parasitic elements, has been derived referring to the transfer functions that result from the small-signal equivalent circuit of the power circuit parasitic elements. The effectiveness of the proposed EMI filter has been proved through both time-domain computer simulation and experimental test results.

References

[1] M. Ramdani, E. Sicard, et Al., *The Electromagnetic Compatibility of Integrated Circuits - Past, Present and Future*, IEEE Trans. on EMC, vol.51, no.1, pp.78-1000, Feb. 2009

[2] F. Fiori, *Design of an Operational Amplifier Input Stage Immune to EMI*, IEEE Trans. on EMC, Vol. 49, no. 3, pp. 834-839, Aug. 2007

[3] C.E.Larson,J.M.Roe, *A Modified Ebers-Moll Transistor Model for RF-Interference Analysis*, IEEE Trans. on EMC, vol.21, no.4, pp.283-290, Feb. 1979

[4] Y. Hattori, H. Tadano, and H. Nagase, *A Study of dc Operating point Shifts in MOSFETs with Large RF Signals*, Electronics and Communications in Japan, vol. 84, pp. 2375-2383, Dec. 1999

[5] J. J. Laurin, S. G. Zaky, K. G. Balmain, *On the prediction of digital circuit susceptibility to radiated EMI*, IEEE Trans. on EMC, Vol. 37, no. 4, pp. 528-535, Nov. 1995

[6] O. Jovic, U. Stuermer, W. Wilkening, A. Baric and C. Maier, *Susceptibility of PMOS Transistors under High RF Exitations at Source Pin*, 20th International Zurich Symposium on EMC, pp. 401-404, Jan. 2009

[7] C. Bona, F. Fiori, *EMI Inducted Failures in DMOS Power Transistors*, International Conference on Electromagnetics in Advanced Applications, ICEAA 2009, pp.564-567

[8] IEC 62132-4:Integrated Circuits, Measurement of Electromagnetic Immunity - Part 4: *Direct RF Power Injection Method*.