New Stationary Frame Control Scheme for Three Phase PWM Rectifiers Under Unbalanced Voltage Dips Conditions

New Stationary Frame Control Scheme for Three-Phase PWM Rectifiers Under Unbalanced Voltage Dips Conditions

Daniel Roiu, Radu Iustin Bojoi, *Member, IEEE*, Leonardo Rodrigues Limongi, and Alberto Tenconi, *Member, IEEE*

***Abstract*—A new stationary frame control scheme for three-phase pulsewidth-modulation (PWM) rectifiers operating under unbalanced voltage dips conditions is proposed in this paper. The proposed control scheme regulates the instantaneous active power at the converter poles to minimize the harmonics of the input currents and the output voltage ripple. This paper's novelty is the development of a new current-reference generator implemented directly in stationary reference frame. This allows using proportional sinusoidal signal integrator (P-SSI) controllers for simultaneous compensation of both positive and negative current sequence components. No phase-locked loop (PLL) strategies and coordinate transformations are needed for the proposed current-reference generator. Experimental results are presented for a 20-kVA alternative current (ac)/direct current (dc) converter prototype to demonstrate the effectiveness of the proposed control scheme. A comparison with two other existing control techniques is also performed. Fast dynamic performance with small dc-link voltage ripple and input sinusoidal currents are obtained with this control scheme, even under severe voltage dips operating conditions.**

***Index Terms*—AC/DC converter, current-reference generator, voltage dips.**

I. Introduction

WHEN COMPARED with thyristor or diode rectifiers, the pulsewidth-modulation (PWM) ac/dc converter (Fig. 1) has some advantages, such as sinusoidal input current, smaller output filter capacitor, controllable power factor, and bidirectional power flow. However, the PWM rectifier is sensitive to voltage dips and input impedance unbalance. Voltage dips are considered the most severe disturbances for the industrial equipment [1]. They may frequently occur in three-phase power systems due to unbalanced power supply, unbalanced loads, and various faults. Under these conditions, it has been shown in the literature that even dc-link voltage harmonics and odd ac input currents harmonics will appear [2], [3], due to the negative sequence component of the unbalanced source voltage.

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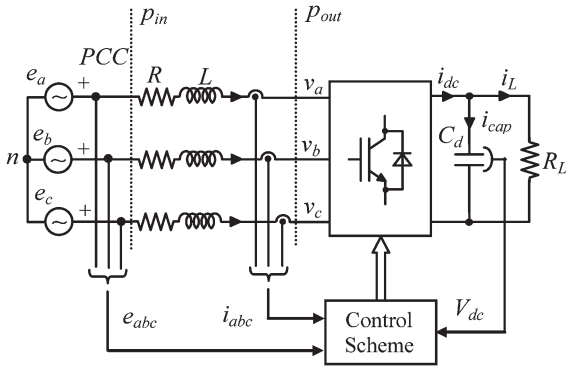

Fig. 1. Block diagram of the PWM ac/dc converter.

Different control schemes have been proposed in the literature to improve the performance of PWM rectifiers under unbalanced voltage supply conditions. Some interesting applications of these control schemes are: the fault ride-through capability of the variable speed wind power plants, adjustable speed drives using back-to-back converters and voltage-source-converter high-voltage dc transmissions [4]–[9].

One of the most used control strategies to minimize the input/output harmonics is the one that regulates the instantaneous active power at a constant value.

In [10]–[13], control schemes in both synchronous and stationary reference frames to regulate the instantaneous active power supplied from the ac source $p_{\rm in}$ (Fig. 1) under unbalanced input voltage conditions have been proposed. However, even with a constant active power $p_{\rm in}$, the instantaneous active power at the converter poles $p_{\rm out}$ (Fig. 1) is not constant since the power related to the ac input filter is neglected. For high-power applications, the impact of the interface reactors must be taken into account to eliminate the oscillations of the instantaneous active power. Consequently, a ripple-free dc-link voltage should be obtained.

A control scheme that includes the impact of instantaneous power of the ac inductors by regulating the instantaneous active power at the converter poles has been developed in [14], [15]. This method is more effective in harmonics elimination under unbalanced operating conditions when compared with the methods proposed in [10]–[13]. However, this method has the following two disadvantages: 1) the complexity of solving nonlinear equations in real time and 2) the low bandwidth of the current regulator due to the extraction of the sequence current components that introduces a delay in the current loop feedback.

To solve these problems, a control scheme using dual current regulators in a hybrid synchronous reference frame was proposed in [16] and [17]. This way, the extraction of the current sequence components has been eliminated. A simplified current-reference generator is also proposed, with the aim at eliminating the need of solving nonlinear equations in real time. Because of the existence in the reference signals of an oscillating part, a resonant gain in the current regulator was introduced. This scheme requires four separate proportional–integral (PI) sinusoidal signal integrator (SSI) current controllers implemented in positive negative synchronous reference frames (PNSRF). In addition, feedforward and decoupling terms have been used, resulting in a complex control scheme. Notch filters for filtering the oscillating part existing in the feedback and feedforward signals of current control loop were used in [18].

A control scheme with stationary frame proportional SSI (P-SSI) current controllers and a PI-SSI dc-link voltage controller with good result in reducing the dc-link voltage ripple was proposed in [19]. However, this solution has problems under voltage dips operation conditions since a nonzero third harmonic component in the ac input current will appear due to the current-reference generator. This component is proportional with the voltage dip severity.

This paper proposes a new stationary frame control scheme for three-phase PWM rectifiers under unbalanced voltage dips conditions. The proposed control scheme regulates the instantaneous active power at the converter poles $p_{\rm out}$ (considering the instantaneous power related to the ac inductors) for minimizing of input/output harmonics. The novelty consists of the development of a new current-reference generator implemented directly in stationary reference frame. This allows using P-SSIs controllers for simultaneous compensation of both positive and negative current sequence components. Consequently, a simplified control scheme is obtained when compared with existing solutions [16]. Furthermore, no phase-locked loop (PLL) strategies and rotational transformations are needed. Experimental results are presented for a 20-kVA ac/dc converter prototype to demonstrate the effectiveness of the proposed control scheme. A comparison with two other control techniques is also performed. Fast dynamic performance with very small dc-link voltage ripple and sinusoidal input currents are obtained with this control scheme, even under severe voltage dips operating conditions.

II. Voltage Dips

Most of the voltage dips are caused by short-circuit faults; many of them last only a few tens or hundreds of milliseconds and are unbalanced (i.e., involve a negative-sequence component [20]). When a fault occurs at some point in the power system, the voltage drops until a protection trips to clear this fault. During this interval, all loads that are connected at the faulted feeder will be subjected to a voltage dip.

Many surveys on power quality indicate that the most common voltage dips in three-phase power systems are of types A, C, and D [20]. For type A voltage dips, the three-phase voltages are balanced, while the phase voltages are unbalanced for type C or D voltage dips, as shown in Fig. 2.

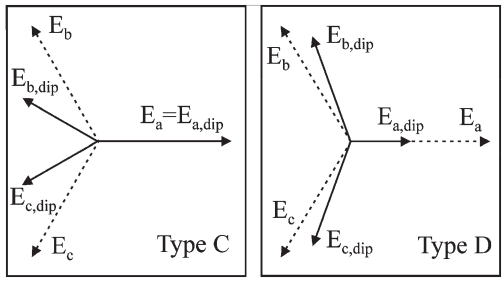

Fig. 2. Phase voltage phasors before (dotted) and during (solid) dip of types C and D.

The type A voltage dip is produced by a three-phase fault, and it is characterized by the same voltage drop in all three phases. The type D voltage dip appears on the secondary side of a distribution transformer with delta/wye connection and having its primary side subjected to a phase-to-phase fault.

A type C voltage dip may occur in any of the following two situations: 1) a phase-to-phase fault at the transformer secondary side or 2) a single-line-to-ground fault in the transformer primary side (seen as phase-to-phase fault at the secondary side).

The three-phase power converters are normally connected without using the neutral wire, and therefore, they are not affected by the zero-sequence voltages due to single-phase and two-phase-to-ground faults. In addition, if a distribution transformer is used, the zero-sequence voltage components will be removed.

As can be noted, the C and D voltage dips involve negative sequence voltage components. As will be demonstrated in Section III, the negative sequence voltage components at a PWM converter input produce a second-order harmonic in the dc-link voltage with undesirable effects. The type A voltage dip does not involve negative sequence components, and thus, the PWM converter operation will not be affected.

In this paper, the effects of type C voltage dips on the operation of a three-phase PWM rectifier are considered, but the conclusions can be extended for type D dips as well.

III. PWM AC/DC Converter Model Under Unbalanced Operating Conditions

The continuous-time dynamic model of the PWM ac/dc converter (Fig. 1) can be represented by the following equations on the ac and dc sides, respectively,

$$\bar{e}_{\alpha\beta} = \bar{v}_{\alpha\beta} + L \cdot \frac{d\bar{i}_{\alpha\beta}}{dt} + R \cdot \bar{i}_{\alpha\beta} \tag{1}$$

$$i_{cap} = C_d \frac{dv_{\rm dc}}{dt} = i_{\rm dc} - i_L \tag{2}$$

where $\bar{e}_{\alpha\beta}$, $\bar{v}_{\alpha\beta}$, and $\bar{i}_{\alpha\beta}$ are the vectors representing the ac input-supply voltages, the converter poles voltages, and the ac input currents in stationary reference frame (α, β), respectively.

It is known that an unbalanced three phase voltage system without zero sequence can be represented as the sum of positive and negative sequence components. The vectors representing

the input-supply voltages, the input currents, and the converter poles voltages can be expressed as

$$\bar{e}_{\alpha\beta} = \bar{e}^{p}_{\alpha\beta} + \bar{e}^{n}_{\alpha\beta} = e^{j\omega t}\cdot \bar{e}^{p}_{dq} + e^{-j\omega t}\cdot \bar{e}^{n}_{dq} \tag{3}$$

$$\bar{i}_{\alpha\beta} = \bar{i}^{p}_{\alpha\beta} + \bar{i}^{n}_{\alpha\beta} = e^{j\omega t}\cdot \bar{i}^{p}_{dq} + e^{-j\omega t}\cdot \bar{i}^{n}_{dq} \tag{4}$$

$$\bar{v}_{\alpha\beta} = \bar{v}^{p}_{\alpha\beta} + \bar{v}^{n}_{\alpha\beta} = e^{j\omega t}\cdot \bar{v}^{p}_{dq} + e^{-j\omega t}\cdot \bar{v}^{n}_{dq} \tag{5}$$

where $\bar{e}^{p}_{dq}$, $\bar{e}^{n}_{dq}$, $\bar{i}^{p}_{dq}$, $\bar{i}^{n}_{dq}$, $\bar{v}^{p}_{dq}$, and $\bar{v}^{n}_{dq}$ are the vectors representing the positive/negative sequence components of the source voltages, input currents, and converter input poles voltages in PNSRF.

The complex power at the converter poles is

$$S_{\text{out}} = (3/2)\cdot\bar{v}_{\alpha\beta}\cdot\bar{i}^{*}_{\alpha\beta} = (3/2)\cdot\left(e^{j\omega t}\cdot\bar{v}^{p}_{dq} + e^{-j\omega t}\cdot\bar{v}^{n}_{dq}\right) \cdot \left(e^{j\omega t}\cdot\bar{i}^{p}_{dq} + e^{-j\omega t}\cdot\bar{i}^{n}_{dq}\right)^{*} \tag{6}$$

where the superscript "*" stands for complex conjugate.

After expanding the terms and rearranging the real part of (6), the instantaneous active power delivered at the converter poles p_{out} has the following three terms: 1) dc component P^{out}_{o}; 2) cosine P^{out}_{c2}; and sine P^{out}_{s2}, the last two at twice the source frequency, i.e.,

$$\text{Re}(S_{\text{out}}) = p_{\text{out}}(t) = P^{\text{out}}_{o} + P^{\text{out}}_{c2}\cdot\cos(2\omega t) + P^{\text{out}}_{s2}\cdot\sin(2\omega t) \tag{7}$$

where

$$P^{\text{out}}_{o} = (3/2)\cdot\left(v^{p}_{d}\cdot i^{p}_{d} + v^{p}_{q}\cdot i^{p}_{q} + v^{n}_{d}\cdot i^{n}_{d} + v^{n}_{q}\cdot i^{n}_{q}\right) \tag{8}$$

$$P^{\text{out}}_{c2} = (3/2)\cdot\left(v^{n}_{d}\cdot i^{p}_{d} + v^{n}_{q}\cdot i^{p}_{q} + v^{p}_{d}\cdot i^{n}_{d} + v^{p}_{q}\cdot i^{n}_{q}\right) \tag{9}$$

$$P^{\text{out}}_{s2} = (3/2)\cdot\left(v^{n}_{q}\cdot i^{p}_{d} - v^{n}_{d}\cdot i^{p}_{q} - v^{p}_{q}\cdot i^{n}_{d} + v^{p}_{d}\cdot i^{n}_{q}\right). \tag{10}$$

The instantaneous reactive power at the converter poles $q_{\text{out}}(t)$ can be calculated on the basis of a set of voltages $\bar{v}^{\perp}_{\alpha\beta}$ that lag the pole voltages $\bar{v}_{\alpha\beta}$ by 90 electrical degrees [17]. Thus, a complex power T_{out} can be defined as

$$T_{\text{out}} = \frac{3}{2}\cdot\bar{v}^{\perp}_{\alpha\beta}\cdot\bar{i}^{*}_{\alpha\beta} = \frac{3}{2}\cdot\left(-je^{j\omega t}\cdot\bar{v}^{p}_{dq} + je^{-j\omega t}\cdot\bar{v}^{n}_{dq}\right) \times \left(e^{j\omega t}\cdot\bar{i}^{p}_{dq} + e^{-j\omega t}\cdot\bar{i}^{n}_{dq}\right)^{*}. \tag{11}$$

After expanding the terms and rearranging the real part of (11), the instantaneous reactive power delivered at the converter poles q_{out} has three terms, namely, the dc component Q^{out}_{o} and harmonic components of twice the source frequency (Q^{out}_{c2} and Q^{out}_{s2}), i.e.,

$$\text{Re}(T_{\text{out}}) = q_{\text{out}}(t) = Q^{\text{out}}_{o} + Q^{\text{out}}_{c2}\cdot\cos(2\omega t) + Q^{\text{out}}_{s2}\cdot\sin(2\omega t) \tag{12}$$

where

$$Q^{\text{out}}_{o} = (3/2)\cdot\left(v^{p}_{q}\cdot i^{p}_{d} - v^{p}_{d}\cdot i^{p}_{q} - v^{n}_{q}\cdot i^{n}_{d} + v^{n}_{d}\cdot i^{n}_{q}\right) \tag{13}$$

$$Q^{\text{out}}_{c2} = (3/2)\cdot\left(-v^{n}_{q}\cdot i^{p}_{d} + v^{n}_{d}\cdot i^{p}_{q} + v^{p}_{q}\cdot i^{n}_{d} - v^{p}_{d}\cdot i^{n}_{q}\right) \tag{14}$$

$$Q^{\text{out}}_{s2} = (3/2)\cdot\left(v^{n}_{d}\cdot i^{p}_{d} + v^{n}_{q}\cdot i^{p}_{q} + v^{p}_{d}\cdot i^{n}_{d} + v^{p}_{q}\cdot i^{n}_{q}\right). \tag{15}$$

In the same manner, the average input active power P^{in}_{o} and the average input reactive power Q^{in}_{o} are obtained as

$$P^{\text{in}}_{o} = (3/2)\cdot\left(e^{p}_{d}\cdot i^{p}_{d} + e^{p}_{q}\cdot i^{p}_{q} + e^{n}_{d}\cdot i^{n}_{d} + e^{n}_{q}\cdot i^{n}_{q}\right) \tag{16}$$

$$Q^{\text{in}}_{o} = (3/2)\cdot\left(e^{p}_{q}\cdot i^{p}_{d} - e^{p}_{d}\cdot i^{p}_{q} - e^{n}_{q}\cdot i^{n}_{d} + e^{n}_{d}\cdot i^{n}_{q}\right). \tag{17}$$

The goal of the control strategy is to avoid ripple in the dc-link voltage and harmonics in the input ac currents, even under severe unbalanced voltage dip operating conditions. At the same time, the output power required by the load and the power factor (close to unity) have to be controlled. To achieve these goals, four constrains must be satisfied [16]. These constraints are represented by a set of four linear equations in PNSRF, i.e.,

$$P^{\text{in}}_{o} = P_{\text{load}} + P_{\text{loss}} = (3/2)\cdot\left(e^{p}_{d}\cdot i^{p}_{d} + e^{p}_{q}\cdot i^{p}_{q} + e^{n}_{d}\cdot i^{n}_{d} + e^{n}_{q}\cdot i^{n}_{q}\right) \tag{18}$$

$$Q^{\text{in}}_{o} = k_{pf}P^{\text{in}}_{o} = (3/2)\cdot\left(e^{p}_{q}\cdot i^{p}_{d} - e^{p}_{d}\cdot i^{p}_{q} - e^{n}_{q}\cdot i^{n}_{d} + e^{n}_{d}\cdot i^{n}_{q}\right) \tag{19}$$

$$P^{\text{out}}_{c2} = 0 = (3/2)\cdot\left(v^{n}_{d}\cdot i^{p}_{d} + v^{n}_{q}\cdot i^{p}_{q} + v^{p}_{d}\cdot i^{n}_{d} + v^{p}_{q}\cdot i^{n}_{q}\right) \tag{20}$$

$$P^{\text{out}}_{s2} = 0 = (3/2)\cdot\left(v^{n}_{q}\cdot i^{p}_{d} - v^{n}_{d}\cdot i^{p}_{q} - v^{p}_{q}\cdot i^{n}_{d} + v^{p}_{d}\cdot i^{n}_{q}\right) \tag{21}$$

where P_{load} is the active power requested by the dc load, P_{loss} is the total power loss (input inductors and converter), and k_{pf} is a coefficient that imposes the average input reactive power Q^{in}_{o} exchanged with the grid (unity power factor is achieved for $k_{pf} = 0$). The first two equations [i.e., (18) and (19)] are related with the average active and reactive power regulation. The remaining constraints [i.e. (20) and (21)] are necessary to nullify the oscillating components of the instantaneous active power at the converter poles to obtain a ripple free dc-link voltage.

IV. Proposed Control Strategy

This paper proposes a new current-reference generator in the stationary reference frame. As it will be demonstrated below, this approach will lead to a much simpler control scheme than the ones implemented in PNSRF [16].

For this reason, (18)–(21) are transformed in stationary reference frame using the following rotational transformations:

$$\begin{bmatrix} x^{p}_{d} \\ x^{p}_{q} \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix}\begin{bmatrix} x^{p}_{\alpha} \\ x^{p}_{\beta} \end{bmatrix} \text{ or } \bar{x}^{p}_{dq} = e^{-j\omega t}\bar{x}^{p}_{\alpha\beta} \tag{22}$$

$$\begin{bmatrix} x^{n}_{d} \\ x^{n}_{q} \end{bmatrix} = \begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix}\begin{bmatrix} x^{n}_{\alpha} \\ x^{n}_{\beta} \end{bmatrix} \text{ or } \bar{x}^{n}_{dq} = e^{j\omega t}\bar{x}^{n}_{\alpha\beta} \tag{23}$$

where the generic variable $\bar{x}$ represents source voltages, input currents, or converter poles voltages.

After the transformations, the new constraints become

$$P_o^{\text{in}} = P_{\text{load}} + P_{\text{loss}} = (3/2)\cdot\left(e_\alpha^p\cdot i_\alpha^p + e_\beta^p\cdot i_\beta^p + e_\alpha^n\cdot i_\alpha^n + e_\beta^n\cdot i_\beta^n\right) \quad (24)$$

$$Q_o^{\text{in}} = k_{pf}P_o^{\text{in}} = (3/2)\cdot\left(e_\beta^p\cdot i_\alpha^p - e_\alpha^p\cdot i_\beta^p - e_\beta^n\cdot i_\alpha^n + e_\alpha^n\cdot i_\beta^n\right) \quad (25)$$

$$P_{c2}^{\text{out}} = \frac{3}{2}\Big[(\cos^2\omega t - \sin^2\omega t)\cdot\left(v_\alpha^n\cdot i_\alpha^p + v_\beta^n\cdot i_\beta^p + v_\alpha^p\cdot i_\alpha^n + v_\beta^p\cdot i_\beta^n\right) - (2\sin\omega t\cos\omega t)\cdot\left(v_\beta^n\cdot i_\alpha^p - v_\alpha^n\cdot i_\beta^p - v_\beta^p\cdot i_\alpha^n + v_\alpha^p\cdot i_\beta^n\right)\Big] = 0 \quad (26)$$

$$P_{s2}^{\text{out}} = \frac{3}{2}\Big[(\cos^2\omega t - \sin^2\omega t)\cdot\left(v_\beta^n\cdot i_\alpha^p - v_\alpha^n\cdot i_\beta^p - v_\beta^p\cdot i_\alpha^n + v_\alpha^p\cdot i_\beta^n\right) + (2\sin\omega t\cos\omega t)\cdot\left(v_\alpha^n\cdot i_\alpha^p + v_\beta^n\cdot i_\beta^p + v_\alpha^p\cdot i_\alpha^n + v_\beta^p\cdot i_\beta^n\right)\Big] = 0. \quad (27)$$

From (26) and (27), it results that P_{c2}^{out} and P_{s2}^{out} become zero if the following two conditions are simultaneously satisfied:

$$v_\alpha^n\cdot i_\alpha^p + v_\beta^n\cdot i_\beta^p + v_\alpha^p\cdot i_\alpha^n + v_\beta^p\cdot i_\beta^n = 0 \quad (28)$$

$$v_\beta^n\cdot i_\alpha^p - v_\alpha^n\cdot i_\beta^p - v_\beta^p\cdot i_\alpha^n + v_\alpha^p\cdot i_\beta^n = 0. \quad (29)$$

Therefore, the new current-reference generator algorithm can be defined using (24) and (25), (28) and (29) in the following matrix form:

$$\frac{2}{3}\begin{bmatrix} P_o^{\text{in}} \\ Q_o^{\text{in}} \\ P_{c2}^{\text{out}} \\ P_{s2}^{\text{out}}\end{bmatrix} = \begin{bmatrix} P_{\text{load}}+P_{\text{loss}} \\ k_{pf}P_o^{\text{in}} \\ 0 \\ 0\end{bmatrix} = \begin{bmatrix} e_\alpha^p & e_\beta^p & e_\alpha^n & e_\beta^n \\ e_\beta^p & -e_\alpha^p & -e_\beta^n & e_\alpha^n \\ v_\alpha^n & v_\beta^n & v_\alpha^p & v_\beta^p \\ v_\beta^n & -v_\alpha^n & -v_\beta^p & v_\alpha^p\end{bmatrix}\cdot\begin{bmatrix} i_\alpha^p \\ i_\beta^p \\ i_\alpha^n \\ i_\beta^n\end{bmatrix}. \quad (30)$$

The current-reference values are obtained from (30) as

$$\begin{bmatrix} i_\alpha^{p*} \\ i_\beta^{p*} \\ i_\alpha^{n*} \\ i_\beta^{n*}\end{bmatrix} = \frac{2}{3}\cdot\begin{bmatrix} e_\alpha^p & e_\beta^p & e_\alpha^n & e_\beta^n \\ e_\beta^p & -e_\alpha^p & -e_\beta^n & e_\alpha^n \\ v_\alpha^n & v_\beta^n & v_\alpha^p & v_\beta^p \\ v_\beta^n & -v_\alpha^n & -v_\beta^p & v_\alpha^p\end{bmatrix}^{-1}\cdot\begin{bmatrix} P_{\text{load}}+P_{\text{loss}} \\ k_{pf}P_o^{\text{in}} \\ 0 \\ 0\end{bmatrix} \quad (31)$$

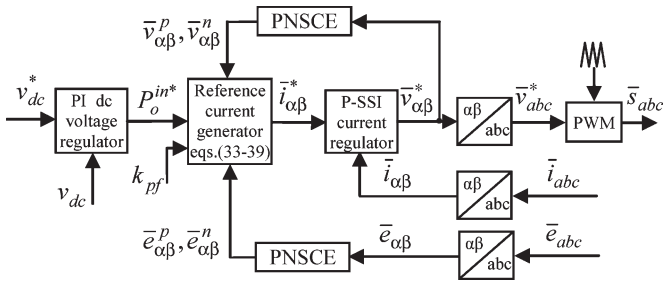

Fig. 3. Block diagram of the proposed control scheme.

$$\bar{i}_{\alpha\beta}^* = \bar{i}_{\alpha\beta}^{p*} + \bar{i}_{\alpha\beta}^{n*} \quad (32)$$

$$i_\alpha^* = i_\alpha^{p*} + i_\alpha^{n*} = \frac{[k_1 + k_3 + (k_2 - k_4)\cdot k_{pf}]\cdot 2P_o^{\text{in}}}{3\cdot den} \quad (33)$$

$$i_\beta^* = i_\beta^{p*} + i_\beta^{n*} = \frac{[k_2 + k_4 + (k_3 - k_1)\cdot k_{pf}]\cdot 2P_o^{\text{in}}}{3\cdot den} \quad (34)$$

where the superscript "*" means reference values and

$$k_1 = e_\alpha^p\left(v_\alpha^{p^2} + v_\beta^{p^2}\right) + e_\alpha^n\left(v_\beta^p v_\beta^n - v_\alpha^p v_\alpha^n\right) - e_\beta^n\left(v_\alpha^p v_\beta^n + v_\beta^p v_\alpha^n\right) \quad (35)$$

$$k_2 = e_\beta^p\left(v_\alpha^{p^2} + v_\beta^{p^2}\right) - e_\alpha^n\left(v_\alpha^p v_\beta^n + v_\beta^p v_\alpha^n\right) + e_\beta^n\left(v_\alpha^p v_\alpha^n - v_\beta^p v_\beta^n\right) \quad (36)$$

$$k_3 = e_\alpha^n\left(v_\alpha^{n^2} + v_\beta^{n^2}\right) - e_\alpha^p\left(v_\alpha^p v_\alpha^n - v_\beta^p v_\beta^n\right) - e_\beta^p\left(v_\alpha^p v_\beta^n + v_\beta^p v_\alpha^n\right) \quad (37)$$

$$k_4 = e_\beta^n\left(v_\alpha^{n^2} + v_\beta^{n^2}\right) - e_\alpha^p\left(v_\alpha^p v_\beta^n + v_\beta^p v_\alpha^n\right) - e_\beta^p\left(v_\beta^p v_\beta^n - v_\alpha^p v_\alpha^n\right) \quad (38)$$

$$den = k_1\cdot e_\alpha^p + k_2\cdot e_\beta^p + k_3\cdot e_\alpha^n + k_4\cdot e_\beta^n. \quad (39)$$

The block diagram of the proposed control scheme is shown in Fig. 3. The key component in the proposed scheme is the reference current generator block that uses the (33)–(39). These equations require multiply and accumulate operations that are easily computed with up-to-date 100 ÷ 150 millions of instructions per second fixed-point digital signal processors.

The sequence components of the source voltage $\bar{e}_{\alpha\beta}^p$, $\bar{e}_{\alpha\beta}^n$ and converter poles voltage $\bar{v}_{\alpha\beta}^p$, $\bar{v}_{\alpha\beta}^n$ are obtained using the positive/negative sequence component extraction (PNSCE) control block. The signals utilized by PNSCE are the measured source voltages $\bar{e}_{\alpha\beta}$ and the converter voltage reference $\bar{v}_{\alpha\beta}$. There are two possibilities of implementing the PNSCE block in a stationary reference frame. The first solution uses the delay signal cancellation method [21]; the intrinsic time delay of 5 ms and the zero steady-state error properties make this

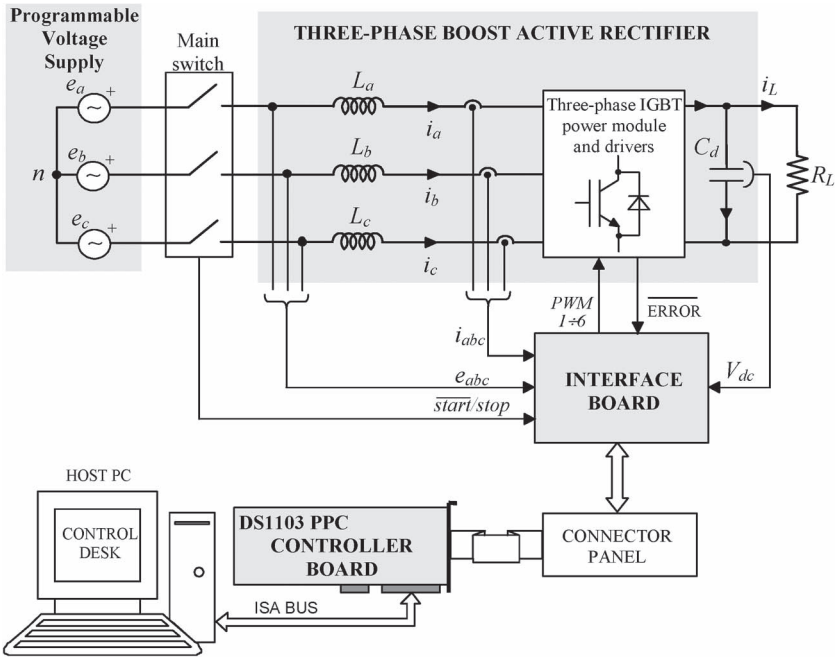

Fig. 4. Experimental setup of the three-phase boost active rectifier.

calculation algorithm a good option for extracting the sequence components. The second solution employs the dual second-order generalized integrator (DSOGI) [22]; this solution is recommended for a clean current-reference generation under grid voltage harmonic distortion. The DSOGI has been chosen for the proposed control scheme to implement the PNSCE block.

The proposed control scheme (Fig. 3) consists of the following two cascaded control loops: 1) an outer dc-link voltage control loop and 2) an inner ac input current control loop. The bandwidth of the current loop is high for fast tracking of the reference currents. The inner ac input current loop employs two P-SSI regulators implemented in stationary reference frame and having the transfer function

$$H_{\text{P-SSI}}(s) = k_{pi} + \frac{2 \cdot k_{ii} \cdot s}{s^2 + \omega_1^2}. \tag{40}$$

A PI controller is employed for the dc-link voltage regulation. Its bandwidth is about 20 times slower than the current controller bandwidth. The dynamic performance of the dc-link voltage regulation is imposed by the dc-link voltage regulator only if the PNSCE transient response is faster than the dc-link voltage loop. The output of the dc-link controller sets the reference for the average input active power.

A small variation (± 1 Hz) of the grid voltage frequency has a minor impact on the P-SSI current regulation. If large frequency variations may occur, a frequency-adaptive P-SSI controller may be used [23] with no particular problems.

If necessary, the robustness of the current controller against grid voltage harmonic distortion (mainly fifth and seventh in three-phase systems) is achieved with a harmonic compensator. It is easy to extend the capabilities of the scheme by adding harmonic compensation features simply with more resonant controllers in parallel with the main controller.

TABLE I
EXPERIMENTAL SETUP PARAMETERS

Parameter	Symbol	Value
Input boost inductor	L	3 mH
DC-link capacitance	C_d	150 µF
Rated DC-link voltage	V_{dc}	700 V
Switching frequency	f_{sw}	10 kHz
Sampling frequency	f_s	10 kHz
Fundamental frequency	f_1	50 Hz
Load resistance	R_L	45 Ω

V. EXPERIMENTAL RESULTS

This section is organized as follows. First, the experimental setup is described. Then, a comparison between the proposed scheme and another two schemes known from the literature is performed. At the end, a complete experimental validation of the proposed scheme is presented, showing the instantaneous active and reactive power components at converter input, the converter poles, and also across the input reactors.

A. Experimental Setup

The general diagram of the experimental setup is shown in Fig. 4. The system parameters are given in Table I. A 20-kVA PWM rectifier prototype using a switching frequency of 10 kHz has been used for the experimental tests. The rectifier interface inductance L is 3 mH. The dc-link reference voltage of the IGBT converter has been set at 700 V, and the dc-link capacitance is only 150 μF, obtained with two film capacitors connected in series. The PWM rectifier control was implemented on the dSPACE DS1103 development board. The quantities measured from the system are the PWM rectifier currents, the source line-to-line voltages, and the dc-link voltage, as shown in Fig. 4. All analog-to-digital conversions are synchronized with the converter PWM operation.

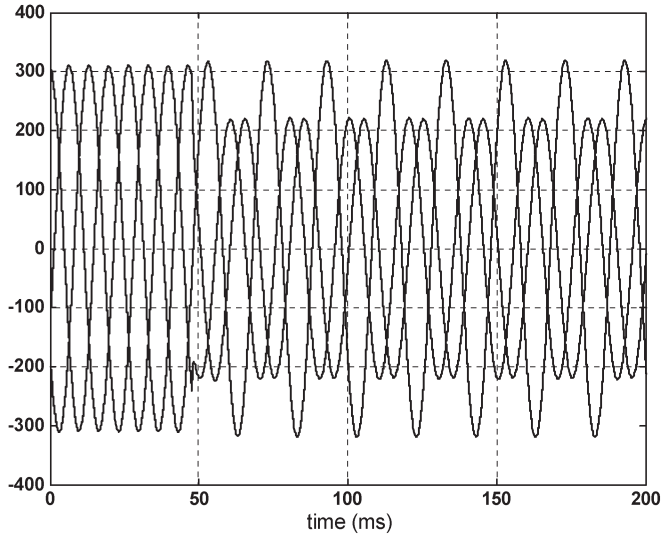

Fig. 5. Sampled source phase voltages e_{abc} (in volts) under a 30% type C voltage dip transient.

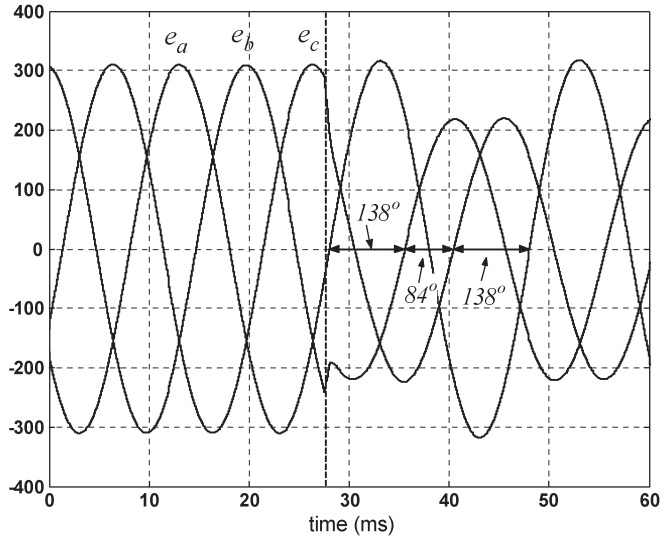

Fig. 6. Zoomed-in view around the voltage dip start time. Sampled source phase voltages e_{abc} (in volts) under a 30% type C voltage dip transient.

A 12-kVA programmable voltage supply (PVS) (Fig. 4) has been used to emulate the grid. A 30% type C voltage dip transient [20] (shown in Fig. 5) has been generated by means of the PVS. The amplitudes of the voltages e_b and e_c drop from 320 to 210 V during the dip. In addition, the phase angles of the generated voltages e_a, e_b, and e_c change from 0°, 120°, and 240° to 0°, 138°, and 222°, respectively, as shown in Fig. 6.

B. Comparison of the Proposed Scheme With Other Solutions Known From the Literature

The two control schemes used for comparison with the proposed solution are given as follows.

1) The first control scheme (Fig. 7) computes the reference currents using the source voltage vector $\bar{e}_{\alpha\beta}$ (41)–(44). In contrast with the proposed control strategy, this control scheme eliminates the second-order harmonics of the

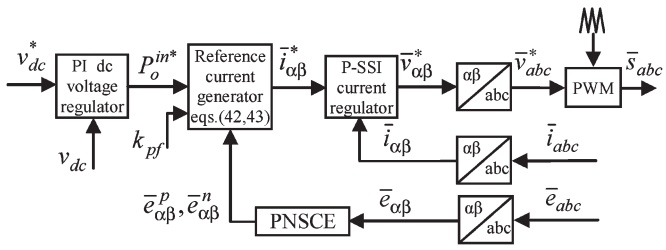

Fig. 7. Block diagram of the IAPI control scheme.

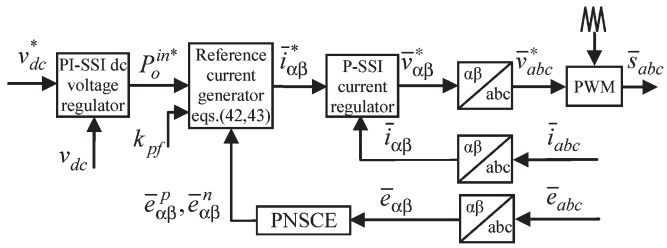

Fig. 8. Block diagram of the dc-PI-SSI control scheme.

Instantaneous Active Power p_{in} at the Input stage (IAPI) of the PWM rectifier [10]–[13], resulting in a different set of equations used for reference currents computation, i.e.,

$$\begin{bmatrix} i_\alpha^{p*} \\ i_\beta^{p*} \\ i_\alpha^{n*} \\ i_\beta^{n*} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} e_\alpha^p & e_\beta^p & e_\alpha^n & e_\beta^n \\ e_\beta^p & -e_\alpha^p & -e_\beta^n & e_\alpha^n \\ e_\beta^n & -e_\alpha^n & -e_\beta^p & e_\alpha^p \\ e_\alpha^n & e_\beta^n & e_\alpha^p & e_\beta^p \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{\text{load}} + P_{\text{loss}} \\ k_{pf} P_o^{\text{in}} \\ 0 \\ 0 \end{bmatrix} \tag{41}$$

$$i_\alpha^* = i_\alpha^{p*} + i_\alpha^{n*} = \frac{\left[e_\alpha^p - e_\alpha^n + \left(e_\beta^p + e_\beta^n\right) \cdot k_{pf}\right] \cdot 2 \cdot P_o^{\text{in}}}{3 \cdot den} \tag{42}$$

$$i_\beta^* = i_\beta^{p*} + i_\beta^{n*} = \frac{\left[e_\beta^p - e_\beta^n - (e_\alpha^p + e_\alpha^n) \cdot k_{pf}\right] \cdot 2 \cdot P_o^{\text{in}}}{3 \cdot den} \tag{43}$$

where the superscript "*" stands for reference values and

$$den = (e_\alpha^p)^2 + \left(e_\beta^p\right)^2 - (e_\alpha^n)^2 - \left(e_\beta^n\right)^2. \tag{44}$$

It can be noted from (41) that only the source voltage sequence components $\bar{e}_{\alpha\beta}^p$, $\bar{e}_{\alpha\beta}^n$ are needed by the reference current generator, and for this reason, only one PNSCE block is used in this control scheme, as shown in Fig. 7.

2) The second control scheme (Fig. 8) uses the same reference current generator like the IAPI control scheme, but a PI-SSI controller is used in the dc-link voltage loop to cancel the second-order harmonic ripple [19] (dc-PI-SSI).

The experimental results of the PWM rectifier transient and steady-state responses are shown in Figs. 9–11 and Figs. 12–14,

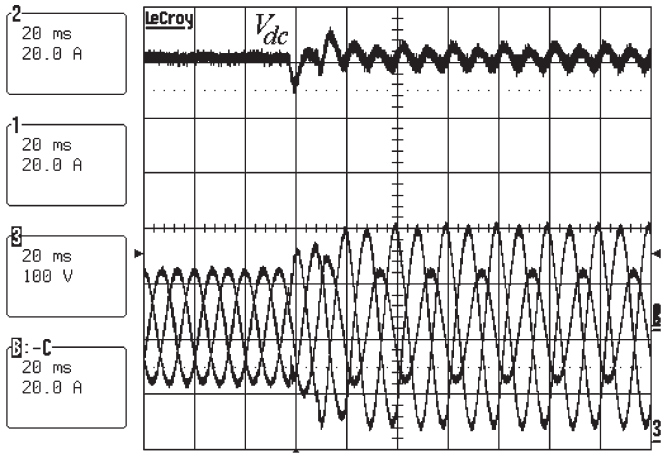

Fig. 9. IAPI control scheme. Transient response under a 30% type C voltage dip. Traces 1, 2, B: converter input currents i_{abc} (in amperes); trace 3: dc-link voltage $V_{\rm dc}$ (in volts).

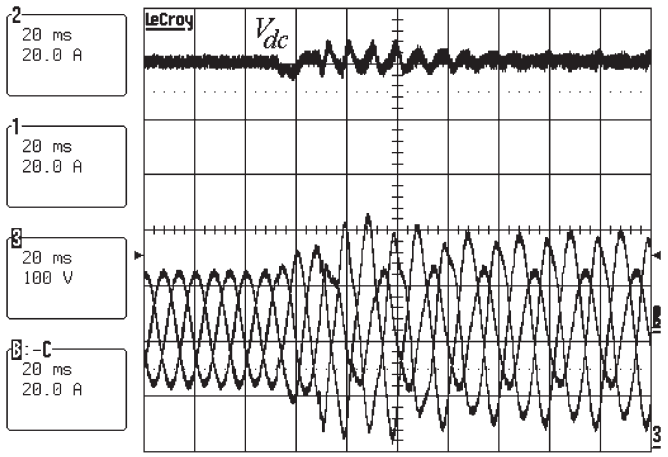

Fig. 10. DC-PI-SSI control scheme. Transient response under a 30% type C voltage dip. Traces 1, 2, B: converter input currents i_{abc} (in amperes); trace 3: dc-link voltage $V_{\rm dc}$ (in volts).

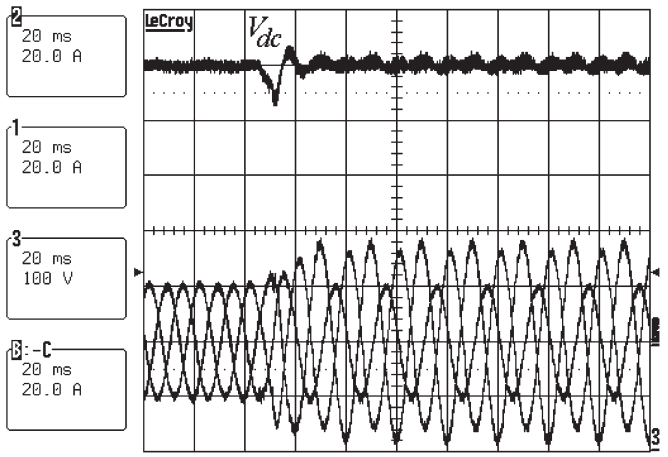

Fig. 11. Proposed control scheme. Transient response under a 30% type C voltage dip. Traces 1, 2, B: converter input currents i_{abc} (in amperes); trace 3: dc-link voltage $V_{\rm dc}$ (in volts).

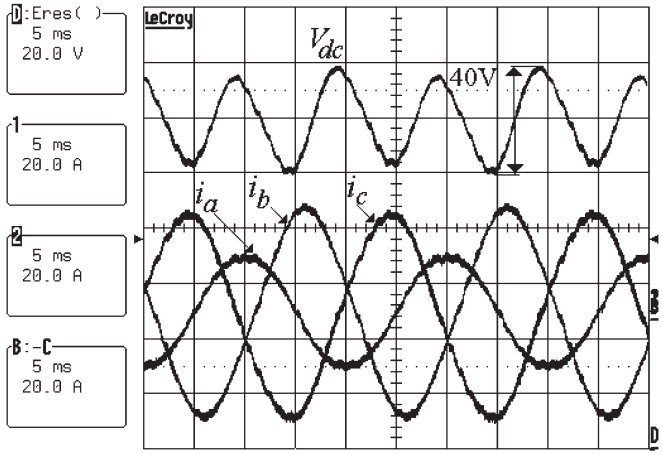

Fig. 12. IAPI control scheme. Steady-state response under a 30% type C voltage dip. Traces 1, 2, B: converter input currents i_{abc} (in amperes); trace D: dc-link voltage V_{dc} (in volts).

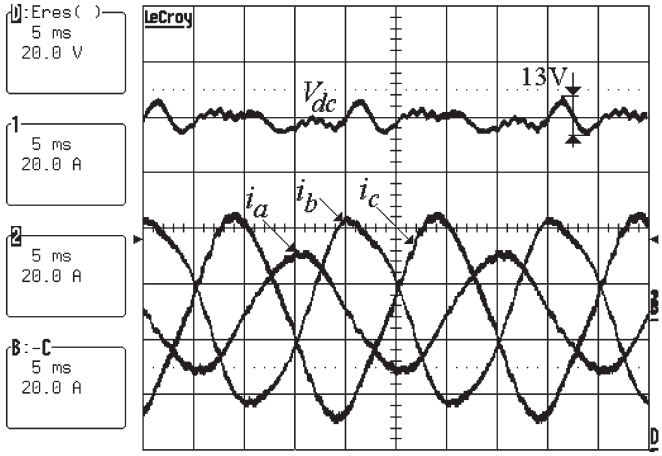

Fig. 13. DC-PI-SSI control scheme. Steady-state response under a 30% type C voltage dip. Traces 1, 2, B: converter input currents i_{abc} (in amperes); Trace D: dc-link voltage $V_{\rm dc}$ (in volts).

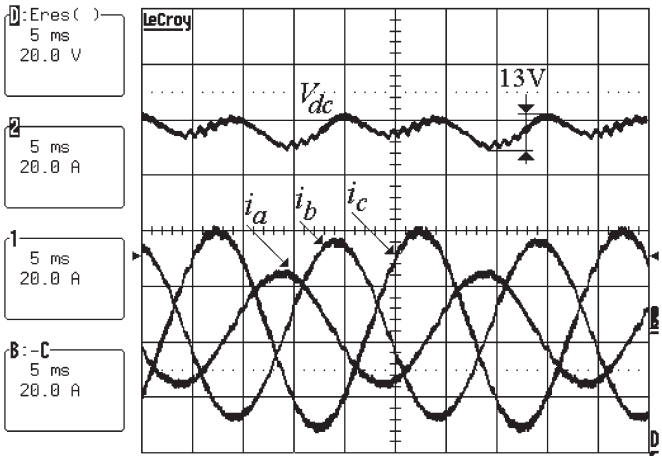

Fig. 14. Proposed control scheme. Steady-state response under a 30% type C voltage dip. Traces 1, 2, B: converter input currents i_{abc} (in amperes); trace D: dc-link voltage $V_{\rm dc}$ (in volts).

respectively. The dc-link voltage in Figs. 12–14 has been filtered to emphasize the low-order harmonics. The transient responses (Figs. 9–11) show a fast dynamic response (15 ms of settling time) of the IAPI control scheme and the proposed control scheme; meanwhile, the dc-PI-SSI control scheme has a major settling time.

TABLE II
STEADY-STATE OPERATION PERFORMANCE

Control scheme	DC-link voltage ripple (peak to peak)	THD of input AC current
IAPI	40 V	2 %
DC-PI-SSI	13 V	6 %
Proposed scheme	13 V	1.2 %

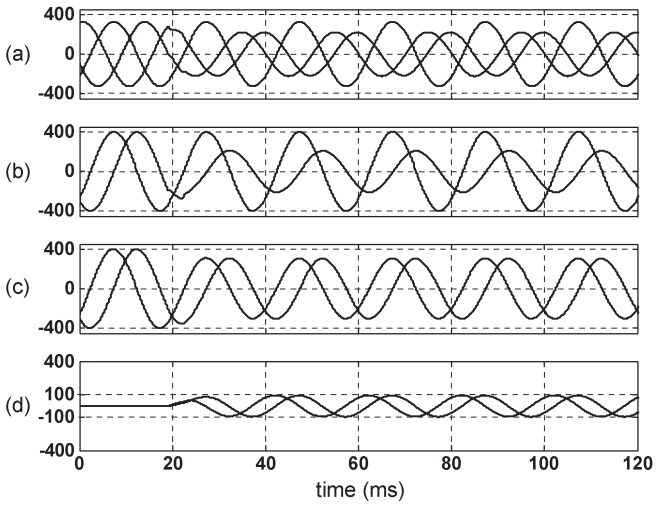

Fig. 15. Extraction of the source voltage sequence components under a 30% type C voltage dip transient using DSOGI. From top to bottom: (a) e_{abc} (in volts); (b) $e_{\alpha\beta}$ (in volts); (c) $e^{p}_{\alpha\beta}$ (in volts); (d) $e^{n}_{\alpha\beta}$ (in volts).

From Figs. 12–14 and Table II, it results that the proposed control scheme and the dc-PI-SSI strategy exhibit better performance at steady-state in dc-link voltage regulation than the IAPI control scheme. However, the converter with dc-PI-SSI control scheme draws a distorted ac input current having a 6% of total harmonic distortion (THD). This value is five times higher than the input current THD obtained with the proposed control scheme. This happens because in the dc-PI-SSI control scheme there is an SSI tuned on 100 Hz in the voltage loop (i.e., on the second-order harmonic). This SSI produces a second-order harmonic component that is proportional with the voltage dip severity. The reference current generator modulates the output of the dc-link voltage controller with the fundamental frequency, generating a third-order harmonic component in the reference current.

The proposed scheme uses for reference currents computation the reference pole voltages instead of the real pole voltages. In practice, there is a slight difference (introduced by the converter) between the real pole voltages and their reference values. This difference will cause a small residual dc-link voltage ripple (about 2% of rated dc-link voltage), as shown in Fig. 14.

The extraction of the source voltage sequence components under 30% type C voltage dip using DSOGI is shown in Fig. 15. The fast transient response (about 5 ms) can be noted in case of a voltage dip, therefore, the dynamic performance of the dc-link voltage regulation is imposed by the dc-link voltage loop.

The proposed control scheme exhibits the best performance in terms of dc-link voltage ripple elimination and THD of the converter inputs currents when compared with the other two solutions. The improvement becomes more evident as the rectifier rated power increases. That happens due to the impact of the neglected instantaneous power related to the input inductors.

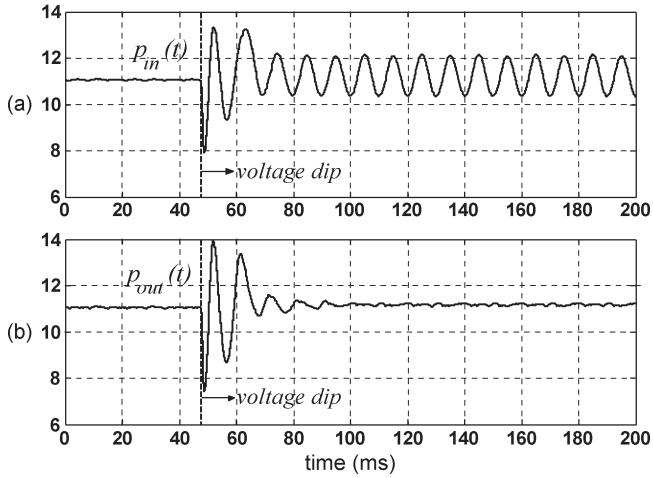

Fig. 16. Instantaneous active power at the front input and at the converter poles for the proposed scheme. From top to bottom: (a) $p_{\rm in}(t)$ (in kilowatts) and (b) $p_{\rm out}(t)$ (in kilowatts).

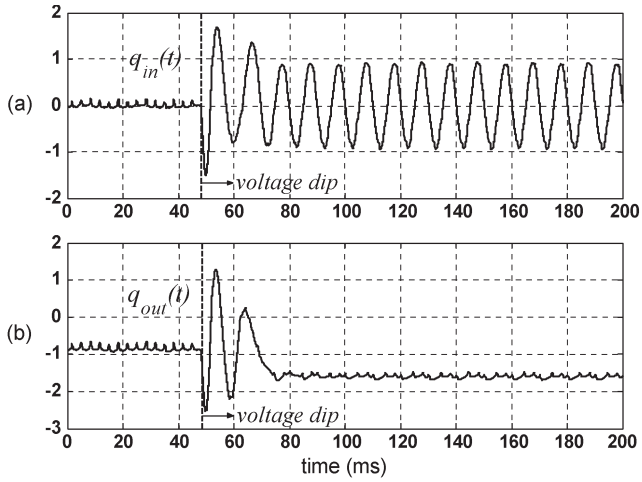

Fig. 17. Instantaneous reactive power at the front input and at the converter poles for the proposed scheme. From top to bottom: (a) $q_{\rm in}(t)$ (in kilovolt-amperes reactive) and (b) $q_{\rm out}(t)$ (in kilovolt-amperes reactive).

C. Performance Validation Using Instantaneous Active and Reactive Power Components

The next experimental results (Figs. 16–19) are related to the instantaneous active and reactive power components at the converter front input, across the inductors, and at the converter poles to confirm the validity of the constraints (24)–(27) used for the reference currents computation. The instantaneous power components have been computed using the sampled source voltages, the converter input currents, and the reference pole voltages.

The first two constraints [i.e., (24) and (25)] are related to the average active and reactive power regulation; the remaining constraints [i.e., (26) and (27)] are necessary to cancel the second-order harmonic components of the instantaneous active power at the converter poles $P^{\rm out}_{c2}\cos(2\omega t)$, $P^{\rm out}_{s2}\sin(2\omega t)$ to obtain ripple free dc-link voltage.

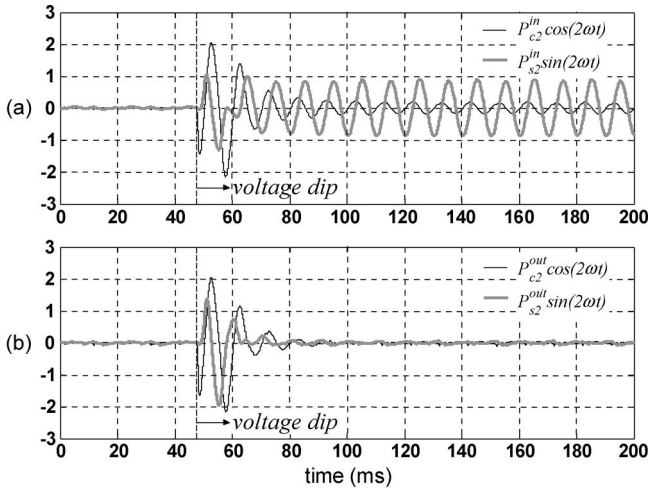

Fig. 18. Second-order harmonic components of the instantaneous active power at the front input and at the poles of the converter for the proposed scheme. From top to bottom: (a) $P_{c2}^{\rm in}\cos(2\omega t)$, $P_{s2}^{\rm in}\sin(2\omega t)$ (kW) and (b) $P_{c2}^{\rm out}\cos(2\omega t)$, $P_{s2}^{\rm out}\sin(2\omega t)$ (kW).

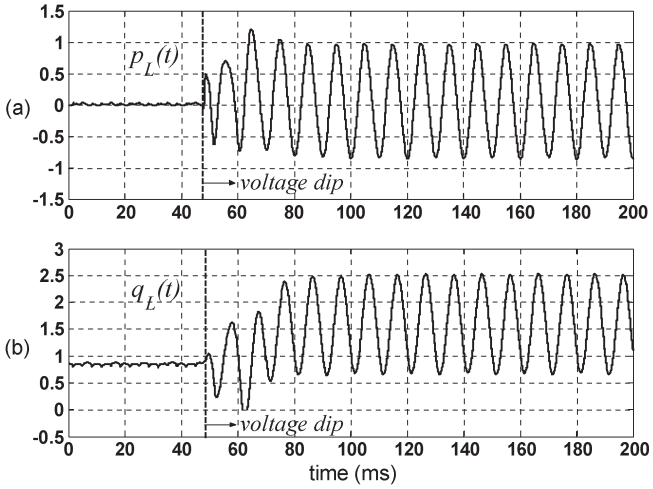

Fig. 19. Instantaneous active and reactive power across the inductor for the proposed scheme. From top to bottom: (a) $p_L(t)$ (in kilowatts) and (b) $q_L(t)$ (in kilovolt-amperes reactive).

The instantaneous active power at the converter front input $p_{\rm in}(t)$ and at the converter terminals $p_{\rm out}(t)$ during the voltage dip transient are given in Fig. 16. From the first constraint given in (24), the average active power at the converter front input is regulated to cover the power required by the dc load and the losses. It can be seen in Fig. 16 that the average part of $p_{\rm in}(t)$ during the voltage dip is higher than the case of normal voltage conditions due to the increased input currents (Fig. 11) that produce increased losses.

The instantaneous reactive power at the converter front input $q_{\rm in}(t)$ and at the converter poles $q_{\rm out}(t)$ during the voltage dip transient are presented in Fig. 17. The second constraint [i.e., (25)] is fulfilled since the average input reactive power is zero in Fig. 17. Consequently, unity average power factor is achieved.

The second-order harmonic components $P_{c2}^{\rm in}\cos(2\omega t)$, $P_{s2}^{\rm in}\sin(2\omega t)$ of the instantaneous active power at the front input, along with the second-order harmonic components $P_{c2}^{\rm out}\cos(2\omega t)$, $P_{s2}^{\rm out}\sin(2\omega t)$ at the converter poles are illustrated in Fig. 18. It can be seen that the oscillating components of the instantaneous active power at the converter poles are cancelled according to the constraints in (26) and (27), as shown in Fig. 18. This can also be noted in Fig. 16, where the instantaneous active power at the converter poles $p_{\rm out}(t)$ contains only a dc component at steady state. Therefore, it can be concluded that all the given constraints [i.e., (24)–(27)] have been experimentally confirmed.

In addition, the instantaneous active and reactive powers $p_L(t)$ and $q_L(t)$ across the inductor are shown in Fig. 19. It can be noted that the average component of the instantaneous active power across inductors (during the voltage dip) is not zero, showing the inductors power losses. Moreover, the average reactive power across the inductor is also increased due to the increase of the converter input currents.

Independently of the unbalanced voltage dip type, there is always a second-order harmonic power ripple at the converter poles. As it has been demonstrated, the proposed control scheme eliminates the second-order harmonic power ripple at the converter poles. For this reason, the proposed scheme is an effective control method that successfully mitigates with any type of voltage dip.

The design of the power converter must take into account the increase of the currents during the voltage dips compensation. As an example, during a 30% type C voltage dip (phases b and c), the i_c current increases by 60% (Fig. 11). Most of voltage dips magnitudes are within 40% [20]. The designer should consider the worse case for the specific application to oversize the power part accordingly.

VI. Conclusion

A new stationary frame control scheme for three-phase PWM rectifiers operating under unbalanced voltage dips conditions has been proposed in this paper. The proposed control scheme regulates the instantaneous active power at the converter poles to minimize the harmonics of the input currents and the output voltage ripple. The novelty consists of the development of a new current-reference generator that is implemented directly in stationary reference frame. This allows using P-SSI controllers for simultaneous compensation of both positive and negative current sequence components. Consequently, no PLL strategies and coordinate transformations are needed for the proposed reference current generator. Experimental results are presented for a 20-kVA PWM rectifier prototype. A comparison with two different existing control techniques is also performed. The experimental results demonstrate that the proposed control scheme has fast dynamic performance and yields small dc-link voltage ripple (with only 150 μF of dc-link film capacitor) and sinusoidal input currents, even under severe voltage dips operating conditions.

References

[1] C. J. Melhorn, T. D. Davis, and G. E. Beam, "Voltage sags: Their impact on the utility and industrial customers," *IEEE Trans. Ind. Appl.*, vol. 34, no. 3, pp. 549–558, May/Jun. 1998.

[2] L. Moran, P. D. Ziogas, and G. Joos, "Design aspects of synchronous PWM rectifier-inverter systems under unbalanced input voltage conditions," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1286–1293, Nov./Dec. 1992.

[3] P. N. Enjeti and S. A. Choudhury, "A new control strategy to improve the performance of a PWM AC to DC converter under unbalanced operating conditions," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 493–500, Oct. 1993.
[4] C. Du, M. H. J. Bollen, E. Agneholm, and A. Sannino, "A new control strategy of a VSC–HVDC system for high-quality supply of industrial plants," *IEEE Trans. Power Del.*, vol. 22, no. 4, pp. 2386–2394, Oct. 2007.
[5] L. Xu, B. R. Andersen, and P. Cartwright, "VSC transmission operating under unbalanced AC conditions—Analysis and control design," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 427–434, Jan. 2005.
[6] J. Zhang, H. Chen, W. Pan, and C. Wang, "VSC-HVDC control under unbalanced supply conditions," in *Conf. Rec. IEEE Power Eng. Soc. Gen. Meeting*, 2007, pp. 1–6.
[7] L. Xu and Y. Wang, "Dynamic modeling and control of DFIG-based wind turbines under unbalanced network conditions," *IEEE Trans. Power Syst.*, vol. 22, no. 1, pp. 314–323, Feb. 2007.
[8] L. Xu, "Coordinated control of DFIG's rotor and grid side converters during network unbalance," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1041–1049, May 2008.
[9] R. Pena, R. Cardenas, E. Escobar, J. Clare, and P. Wheeler, "Control system for unbalanced operation of stand-alone doubly fed induction generators," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 544–545, Jun. 2007.
[10] P. Rioual, H. Pouliquen, and J. P. Louis, "Regulation of a PWM rectifier in the unbalanced network state using a generalized model," *IEEE Trans. Power Electron.*, vol. 11, no. 3, pp. 495–502, May 1996.
[11] H. Song and K. Nam, "Dual current control scheme for PWM converter under unbalanced input voltage conditions," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 953–959, Oct. 1999.
[12] B. Yin, R. Oruganti, S. K. Panda, and A. K. S. Bhat, "High-performance control of a boost type PWM rectifier under unbalanced operating conditions with integral variable structure control," in *Conf. Rec. IEEE PESC*, 2005, pp. 1992–1997.
[13] P. Rodríguez, A. V. Timbus, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Flexible active power control of distributed power generation systems during grid faults," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2583–2592, Oct. 2007.
[14] Y. Suh, V. Tijeras, and T. A. Lipo, "A control method in dq synchronous frame for PWM boost rectifier under generalized unbalanced operating conditions," in *Conf. Rec. IEEE PESC*, 2002, vol. 3, pp. 1425–1430.
[15] Y. Suh, V. Tijeras, and T. A. Lipo, "A nonlinear control of the instantaneous power in dq synchronous frame for PWM AC/DC converter under generalized unbalanced operating conditions," in *Conf. Rec. IEEE IAS Annu. Meeting*, 2002, vol. 2, pp. 1189–1196.
[16] Y. Suh and T. A. Lipo, "Control scheme in hybrid synchronous stationary frame for PWM AC/DC converter under generalized unbalanced operating conditions," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 825–835, May/Jun. 2006.
[17] Y. Suh and T. A. Lipo, "Modeling and analysis of instantaneous active and reactive power for PWM AC/DC converter under generalized unbalanced network," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1530–1540, Jul. 2006.
[18] A. Yazdani and R. Iravani, "A unified dynamic model and control for the voltage-sourced converter under unbalanced grid conditions," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1620–1629, Jul. 2006.
[19] J. G. Hwang, P. W. Lehn, and M. Winkelnkemper, "Control of grid connected AC-DC converters with minimized DC link capacitance under unbalanced grid voltage condition," in *Conf. Rec. EPE*, 2007, pp. 1–10.
[20] M. H. J. Bollen, *Understanding Power Quality Problems: Voltage Sags and Interruptions*. Piscataway, NJ: IEEE Press, 2002.
[21] J. Svensson, M. Bongiorno, and A. Sannino, "Practical implementation of delayed signal cancellation method for phase-sequence separation," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 18–26, Jan. 2007.
[22] P. Rodríguez, R. Teodorescu, I. Candela, A. V. Timbus, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *Conf. Rec. IEEE PESC*, 2006, pp. 1–7.
[23] A. V. Timbus, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Adaptive resonant controller for grid-connected converters in distributed power generation systems," in *Conf. Rec. IEEE APEC*, 2006, pp. 1601–1606.

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