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Test infrastructures evaluation at transaction level / DI CARLO, Stefano; Hatami, N.; Prinetto, Paolo Ernesto. - ELETTRONICO. - (2009), pp. 1-1. (IEEE International Test Conference (ITC) Austin (TX), USA 1-6 Nov. 2009 [10.1109/TEST.2009.5355830].

Availability:

This version is available at: 11583/2296432 since: 2016-09-16T17:28:13Z

Publisher:

IEEE

Published

DOI:10.1109/TEST.2009.5355830

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Published in the Proceedings of the IEEE International Test Conference (ITC), 1-6 Nov. 2009, Austin (TX), USA.

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PUBLISHED manuscript is available on IEEE Xplore®:**

URL: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5355830>

DOI: [10.1109/TEST.2009.5355830](https://doi.org/10.1109/TEST.2009.5355830)

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Test Infrastructures Evaluation at Transaction Level

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Abstract

The goal of this work is to propose a method to fully exploit TLM2.0 potentialities to evaluate test infrastructures. By providing the high level model with necessary information from RTL, the behavior of test infrastructures can be simulated taking advantage of high simulation speed of TLM. This way, the high level model is able to both estimate the cost of test infrastructure much faster and facilitate decision making for proper test infrastructure at RTL.

1. Introduction

Transaction Level Modeling (TLM) is vastly used by Electronic System Level (ESL) design industry to describe systems at the early stages of the design. As TLM is proving to be a valuable medium to increase the design flow efficiency by moving the overall design problem to higher abstraction levels, testing solutions are still defined at lower abstraction levels. The communication-centric view of TLM is well suited to model test infrastructures involving the exchange of significant amounts of data. Also, performance modeling in TLM tries to accurately capture concurrency in a system, which is easily adapted to model the concurrency in testing [1].

A few publications tackled test problems at TLM level. [2] proposes a plug and test design methodology based on insertion of testing capabilities at the transaction level using testable TLM primitives. It only deals with basic FIFO communication channels defined in TLM1.0 standard. [1] shows how TLM can be used to efficiently evaluate Design for Testability decisions in the early design steps, and how to evaluate test scheduling and resource partitioning during test planning. Although these publications are starting to address the problem of testing at TLM, the results are still limited and a strong investment to address this problem in a more general way is required.

Here, the idea is to propose a method to use TLM high simulation speed to validate low level test infrastructures. This way, we can evaluate different test infrastructures using simulation; such an evaluation is usually not feasible at RTL, due to the simulation time restrictions.

2. Discussion

Evaluating test and testability at RTL is too expensive, as the simulation time increases rapidly with the increase in test patterns. High simulation speed of TLM can provide us with the ability to evaluate the impact of the test infrastructures that will be later added at lower level.

Information items related to the test infrastructure are either provided by the designer (e.g., the BIST architecture, the type of compressor/decompressor used, the number of scan chains, ...), or estimated via the synthesis tools, or directly imported from RTL when the RTL description is already available, as in the case of legacy or bought cores. This information is then used at high level to provide design metrics to evaluate test infrastructures at TLM level.

Fast simulation speed of TLM makes it possible to simulate several copies of the design using different test infrastructures and to compare those targeting defined metrics at this level. So to evaluate test infrastructure at high level, we can replicate the design at system level and simulate each replica with a proposed testing mechanism. The comparison can be done focusing, for instance, on system throughput, test delay and frequency penalties, power consumption and area overhead.

To provide an example, we can think of test optimization with respect to the test time. Two test mechanisms are considered: BIST structure with the delay time of "X" calculated at RTL, and scan chains with "K" flip-flops each with the delay of "k" at test mode. In both cases, TPG block should be used to provide the test data to both replicas of the design. To compare, for BIST we can model the test infrastructure as below:

```
if (test is enabled) ...;      Wait for "X" ns;  
else                            Normal Operation of the design;
```

In case of scan chains, it can be modeled as:

```
if (test mode)                ...;      Wait for K*k;  
else                            Normal operation of the design;
```

The execution time comparison of the two cases can give us a relative idea of test execution time at RTL. Other metrics can be defined using similar method.

Although this idea is still under development and needs more work to complete, it can be a big step forward to define test infrastructures at TLM which leads to higher performance of the overall design.

3. References

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