Electrical Model of a Microcontroller for EMC Analysis

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***Abstract* — In this paper a new methodology to model the power supply network of complex integrated circuits by means of circuit and electromagnetic simulations of internal building blocks is proposed. The models obtained by adopting this methodology can be employed by silicon manufacturers to perform SPICE-like simulations in the early phases of a chip development with the aim to analyze and optimize their designs in terms of EMC performances. The comparison between measurement results on an 8-bit microcontroller with model simulations validates the proposed approach.**

1. INTRODUCTION

Due to the semiconductor technology scaling trend, integrated circuits (ICs) are among the major sources of electromagnetic emissions (EMEs) at the system-level. The ever-increasing operating frequency and integration density of ICs are causing steep currents to flow through the on-chip power supply network (PSN) and the package frame, driving the generation of radiated and conducted emissions at printed-circuit-board (PCB) level. Research activities focused on reducing EMEs of ICs have received increasing attention in recent years due to the advantages that on-chip mitigation techniques of EMEs can offer compared with PCB-level solutions [1,2]. Transistor-level simulations could provide designers with insight as to how their design solutions contribute to the generated emissions and how to implement modifications that will result in lower EMEs. However, simulations of complex ICs are not feasible and simulations at a higher abstraction level cannot provide the required information.

In this work is presented a methodology to model the PSN of mixed-signal ICs, like microcontrollers (μCs), by constant, lumped and linear parameters obtained by simulations performed in the early design phases. The proposed model allows one to investigate EMEs of μCs by carrying out low time-consuming simulations in a SPICE-like environment. The methodology is based on the assumption that complex ICs are composed of functional blocks, each devoted to a specific function, but also PSN at the chip- and the package-level and parasitic propagation paths for disturbances like the substrate. Realistic circuit models of functional blocks can be extracted from transistor-level small-signal simulations and from an estimation of area occupancy.

The model of interconnects is derived in terms of RLC parameters obtained from electromagnetic simulations and by considering the parasitic coupling through the semiconductor substrate. The approach proposed in what follows differs from those available in the literature like the ICEM and the LEECS models, in some ways. ICEM

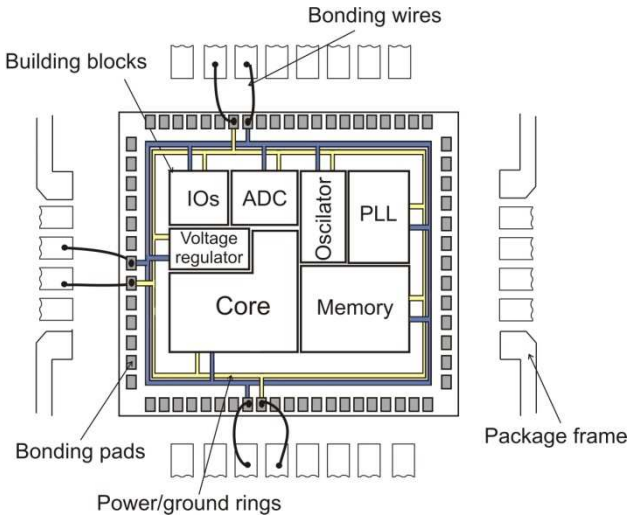

Fig. 1. Block diagram of a generic μC.

and LEECS models are powerful black-box (i.e. behavioral) macro-models of ICs that semiconductor manufacturers provide to system designers to be employed as equivalent emission sources in computer simulations of EMEs at the PCB-level [3,4]. The parameters that describe such models are derived, for this purpose, from measurements or simulations at the external ports of an IC. As a consequence, although they can also be employed by IC designers in the preliminary design phases, detailed information on the impact of design parameters and the effects of design modifications on delivered EMEs cannot be obtained. The proposed methodology also differs from other modeling techniques, such as that described in [5], where the derivation of functional model blocks requires the use of specific software tools.

In this paper, the proposed model methodology is described for a generic μC with the aim to predict conducted emissions induced by core switching activity and delivered through input/output (IO) ports. The comparison between measured and simulated scattering (S) parameters at external ports of an 8-bit μC and the comparison between simulated and measured conducted EMEs of the device under test are presented and commented on.

2. MODELING METHODOLOGY

Conducted EME of ICs originates from currents flowing through the PSN during transistor switching. In this context, the impedance that loads the on-chip power network is the reason for the coupling of disturbances among the different sections of an IC and it determines

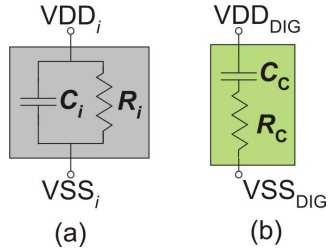

Fig. 2. Model of the: (a) analog blocks; (b) digital blocks.

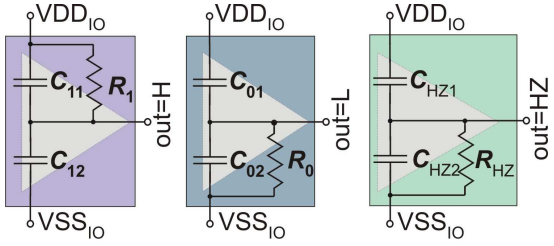

Fig. 3. IO port models: (a) high output; (b) low output; (c) high impedance

the amount of emissions that will be delivered from external ports. Such PSN impedance consists of the impedances between power supply terminals of each IC functional block and that of supply interconnects.

With reference to the diagram of a generic µC shown in Fig.1, functional blocks can include a digital core section, memories, analog-to-digital (ADC) and digital-to-analog (DAC) converters, timers and counters, input/output (IO) ports, serial communication interfaces and oscillator circuits. Variations in the functional blocks may exist from one manufacturer to another. Non-functional blocks within the µC in Fig.1 consist of the passive power supply interconnects composed of traces routed at chip-level, bonding wires and package lead-frame conductors.

The impedances between supply connections for each block have been computed as explained in what follows and then they have been assembled together to form a complete model for the whole µC. To be able to simulate emission properly, the model also includes the parasitic network of the semiconductor substrate.

2.1 Functional Block Models

In this work, the impedance seen between the supply terminals of the analog blocks have been derived from small-signal AC simulations performed at the transistor-level of each block with their input and output ports loaded with the equivalent impedances of the connected circuits. The analog sections, in fact have limited die-sizes that allow designers to perform low-time consuming simulations. The model of analog blocks is shown in Fig.2(a). Different circuit parameters can be computed by modifying configuration inputs (if present) to analyze the impact on EMEs of a specific operating mode of the block. The model of the IO ports has also been derived from transistor-level simulations performed at the supply pads and with the aim to simulate the impact of core activity on the conducted emissions delivered through IO ports, the circuit model of IOs also includes the impedance seen from the output terminals. Fig.3 shows

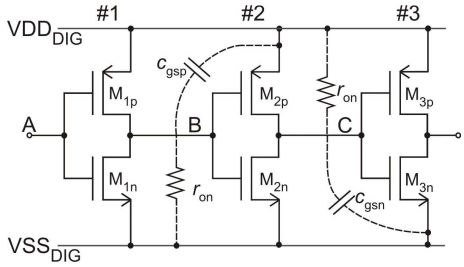

Fig. 4. Inverter chain

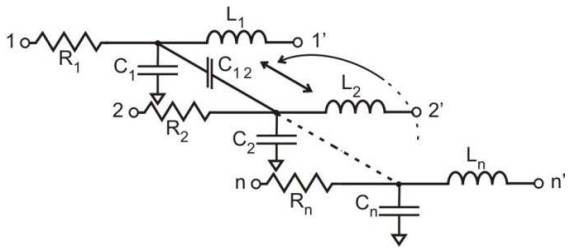

Fig. 5. Per-unit-length MTL model of a package-frame and bonding wire structure having *n* terminals.

three different equivalent circuits for IO ports that can be obtained by small-signal simulations for different output logic levels.

The model of the digital blocks is shown in Fig. 2(b) and it has been obtained with reference to the chain of the three inverters shown in Fig.4. With logic input A=1, transistors M_{1n}, M_{2p} and M_{3n} are on and they operate in the resistive region, while M_{1p}, M_{2n} and M_{3p} are switched off. M_{1n} provides a low resistance path (r_{ON}) from node B to VSS_{DIG}, thus placing the gate-source capacitance of M_{2p} between VDD_{DIG} and VSS_{DIG}. Similarly, M_{2p} connects the C_{gsn} of M_{3n} between VDD_{DIG} and VSS_{DIG}, while with A=0 the role is reversed. Focusing attention on the inverter #2, the average ratio $K_{eff(inv)}$ between the effective capacitance $C_{eff(inv)}$ at its power terminals and the total inverter capacitance $C_{tot(inv)}$ can be derived as

$$K_{\text{eff(inv)}} = \frac{C_{\text{eff(inv)}}}{C_{\text{tot(inv)}}} \cong \frac{p_0 C_{\text{gsp}} + p_1 C_{\text{gsn}}}{\sum_{j=\text{p,n}} \left(C_{\text{gs}_j} + C_{\text{gs}_j} \right)} = \frac{p_0 C_{\text{gsp}} + p_1 C_{\text{gsn}}}{C_{\text{OX}} A_{\text{C}}}$$

where A_C is the sum of the transistor channel areas (WL) and p_0 and p_1 are the probability that the inverter will operate with 0 or 1 at its input [6]. Supposing that the inverters have been designed for equal rise and fall time delays using nMOS and pMOS transistors with threshold voltages $V_{THn}=|V_{THp}|$, then [7]

$$r_{\text{on}} = \frac{1}{k_{\text{n}}(\text{VDD}_{\text{DIG}} - \text{V}_{\text{THn}})},\ k_n = \mu_{\text{n}} C_{\text{OX}} \frac{W_{\text{n}}}{L_{\text{n}}}$$

The model of the generic *i*-th digital block with area A_i has been obtained with reference a simplified architecture composed of N cascade elementary inverters each with area A_{inv} powered by the same supply rail. Capacitance C_c and resistance R_c in Fig.2(b) are $C_c=C_{ox}NK_{eff(inv)}A_C$ and $R_c=r_{on}/N$, where $N=A_i/A_{inv}$. Such a procedure simplifies the derivation of the model of large blocks assuring a reliable estimation of the required impedance.

2.2 Model of the Interconnects

Interconnects, together with the substrate parasitic coupling, are the main reasons for disturbance coupling between the µC blocks and they also contribute to the

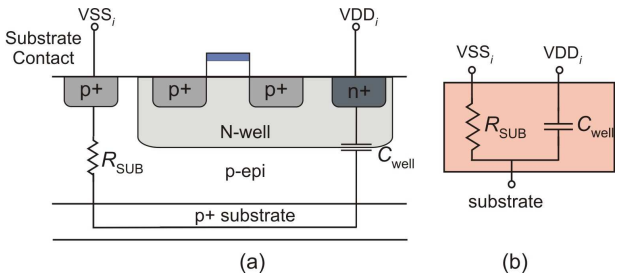

Fig. 6. (a) Cross-section of a low-resistivity CMOS process; (b) substrate coupling model.

impedance seen between power terminals. In order to take into account distributed effects on these interconnects due to the ever-increasing scaling trend, both the on-chip supply lines and the package frame have to be described by a RLC per-unit-length multiconductor transmission line (MTL) model. As far as the model of conductors routed on silicon is concerned, a MTL circuit can be derived from the technology cross-section geometry and layout design by applying simplified but accurate formulas or using specific simulation tools [8]. The models of package lead-frame and bonding wires, due to their complex geometry, can be derived from quasi-static electromagnetic simulations or characterization measurements. Fig.5 shows an example of a section of a per-unit-length MTL model that can be employed for both the on-chip conductors and the package lead-frame.

2.3 Substrate Model

The parasitic coupling between the power supply connections of core circuits with those of different IC building blocks through the common semiconductor die can represent an efficient propagation path for conducted disturbances. Major concern arises in modern CMOS technologies, which in order to avoid latch-up issues, employ a heavily doped substrate covered by a lightly doped epitaxial layer with the same polarity. Since the substrate has a very-low resistivity and it can be regarded as an equipotential node, power supply currents easily flow through the substrate thus inducing coupling among different on-chip blocks.

The model of such a coupling mechanism is shown in Figs.6 (a) and (b) where the R_{sub} describes the resistive coupling due to substrate contacts and the C_{well} represents the capacitive coupling due to reverse-biased isolation junctions. R_{sub} and C_{well} can be derived by analyzing the layout and the technological characteristics of each block (e.g. cross-section geometry and doping profile) and by taking into account the number of substrate contacts [9].

The model of the PSN at chip-level also should include electrostatic discharge (ESD) protections and filler decoupling capacitances that contribute to the PSN impedance with an equivalent decoupling capacitance.

Finally, Fig.7 shows the schematic circuit of the PSN of the generic µC in Fig.1 obtained by assembling the circuit models of each building block derived by the previously described methodology. In order to describe the switching activity of the µC, the model of the Fig.7 also includes the current source I_0 connected to the core section.

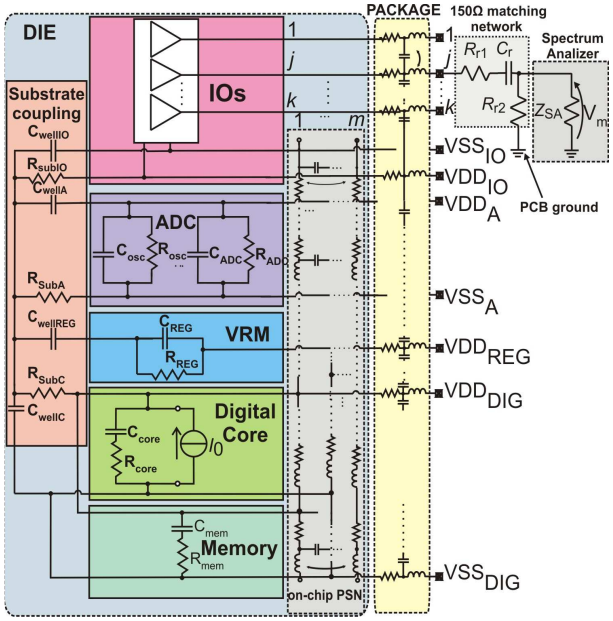

Fig. 7. Schematic Circuit of a µC model.

3. MODEL VALIDATION

The methodology for modeling the IC PSN has been validated by measuring the S-parameter at external ports of an 8-bit µC and then comparing experimental results with model simulations in the 1MHz to 1GHz range.

The µC has been programmed in order to have the central-processing-unit (CPU) and peripheral clock stopped and all the IO ports have been configured to output a low logic level. Circuit model of the µC functional blocks has been derived as described in Section 2 with p_0=p_1=0.5 and $K_{eff(inv)}$=0.25. Package MTL model has been derived from quasi-static electromagnetic simulations [10].

A two-layer PCB (FR4 material, ε_r=4) containing only the µC has been designed and fabricated to perform S-parameter measurements. Measurements have been carried out by employing a two-port 50Ω network analyzer connected to the µC pins through ground-signal (GS) microwave PCB probes calibrated by the short-open-load-thru (SOLT) procedure.

Supply voltage (VDD=3.3V) has been provided during the measurements to the µC through the microwave probes using the bias-tee feature of the network analyzer while all the VSS pins have been connected to the PCB ground reference voltage. Fig.8 shows, for example, the comparison between measured and simulated open-circuit impedances obtained from measured S-parameters of the two-port network consisting of the VDD_{REG}-VSS port (port 1) and the VDD_{IO}-VSS port (port 2) when all the remaining µC pins have been left open (see Fig.7). The sensitivity of model parameters on the simulations has been investigated with the aim of reducing the complexity of the models.

4. PREDICTION OF CONDUCTED EMISSIONS

The proposed model has been employed to compute the conducted emissions induced by core switching activity and delivered through the IO terminals of the above

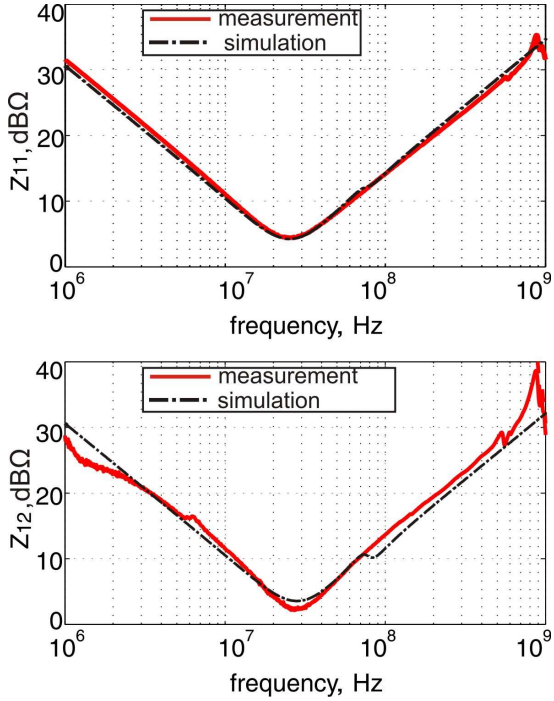

Fig. 8. Measured (continuous line) and simulated (dot-dashed lines) open-circuit impedance parameters

described µC. The device has been programmed in order to exercise the digital core while the timers have been activated to count inside an infinite loop. Operations are synchronized to the frequency of the internal oscillator and no external oscillator is required. Finally, the IO ports have been configured to output a low logic level.

Conducted emission measurements have been performed at IO pins by using the same PCB cited in Section 3. The input port of a spectrum analyzer has been connected to the output port of the 150Ω matching network, as prescribed in the part 4 of [11] through a GS probe and the spectrum of the voltage developed across the spectrum analyzer input impedance has been measured.

The µC activity has been described by an I_0 current source with a triangle-shaped pulsed waveform. Fig.9 shows the comparison between the measured spectrum at an IO output port of the µC and the model predictions.

5. CONCLUSION

In this work a circuit model of a µC PSN has been extracted with the aim to provide insight into the EME performances at the chip and the package level. The model has been derived by performing transistor-level small-signal simulations, by considering layout and technology parameters and by carrying out electromagnetic simulations. By employing the proposed model, IC designers can evaluate the effects on the EMEs that come from different noise coupling paths existing between the internal building blocks and the effects of design modifications on the delivered EMEs can be taken into account easily.

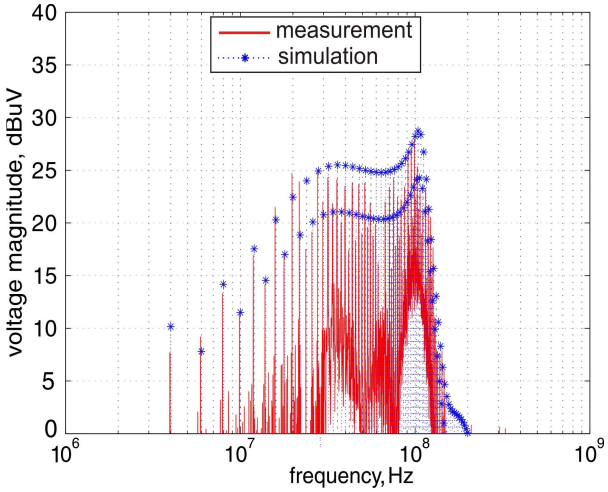

Fig. 9. Measured (continuous line) and simulated (star marks) conducted emission spectra at an IO port of the µC

6. ACKNOWLEDGEMENT

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