A New Grounding Scheme to Reduce the Electromagnetic Emission of Smart Power SoCs

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***Abstract*—The paper deals with the electromagnetic emissions of smart power System-on-Chips (SoCs). The propagation of core-logic switching noise through the silicon substrate and through the package lead-frame is investigated and the effectiveness of three different substrate grounding solutions to attenuate conducted emission is proved by means of computer analyses and experimental tests.**

I. Introduction

In the last decades, the strong development of semiconductor technologies has led to smaller and more performing electronic units that often include a microcontroller, analog, digital and power front-end devices for sensing and control purposes. With the aim of increasing the performance and the reliability of electronic systems, while reducing the production costs, such analog, digital and power front-end circuits are often integrated in a single chip, usually called ”smart power SoC” or front-end ASICs (see Fig. 1).

Smart Power SoCs are often directly connected to sensors and actuators through printed circuit board (PCB) traces and cables, so that disturbances originated by on-chip switching circuits (charge pumps, power transistors and core logic gates) drive such interconnects that behave as unintended antennas delivering unwanted electromagnetic emission (EME). While the electromagnetic emission originating from switching power transistors directly connected to cables can be easily figured out, that related to on-chip switching circuits (e.g. core logic gates) could be difficult to explain.

To this purpose, the parasitic coupling of analog and digital building blocks of such SoCs with the power sections through the silicon substrate and through the package parasitic elements should be taken into account. For this reason, the paper analyzes the parasitic coupling among components integrated in the same SoCs through the silicon substrate, and based on that, a new grounding scheme to reduce electromagnetic emissions is proposed.

The paper is organized as follows: Section II summarizes some important issues of smart power technology processes, while Section II-A shows an equivalent circuit describing the parasitic coupling of components through the silicon substrate. Section II-B describes a new grounding scheme that significantly reduces electromagnetic emissions of smart power ICs. Section II-B shows the procedure we followed to build up an electric EME equivalent model of a real smart-power SoC. In section IV, experimental results that prove the effectiveness of the proposed solution are shown and finally, Section V draws some concluding remarks.

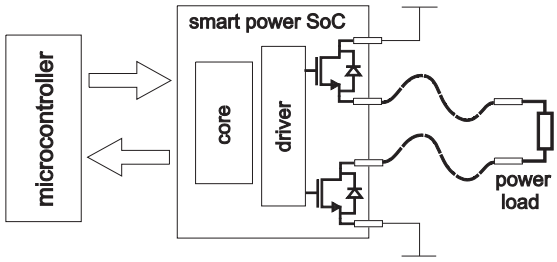

Fig. 1. Electronic unit including a smart power SoC.

II. Electromagnetic Emission in Smart Power SoCs

As mentioned in the introduction, improvements in mixed-signal technologies, have boosted the integration into a single chip of power, analog and digital sections, leading to lower costs and improved performance. In this context, the technology process to be employed for the design of application specific ICs should be carefully selected, in order to fulfill both electrical and thermal specifications, as well as intra-compatibility issues, while keeping the overall chip area at a minimum. For this reason smart power technology processes can be qualified through several basic features among which the list of available components (design kit), voltage classes, lithography and substrate isolation type [1]. Currently, junction-isolated processes are largely used in mass production because of their low cost, even though they are critical in terms of substrate parasitic coupling (latch-up, parasitic bipolar transistors), high temperature and leakage currents. Such problems can be overcome with silicon-on-insulator (SOI) technology processes, in which oxide isolation is exploited. As a drawback, SOI processes show greater thermal resistance and higher production costs. Both technologies show a parasitic coupling of surface components through the silicon substrate that could be effective at high frequency affecting the EMC performance of such ICs.

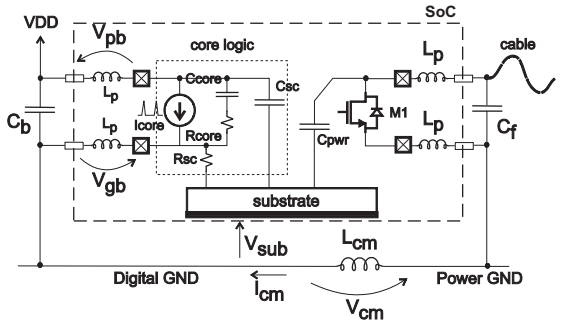

Fig. 2. Simplified schematic view of the parasitic substrate coupling in common smart-power system-on-chips.

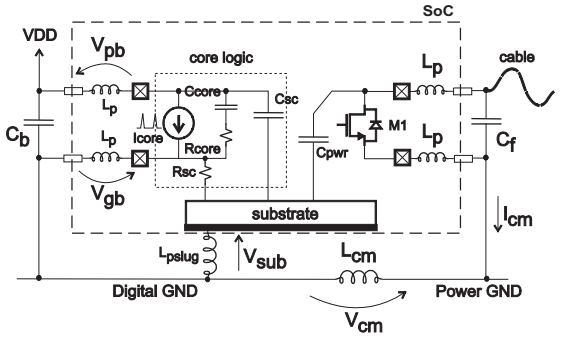

Fig. 3. Substrate to ground connection.

A. Substrate Parasitic Coupling

With reference to junction-isolated process, it should be noted that parasitic coupling among SoC subcircuits takes place through substrate contacts (resistive) as well as through p-n reverse-biased isolation junctions (capacitive) [2] [3]. Based on that, and considering those smart-power SoCs that include at least a digital core block and a power transistor, the parasitic coupling through the silicon substrate can be modeled by the equivalent circuit shown Fig. 2. Here, the digital core is described by a time-variant current source (I_{core}), in parallel with the series of the core capacitance C_{core} and the resistance R_{core}. In this circuit, the capacitance C_{sc} describes the parasitic coupling of core reverse-biased isolation junctions with the substrate, while R_{sc} models the substrate contacts. Similarly, parasitic coupling of a power transistor with the substrate is modeled by the capacitance C_{pwr}. In the same figure, the package model is recalled by means of inductors, that connect pads on silicon (crossed square) to printed circuit board components. Furthermore, this circuit includes PCB level components like the logic gates power supply bypass capacitor C_b, an EMI connector filter (C_f) and the common mode inductance L_{cm}. This last element is strictly related to the PCB layout. With reference to such an equivalent circuit, it can be noticed that a part of the switching current (I_{core}) flows through the common-mode inductance (L_{cm}) so that common-mode EME delivered by cables is experienced. To this purpose, it is worth mentioning that EME spectra are strictly related to PCB parasitic elements (like L_{cm} in Fig. 2), which cannot be controlled or taken into account by IC designers. Nonetheless, it can be observed that most of the switching current sunk by the core block is taken from the internal core capacitance C_{core} and the external bypass capacitance C_b, while only a small part of it is taken from off-chip components and parasitic paths. Switching currents that flow through package interconnections are mostly responsible for electromagnetic emissions, particularly those flowing in the IC power supply interconnects [4], since the ground- and power-bounce they drive could reach all the IC pins through the substrate parasitic couplings. Depending on the overall resistance of substrate contacts of the digital block (R_{sc} in Fig. 2), the current loop that involves the common-mode impedance can be closed (predominantly) either through the V_{DD} pin or through the GND pin. In case of low-resistance substrate contact (i.e. $R_{sc} < 1\ \Omega$), a part of the core supply current flows through the external bypass capacitor C_b and substrate voltage fluctuations are mostly driven by the *ground-bounce* (V_{gb}). On the contrary, for high-resistance substrate contacts, the substrate voltage fluctuations are mostly driven by the *power bounce* (V_{pb}). In both cases, the substrate is involved by unintentional current loops that drive electromagnetic emission.

B. Mitigation of IC EME

In order to reduce the magnitude of the common mode current, which is mostly responsible for EME, different strategies have already been explored, among which:

- use of package with reduced size and/or increased number of parallel power supply and ground pins to reduce the equivalent inductance of power supply loops [6],
- increment of on-chip bypass capacitor to reduce the magnitude of the current flowing through package interconnects [7],
- use of circuit topologies and proper architecture of digital building blocks for power supply current shaping [8],
- use of proper grounding topologies which reduce substrate voltage bounce [5].

This paper points out through the analysis of experimental tests and computer simulation results the key role played by the silicon substrate on the propagation of switching noise in smart-power SoC. To this purpose the effect of connecting the die backside contact to the PCB ground has been explored. This additional connection, which is described in Fig. 4 by the parasitic inductance L_{pslug} acts as a current shunt, preventing the switching noise current to flow through the common mode inductance L_{cm}, thus reducing EMEs. In this circumstance the digital ground pin should not be connected to the PCB ground avoiding the ground bounce to drive common mode currents. Unfortunately, the mutual coupling of package parasitic inductances reduces the effectiveness of this decoupling method, especially at higher frequencies. For this reason, the way the package realizes the substrate contact significantly affects the emission level.

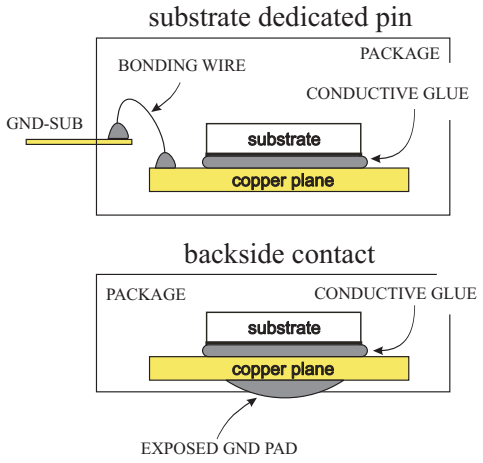

Fig. 4. Substrate Grounding.

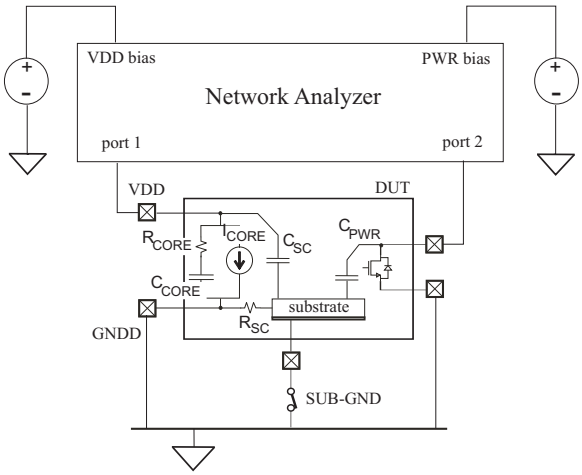

Fig. 5. S-parameter Measurement Setup.

III. Substrate Grounding

With the aim to analyze the effect of different substrate grounding solutions on the EME of smart power SoCs, two identical integrated circuits encapsulated into the same package type, with and without an exposed backside pad, have been considered. In particular, the substrate of the first device under test (DUT) has been grounded through one of the package pin, which has been connected to the die backside with a down-bond, while in the second DUT, the die backside is directly accessible for soldering on the package backside, as it is sketched in Fig. 4. Based on that, three different solutions for substrate grounding have been considered:

(a) substrate connected to ground by means of metal-substrate contacts through the GND pin of core logic gates,
(b) die backside contact connected to ground through a dedicated pin,
(c) die backside contact connected to ground through an exposed package backside pad.

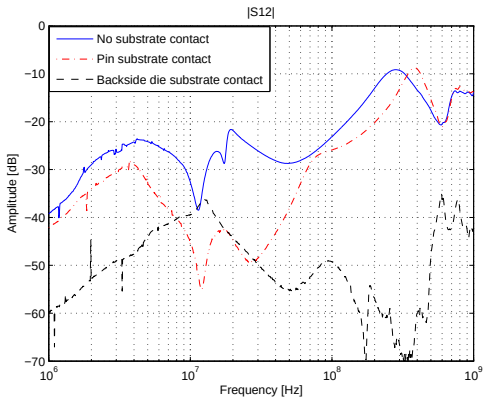

Fig. 6. Transmission scattering parameters for different substrate grounding.

These DUTs have been mounted in identical test boards, making their pins accessible through RF probe contacts. The digital GND pin has been tied to the PCB ground. Then, the scattering parameter matrix between the digital core power supply port and the drain contact of one of the SoC power transistors has been measured by using the Network Analyzer HP8753E. The above mentioned substrate grounding connections have been considered for experimental tests, which have been carried out providing to the DUT input and output ports proper DC bias voltages (see Fig. 5). Furthermore, to avoid the measurement being affected by time-variant current absorption of switching logic gates, the input clock signal has not been provided to the DUT and the clock input pin has been connected to ground. S-parameter measurements have been performed for each one of the above mentioned substrate grounding scheme, and it has been found that the transmission of RF power from the logic core to one of the power transistor is significantly reduced if the package backside ground contact is connected to the PCB ground, as it is highlighted by the plots in Fig. 6. This result leads to conclude that the more the substrate is "well-connected" to ground (high-doped substrate), the less the switching noise is allowed to spread all around the integrated circuit. This statement has been proved through several experimental tests carried out on the same smart power IC, which has been considered for S-parameter measurements.

IV. Test Results

The measurement of IC conducted emisison has been carried out referring to the international standard IEC 61967-4 (150 Ω method) that requires measuring the voltage spectra at IC pins while the IC switching circuits are running. In particular, the DUT terminals of embedded power transistors, which are not connected from the switching building blocks (i.e. core logic gates), have been considered and measurements have been performed referring to a test setup like that shown in Fig. 7. Here, the power supply ($V_{DD} = 3.3\ V$) and the clock signal ($f_c = 8\ MHz$) are provided to the DUT, and conducted emissions are measured by means of a 150Ω-to-50Ω resistive matching network, a 32dB low-noise amplifier

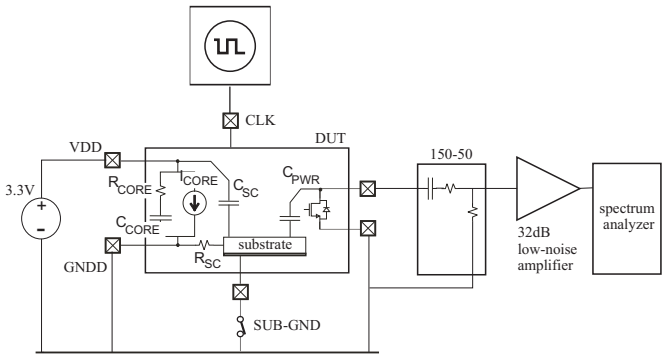

Fig. 7. Set up for conducted emission measurements compliant to IEC61967-4, 150 Ω method.

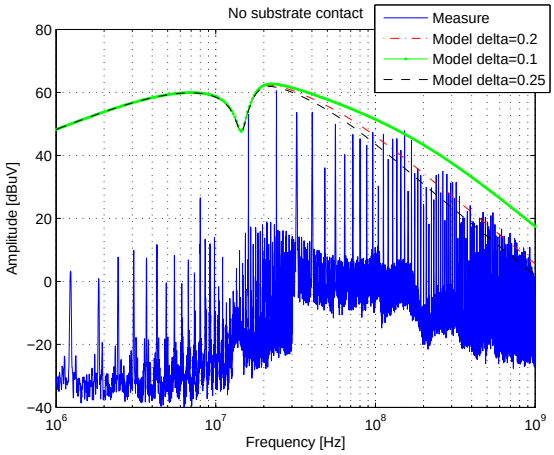

Fig. 8. Conducted emissions measurements with no substrate contact.

and a spectrum analyzer as required in [11].

The measurement of the conducted emission has been performed referring to three samples of the same chip encapsulated similar package lead-frames that differ for the substrate grounding scheme. In particular, the spectrum reported in Fig. 8 refers to the case of the silicon substrate grounded by the logic core ground pin, that in Fig. 9 was obtained with the substrate grounded through a dedicated pin and finally Fig. 10 refers to the case of substrate backside connected to ground by means of a backside exposed pad. Basically, these test results confirm the conclusion that has arisen from the S-par measurements.

In addition to the above shown analyses, an electrical model that looks like that shown in Fig. 3, but including additional ports, has been derived. It is made of the package model [9], the substrate model [2], the macro-model of the core-switching gates and the electrical model of the power transistors. The tools used to evaluate the model parameters are listed in Table I. In particular, the core macro-model parameters (C_{core} and R_{core} in Fig. 3) have been obtained on the basis of S-parameter measurements, while the time-varying current source (I_{core}) that describes the core switching activity has been modeled with a triangular-shaped current like that shown in Fig. 11.

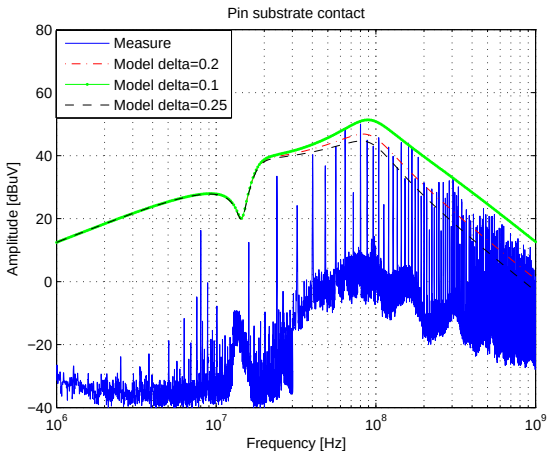

Fig. 9. Conducted emissions measurements with the substrate connected to the PCB GND by means of a dedicated pin.

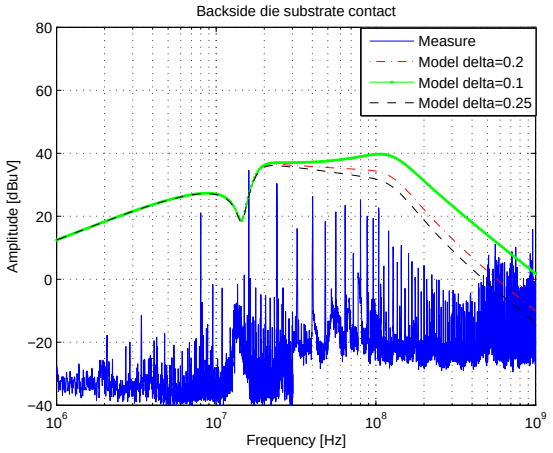

Fig. 10. Conducted emission measurements with a package backside soldering pad connected to PCB GND.

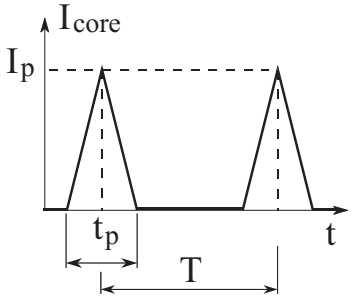

Fig. 11. Basic model of the current sunk by the logic switching gates.

This current has period $T = 1/f_c$, peak value I_p and pulse width t_p that usually ranges from about $\frac{T}{10}$ to $\frac{T}{4}$.
In the ferequency domain, this triangular-shaped current can be expressed as

$$I_c(f) = I_p \cdot \frac{t_p}{T} \cdot sinc^2\left(\frac{t_p}{2} \cdot f\right) \cdot \left[\sum_{n=1}^{+\infty} \delta\left(f - \frac{n}{T}\right)\right], \quad (1)$$

TABLE I
TOOLS AND METHODS USED TO DERIVE THE MODEL PARAMETERS.

Parameter(s)	Evaluation Method
R_{sc}	DC measurement
C_{sc} and substrate network	Layout view and tech. parameters
power transistor	Layout view and tech. parameters
Package Model	Ansoft Q3D Extractor
C_{core}, R_{core}	S-parameters
I_{core}	DC measurement & Math. model

where I_p is related to the waveform mean value, i.e. the DC current consumption of the core switching gates, by

$$I_{DC} = \frac{1}{T} \cdot \int_0^T i_c(t) \cdot dt = \frac{I_p}{2} \cdot \frac{t_p}{T} \Rightarrow I_p = 2I_{DC} \cdot \frac{T}{t_p}. \quad (2)$$

Substituting (2) in (1) and using the parameter $\Delta = \frac{t_p}{T} = t_p \cdot f_c$, the current spectrum envelope can be expressed as

$$I_c(f) = 2I_{DC} \cdot sinc^2 \left(\frac{\Delta}{2 \cdot f_c} \cdot f \right). \quad (3)$$

The asymptotic plot of this current spectrum is flat up to the cutoff frequency at $f_p = \frac{2f_c}{\Delta}$ then it rolls off at $-40\ dB/dec$. The prediction of this circuit model is shown in Figs.8, 9, 10 by continuous and dashed lines. In particular, the continuous lines, the dash-dotted lines and the dashed lines have been obtained for $\Delta = 0.1,\ 0.2,\ 0.25$ respectively, while keeping the mean-value of the source current at the constant value $\overline{I}_{core} = 2$ mA.

On the basis of these results, it can be concluded that the attenuation of conducted interference obtained by a proper ground connection of the silicon substrate can be significantly greater than that usually achievable through the power supply current spreading.

V. CONCLUSION

In this paper, the propagation of switching noise in Smart Power SoC through unwanted parasitic paths has been investigated and different substrate grounding schemes have been considered with the purpose of reducing electromagnetic emission.

The experimental tests performed within this work have shown that conducted emissions can be significantly reduced if the die backside is connected to the PCB ground layer through a low-impedance (at low and at high frequency).

Finally, a macromodel that describes the parasitic coupling of components of the same SoCs has been presented and it has been shown that the reduction obtained by the substrate grounding can be significantly greater than that usually obtained by spreading in time the core-block current consumption.

VI. ACKNOWLEDGEMENT

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