An Effective Way of Testing the Susceptibility to EMI of Custom ICs

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***Abstract* — The paper presents the result of investigations carried out in the development phase of an IC to evaluate its susceptibility to EMI. The IEC-62132 and the ISO standards 11452-4 are considered, and a non-standard test board that makes the DUT in a contest similar to that of the application board has been designed and fabricated. The main advantages of this unusual solution with respect of classic ones are presented. The test vehicle for this analysis is an automotive power train product: an inductive load pre-driver that includes several power channels. DPI and BCI test result are shown and discussed.**

1. INTRODUCTION

In the last decades, the strong demand for electronic systems to be employed in automotive applications and the continuous development of semiconductor technology processes have boosted the design and fabrication of application specific integrated circuits (ASICs) including analog, digital, power and RF blocks that drastically reduce production costs while increasing system performance and reliability.

Basically, design issues to fulfill module level specifications have gradually shifted from printed circuit board (PCB) to integrated circuits so that current IC design (especially custom ICs) are mostly performed to fulfill most of module level specs including those dealing with electromagnetic compatibility.

Actually, maximum limits for conducted and radiated electromagnetic emissions of electronic modules cannot be easily related to electrical parameters at IC level like DC current consumption, clock frequency, IC package physical size, I/O voltage and current slew rate, etc.. Similarly, the level of RF disturbance to be applied to an electronic module to check its susceptibility to electromagnetic interference (EMI) cannot be treated like any other design specification.

In general, both electromagnetic emission and susceptibility of ICs are strongly related to the surrounding environment they operate, i.e. PCB layout, EMI filters, PCB grounding scheme, size and shape of metal case etc. However, in the last decades several methods for measuring the electromagnetic emissions and the susceptibility to EMI at IC level have been presented and some of them have been included in international standards [1].

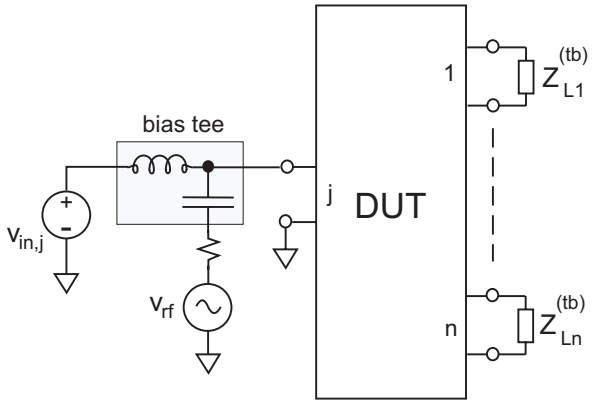

Fig. 1 RFI superposition to a DUT nominal input signal with the DPI method

To this purpose, documents like IEC-61967 and IEC-62132 include several recommendations regarding test-setup design, measurement procedures and instruments setting, which are useful to achieve good repeatability as well as good accuracy. Such methods were originally proposed to compare the EMC performance of ICs implementing the same functions (executing the same code) while operating in the same environment (the test setup).

Nowadays, such measurement methods are largely used to address EMC issues in the early stage of the design, although IC emission and susceptibility are usually affected by application design choices and parasitic elements. As a consequence, an IC that fulfills chip level EMC specifications can make module-level EMC tests to fail. Such a problem becomes relevant in the development of complex custom ICs whose design flow requires chip level EMC tests on the 1st silicon issue with

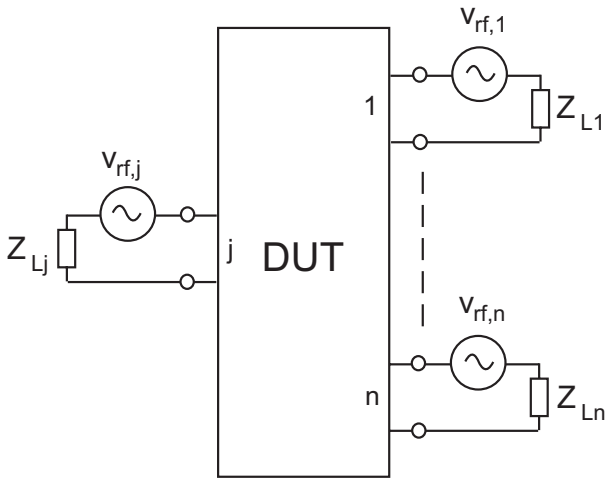

Fig. 2 Equivalent circuit describing the multiport injection of RFI during BCI tests

the aim of identifying possible design weaknesses to be addressed in the redesign of the 2nd silicon.

Based on that, and being the redesign to be performed in a tight timeframe, the paper shows how EMC measurement at module level can be employed to check the EMC performance of ICs even if the application board has not been completed yet.

In particular, the measurement of IC susceptibility to EMI is discussed referring to the direct power injection (DPI) method while the bulk current injection (BCI) method is considered for module level susceptibility tests.

The paper is organized as follows: in Section 2 and 3 the DPI and BCI measurement methods are described referring to the IEC and ISO standards. The operation of the device under test (DUT) and the main characteristics of the test board used in the experimental tests are described in Section 4 and Section 5 respectively, while Section 6 shows the results of DPI and BCI tests. Finally, Section 7 draws some concluding remarks.

2. DPI VERSUS BCI

As mentioned in the introduction, the susceptibility to EMI of ICs is usually related to the surrounding environment they operate or equivalently the off-chip impedance loading each IC pin. As a consequence, common test procedures like those described in [1] require the device under test (DUT) to be mounted in a test board that complies with several design constraints. In this way, possible unintended interactions of the DUT with the test board parasitic elements should be avoided and ICs performing the same function can be compared. Such test boards allow one to perform both conducted (DPI method) and radiated (TEM cell method) susceptibility tests because the DUT is mounted above a ground plane while IC pins to be tested against conducted interference are connected to bias tees like that shown in Fig.1.

With reference to a given set of susceptibility criteria, the DUT is made executing repeatedly a well defined bunch

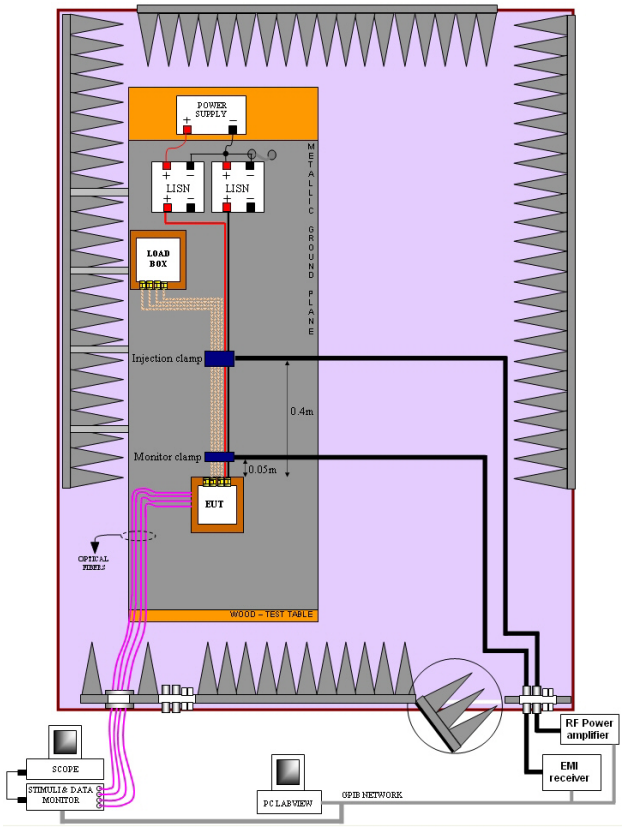

Fig. 3 BCI test setup.

of functions while RFI is added to its nominal signals. In this framework, the DPI method requires adding RFI to one pin at time, while having all the remaining pins loaded by known impedances ($Z_{Li}^{(j)}$).

The value of such impedances should drop within a given range since the interference added to the j-th pin propagates throughout the chip reaching all the remaining pins not directly driven by the RFI source. Based on that, the DPI method, which is intended as a single-pin susceptibility test, is actually a multi-pin injection so that the off-chip impedances influence the DUT immunity level.

Conversely, module level susceptibility tests like the bulk current injection method (BCI) requires adding interference to nominal signals in the form of common mode interference, by means of an high frequency transformer (the injection clamp), that magnetically couples the RF source with a bundle of cables of the module under test. As a result, RFI reaches integrated circuits but in this case most of IC pins are simultaneously interested by RFI as it is sketched in Fig.2 (all pins in principle). To this purpose it is worth mentioning that in this test, the magnitude and the phase of each equivalent RF source superimposed to IC nominal signals depend on several parameters among which, PCB layout and grounding, EMI connector filtering, IC input impedance etc..

On balance, the DPI test setup is far from emulating any real application environment and furthermore, it is required to add the interference to one DUT pin at time, while in module level susceptibility tests, like BCI,

interference is added simultaneously to several DUT pins (all pins in principle). On the basis of these considerations and knowing that any IC can be modeled as a multiport nonlinear network (the superposition principle is not applicable), it can be easily concluded that DUT failures observed in DPI tests can difficultly take place in module level BCI tests, and vice versa. As a consequence, what follow focuses on the bulk current injection method even if the test board, which has been developed to this purpose, includes all the circuits and connectors needed for DPI tests.

3. BCI TEST SETUP

With the aim of comparing the susceptibility to EMI of the same DUT by means of the DPI and the BCI test method, a proper test board has been designed and fabricated. This test board is a part of the BCI test setup, as it is sketched in Fig. 3 (into the EUT), where the "remotely grounded" configuration is employed. To this purpose, two LISNs, which are loaded by 50Ω terminations, have been used to provide to the DUT a proper power supply.

The whole system has been accommodated into an automotive certified anechoic chamber. On a wood table, a metallic plane has been positioned. The power supply of the system is provided by a standard lead acid battery, similar to the one normally used in the car. Through two LISN, the positive and negative connections (about 1 m length) reach the EUT. These last together with the wires needed to connect the loads, are grouped and fixed to a wood support to maintain the harness at 5cm above the ground plane. The injection clamp and the monitoring clamp are positioned at 40 cm and 5 cm from the EUT box, respectively. Being the EUT usually screwed to the car chassis, it has been decide to connect the EUT metal case to the ground plane. This test setup includes a load box that is made of a metallic case containing the loads needed to make the DUT working like in a car. The load box metal case is electrically connected to the ground plane. In order to provide to the DUT the input signals needed for its operation and to monitor a set of output signals that highlight possible EMI-induced failures, a set of optical transceiver has been included in the above mentioned test board. The communication of the EUT with the control systems and the measurement instrumentations takes place through optical fiber avoiding any unintended common mode path.

Outside the chamber a PC, through a GPIB network, drives the RF equipments (RF signal generator, power amplifier and EMC analyzer) and interfaces the oscilloscope and the stimuli generator. A Computer executing an ad hoc software controls the RFI frequency and magnitude while monitoring the DUT operation. The test bench is fully automated.

4. THE DEVICE UNDER TEST

The device under test is a multi pre-driver IC made up of a digital sequencer, a timing unit and a set of pre-driver that control the switching of off-chip MOS power

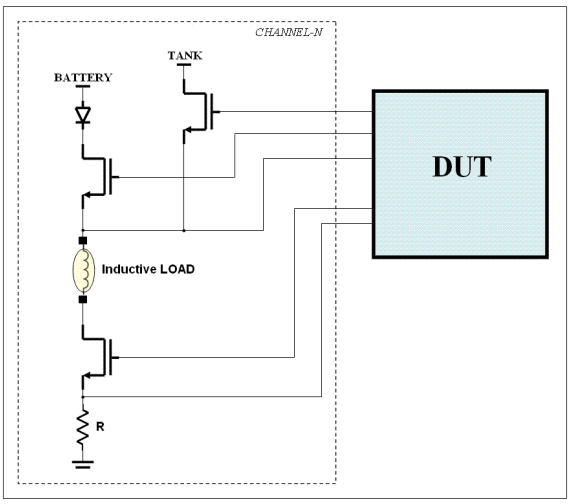

Fig. 4 Schematic of the circuit feeding the inductive load that includes the DUT.

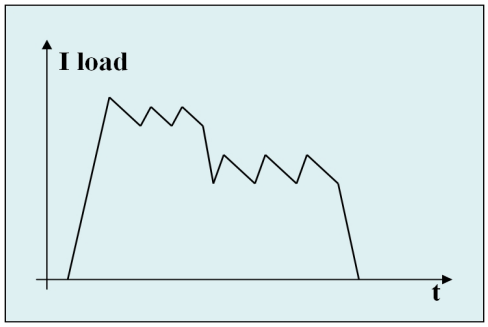

Fig. 5 Typical load current profile.

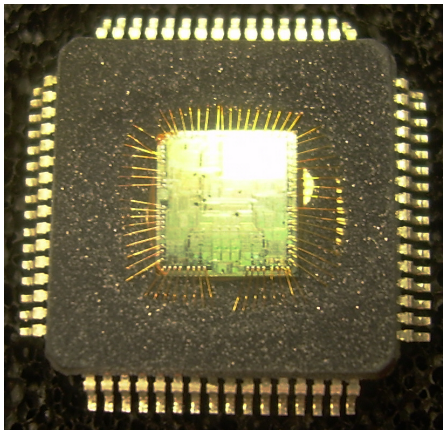

Fig. 6 DUT photo.

transistors. The DUT was specifically designed to drive the inductive loads of an automotive application. It includes a peak & hold current control and a DC/DC step-up converter that provide full protection and diagnosis in case of hardware faults and malfunctions. In Fig. 4 a schematic picture of a driving channel is shown.

The device can be programmed and controlled by a microcontroller through a serial interface (SPI). In this application diagram, below the low side transistor a sensing resistor is present. The voltage drop across this resistor is read by an internal sensing and it is used by a programmable FSM to control the load current, according

to the current profile defined by the microcontroller. A typical peak & hold current profile is shown in Fig. 5. The device (Fig. 6) was designed and fabricated referring to a 0.35um CMOS ST proprietary technology process.

5. TEST BOARD DESCRIPTION

A dedicated board for the BCI and DPI immunity tests has been used (Fig. 7). The board is designed as much as possible similar to the application ECU, in terms of electrical schematic, components placement and routing. The board dimensions, case and connectors are the same of the real application ECU. The expected benefit of this design is to relate the immunity test results performed on this test board with the behavior of the DUT on the real application ECU. The board is made up by a four-layers PCB with the DUT custom IC and the other devices mounted on its top layer. On the PCB bottom layer, only passive components are placed. On the board are present also the devices needed to supply and communicate with the DUT and the power components driven by the DUT, used to actuate the external inductive loads. The logic needed to program and to control the DUT during the susceptibility tests is placed outside the board, to avoid potential immunity issues of the control logic itself. The communication between the control logic and the DUT is performed through an optical interface carrying the SPI signals and the I/O digital signals used for the load actuation.

The board is connected to negative reference of the battery supply through a dedicated pin of the connector.

This pin acts as the centre of a PCB "ground star" on which two ground planes are connected: the first, covering the whole PCB, is related to the digital and power devices (DUT, passive power components, power supplies, communication interfaces, etc.) and the second, referred as "RF ground", is placed under the board connector, used for the RF decoupling capacitors located near the connector pins. Moreover, a separated ground ring is present on the border of the board, connected to the RF ground plane through a RC decoupling network. The ECU case contacts this ground ring, and acts as a "case ground". More in detail the test board include a set of communication optical interface, a power supply section a load actuation power stage as well as SMA connectors for DPI tests.

5.1 Communication optical interface

An optical interface is used to communicate between the DUT and the control logic. The signals, connected through this interface, are the SPI signals needed to program and to control the DUT during the test execution (to get diagnostic information related to the DUT functionality and the power stage state), and the I/O digital signals, used to actuate the external inductive loads. The electrical signals for/from the DUT are converted into optical signals by the transceivers present on the board; the fiber optics connections are brought outside the anechoic chamber to an interface board, performing the conversion optic/electric and directly connected to the DUT controller. Since the optical transceivers are devices strictly related to the immunity tests execution and they are not present in the real application ECU, their placement and routing has been performed in order minimize the impact on the layout routing in the area around the DUT.

5.2 5V supply stage

The 5V supply needed for the components functionality is generated on the board. To avoid influence of the optical interface stage on the DUT, two 5V linear regulators, supplied by the battery voltage coming from the board connector, are used to generate different 5V for the DUT and the optical interface. The purpose of this architecture is to maintain the DUT and the optical interface supply domains as much as possible independent from each others. The optical interface, in fact, should not be influenced by the DUT behavior during the tests execution.

5.3 Loads actuation power stage

The power stage driven by the DUT to actuate the external inductive loads is present on the board. It is made up of the power mosfets and diodes used to force and control the current flowing through the external loads. Some of the loads used require a "Vtank" voltage higher than the battery voltage. For this reason, the DUT can control a DC/DC step-up converter, used to generate the required voltage starting from the battery voltage. On the board is present the DC/DC converter circuitry driven by the DUT. The supply of the DC/DC step-up voltage, as well as of the inductive loads actuation channels, comes from a "power" battery line present on a dedicated board connector pin.

5.4 RFI injection and probing connectors

The test board is designed to perform BCI and DPI tests. For both tests, the DUT functionality is constantly monitored using the SPI interface, getting the diagnostic information given by the DUT about the external power stage state and the DUT functionality itself.

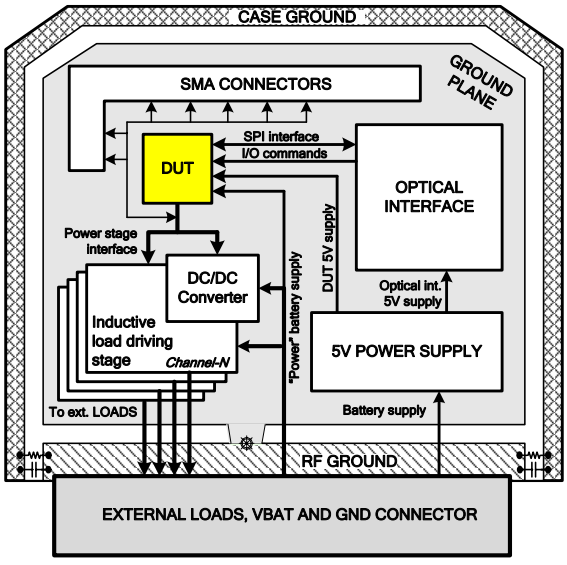

Fig. 7 Test board block diagram.

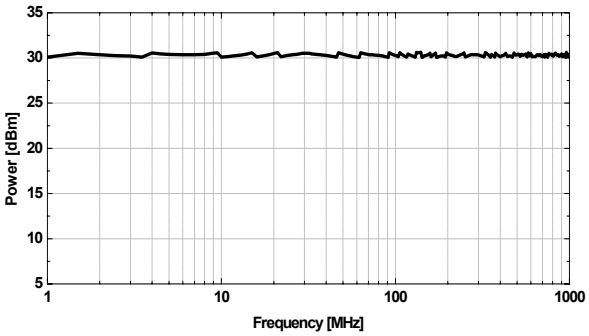

Fig. 8 DPI test results. Incident power versus frequency that refers to the injection of RFI to one of DUT output power pin.

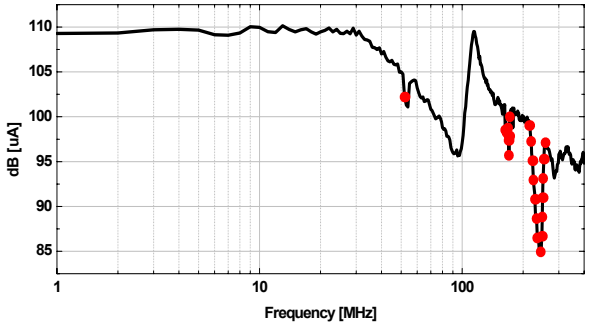

Fig. 9 BCI test results. The Maximum CW RF current flowing through the cable harness that induces DUT operation failures is labeled by the red circles.

Some pads connected to the pins of the DUT are present on the board, to perform a further monitoring of the analog signals. A series of SMA connectors and the related coupling networks are also present on the board, to perform the noise injection on the DUT pins for the DPI tests. Due to this kind of architecture, compliant with the IEC specifications, the board can also be used to perform conducted emissions tests. For these tests, the SMA connectors are used as probes, to measure the conducted noise present on the DUT pins. As described for the optical transceivers, also the SMA connectors and the associated coupling networks are related to the immunity tests execution and, since they are not present on the real application ECU, their placement and routing has been designed in order to minimize the impact on the area around the DUT.

6. MEASUREMENT RESULTS

The susceptibility to RFI of the DUT is evaluated referring to the DPI and to the BCI test methods, and in both tests, DUT operation failures are detected looking at the SDO signal of the SPI interface. Furthermore the load current shape integrity has been checked through an oscilloscope. All these signals have been make available outside the chamber by means of optical links. Any time a violation of these parameters occur, the power injection is stopped, the data are stored and a new cycle at the next step of frequency is launched. At the end a graphs showing the injected current versus frequency is created and failure, if any, is highlighted.

With reference to the DPI test method, measurements have been performed on several pins, one at time, by sweeping the incident power up to 30dBm and the frequency in the range 1MHz – 1GHz and DUT failures never occur. To this purpose, Fig. 8 shows the result of the DPI test performed on a DUT power pin.

On the basis of these results it could be concluded that the DUT is fully immune to EMI hence, no failure should occur in module level susceptibility tests. However, BCI tests, which have been performed on the same DUT, have pointed out several operation failures at around 50 MHz 160 MHz and 240 MHz as it is shown in Fig. 9. In this plot the current magnitude that gives rise to the DUT operation failure is labeled by a red circle.

Basically, the BCI test performed during the development of this smart-power SOC has put on evidence the main design weaknesses to be fixed in the second silicon issue or to be solved at PCB level by a proper use of EMI filters. In this particular case, a simple redesign of the EMI filter at connector level has strongly increased the DUT immunity to EMI. In fact, no failure has been detected on the whole bandwidth up to 300 mA (about 110 dBµA and maximum available power of about 50 W) current injected.

7. CONCLUSIONS

In this paper the results of investigations carried out to check the susceptibility to EMI of a given integrated circuits have been presented. Experimental tests have been performed in the early development phase, just between the 1st and the 2nd silicon, referring to the DPI and the BCI test methods. By these tests it has been found that the same DUT, which is included in a non-standard test board, passes the DPI tests while it fails in BCI tests. This fact, which has been observed for many other devices, has been explained referring to the multiple RFI injection that takes place in BCI tests. Furthermore, it has been observed that a proper design of the test board makes possible identifying the main IC weakness in a very short time to be considered in the following development phases.

8. ACKNOWLEDGEMENT

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9. REFERENCES

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