Design of a new MagFET-based Integrated Current Sensor Robust to EMI

Orazio Aiello
EMC Competence Center
Istituto Superiore M. Boella (ISMB)
Via P. C. Boggio 61, Turin, Italy
aiello@ismb.it

Franco Fiori
Microelectronics EMC Group,
Eln. Dpt., Politecnico di Torino,
C.so Duca degli Abruzzi 24, Turin, Italy
franco.fiori@polito.it

***Abstract* – This paper deals with the susceptibility to electromagnetic interference of CMOS integrated current sensors for power transistor current monitoring. Conventional integrated solution are first considered, hence a new integrated current sensor based on the Hall effect in a split-drain MOS transistors (MagFET) is proposed. The susceptibility to radio frequency interference of a conventional (wired) current sensor and that of the MagFET-based solution is discussed.**

1 INTRODUCTION

Common electronic systems are usually made of several modules that include printed circuit boards (PCBs), discrete components and integrated circuits (ICs). Power and data interconnects in such systems are usually routed through cables, which in turn behave like unintentional antennas collecting electromagnetic interference (EMI) from the surrounding environment.

Although several studies have dealt with the susceptibility of integrated circuits to EMI [1-2], such a topic is far from being completely addressed and deserves further insights. To this purpose, the paper introduces the susceptibility to radio frequency interference (RFI) of common analog, digital and power front-end circuits like those used in Application-Specific-Integrated-Circuits (ASICs), then it focuses on Smart-Power System-on-Chip [3] and in particular on the susceptibility to RFI of conventional integrated current sensors needed for power transistor current monitoring.

Common circuits for current sensing use a small resistor in series with the power transistor that translates the transistor current in a voltage to be further amplified and processed. Other current sensing circuits base their operation on the current mirroring principle: a small transistor (the SenseFET [4-5]) is driven by the same gate-source voltage of the power transistor so that its drain current is proportional to the power transistor current. Such integrated current sensors show low-power dissipation, need reduced silicon area and provide reasonable accuracy.

However, any current sensor electrically connected to power transistor terminals like those mentioned above, is exposed to interference collected by cables. For this reason additional passive filters at printed circuit board (PCB) or at IC level are usually needed. Based on that and aiming at the design of integrated current sensors intrinsically immune to EMI, this paper describes a new current sensor based on the Hall effect, which takes place in a split-drain nMOS transistor (the MagFET) whenever it is surrounded by the magnetic field of the current to be monitored [6].

The paper is organized as follows: Section 2 describes a circuit that implements the current mirroring principle (the SenseFET circuit). Section 3 recalls how magnetic field unbalances the drain current of a splitted drain MOS transistor (MagFET) and shows the operation of the new current sensor developed in this work. Then, Section 4 shows the results of computer simulations carried out to evaluate the susceptibility of the MagFET-based current sensor. These results are compared with those of the SenseFET that operates in the same condition. Finally, in Section 5 some concluding remarks are drawn.

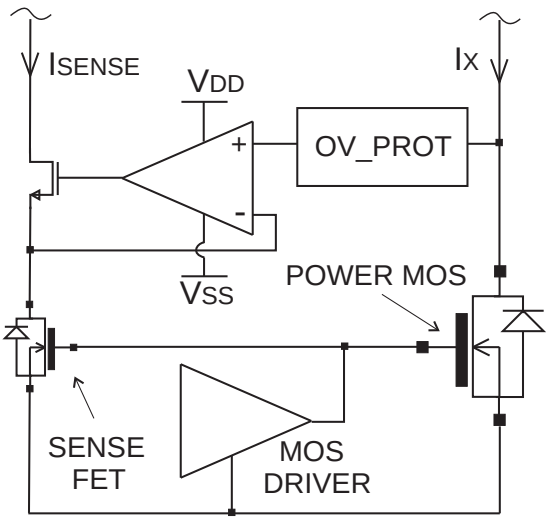

Fig. 1: Current sensor based on the mirroring principle.

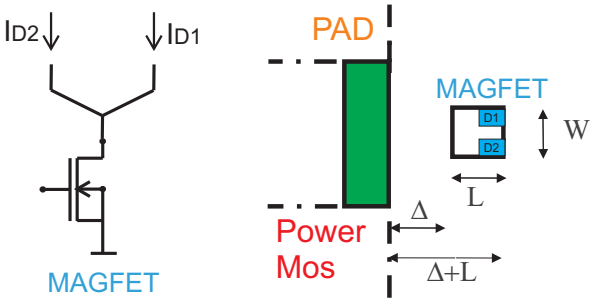

Fig. 2: MagFET symbol and layout view.

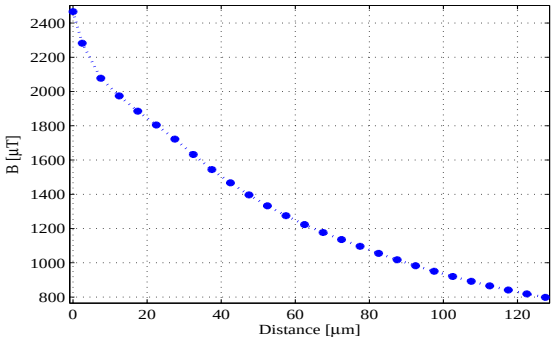

Fig. 3: Vertical Magnetic Field strength vs distance impinging the MagFET. Power transistor current *Ix*=1A.

2 A CONVENTIONAL CURRENT SENSOR: THE SENSEFET CIRCUIT

A common way of sensing the current that flows through a power transistor consists in mirroring it by means of a circuit like that shown in Fig. 1, where an elementary transistor (the SenseFET) of the same type of those used in the power transistor is driven by the same gate-source voltage of the power transistor itself. The SenseFET drain-source voltage is kept equal to that of the switched-on power transistor by means of a voltage follower. Such a bias circuit makes the SenseFET drain current (*Isense*) proportional to that of the power transistor (*Ix*) through a constant mirroring factor, which is given by the ratio of the two transistors areas (transistors with the same channel length are considered). To this purpose, it is worth mentioning that the accuracy of such a circuit is surely limited by the transistor mismatches, which always occurs for high mirroring factor.

However, the accuracy of such a current sensor can be significantly reduced by disturbances affecting the power transistor nominal signals and, for this reason, the possibility of building up a current sensor with no electrical connection with the power transistor terminals and limited bandwidth has been investigated. To this purpose, the idea of monitoring the power transistor current by sensing the magnitude of the related magnetic field has been considered.

3 A NEW CURRENT SENSOR BASED ON THE MAGFET TRANSISTOR

An alternative way of monitoring the power transistor current is that of sensing the magnetic field, which is related to such a current, through the Hall effect that takes place in the channel of a MOS transistor surrounded by the magnetic field. To this purpose, let's consider a splitted-drain MOS transistor (MagFET) placed very close to a metal strip which carries the current to be monitored, and let's further assume such a sensing transistor biased in saturation. In this condition, the power transistor current gives rise to the magnetic field that induces a Lorentz force on the electrons that flow from the source to the drain in MagFET channel: in fact, the split-drain currents are imbalanced by the Hall effect. To this purpose, previous works [7-8] have shown that the current unbalance (ΔI) can be expressed as

$$\Delta I = S_I I_B B_\perp = S_I I_B F_c I_x \qquad (1)$$

where I_B is the split-drain MOS bias current (I_{D2}+I_{D1}); F_c is a conversion factor defined as the ratio of the magnetic flux lines density over the split-drain transistor to the current (Ix) flowing through the metal strip current. Furthermore, S_I is the MagFET sensitivity that depends on the geometry of the device (length L and width W), and that can be written as

$$S_I = \frac{1}{2}\mu_{Hch}\frac{L}{W}G_H \,. \qquad (2)$$

In this expression, G_H is a geometrical correction factor (G_H=0.676 for square transistor that maximizes the sensor sensitivity) and μ_{Hch} is the Hall carrier mobility given by the product of the effective carrier mobility μ_n (process-based) and the Hall factor r_H. This last factor is almost independent on temperature (r_H = 1.05 for current sensor operating temperature dropping in the range 20°C < T < 120°C [9]), hence current sensing circuits based on MagFET are suitable to be embedded in power transistors and smart-power system-on-chips that usually experience large temperature variations.

In this work, the conversion factor F_c that relates the normal magnetic field strength with the current *Ix* has been evaluated performing electromagnetic simulations for a metal strip of thickness t=4μm and width w=10μm [7]. Computer simulations have been repeated for several metal-strip-to-MagFET distances in the range 0 - 130μm and the results are shown in Fig. 3. On the basis of these considerations and

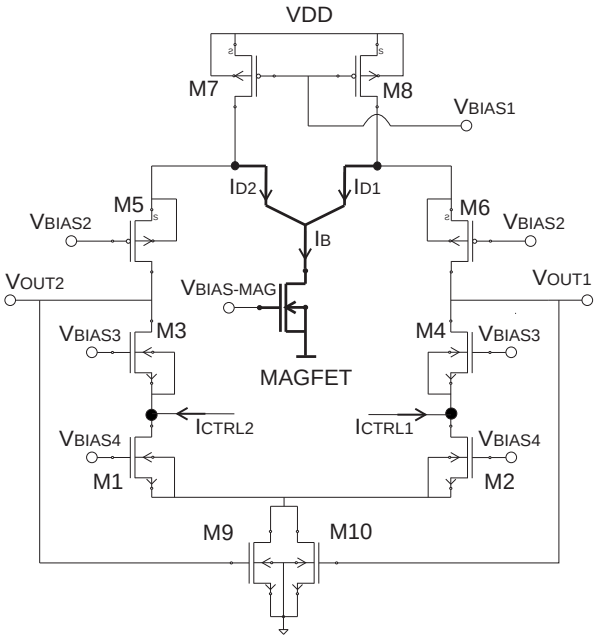

Fig. 4: Trans-resistance amplifier of the MagFET output currents.

referring to a square MagFET (W=L=10μm) and metal strip to MagFET distance Δ = 10μm, the conversion factor is equal to Fc=1.845mT/A and the overall conversion factor is about $\Delta I/Ix = 2.5 \cdot 10^{-9}$.

On the basis of the above mentioned parameters and assuming the current to be monitored ranging from 0A to 10A, the dynamic range of the MagFET differential output current takes values in the range 0-50nA. Being this current unbalance so small a trans-resistance high-gain amplifier (folded cascade topology) like that shown in Fig. 4 has been designed referring to an auxiliary circuit for offset cancellation like 0.35μm CMOS technology process. This gain stage shows a trans-resistance greater than 100dBΩ and it that sketched in Fig. 5. Offset compensation is performed whenever the power transistor is switched-off and no current flows through the power transistor. In this condition, the feedback loop, which is made of a voltage comparator, a 10-bit up/down counter, a DAC converter and a fully differential trans-conductance amplifier (OTA in Fig. 5), forces the sensor differential output voltage ($V_{OUT}=V_{OUT2}-V_{OUT1}$) to zero. In particular, with the *err_signal* set high, the comparator output voltage V_{O_comp} could be high or low depending on the offset sign. In the first case (i.e. V_{O_comp} high) the binary counter is enabled to count up and the compensation process start taking place, while in the second case (i.e. V_{O_comp} low) the logic control signal (*err_signal*) is set to zero and the comparator input voltage is inverted. Also in this last case the binary counter is made counting up.

The code generated by the binary counter is provided to a C-2C DAC that translated it to a voltage hence to the current imbalance I_{CTRL1}-I_{CTRL2}. This upset in the gain stage bias current compensates the trans-resistance output offset voltage. This compensation proceeds step-by-step as long as the comparator output voltage (V_{O_comp}) switches from high to low, then the binary count starts proceeding backward. Once the comparator output voltage toggles stably to the clock frequency, the compensation process is stopped and the resulting binary code, which is proportional to the amplifier input offset current, is then stored in a binary register. This code is constantly used during the current sensing for offset compensation purposes.

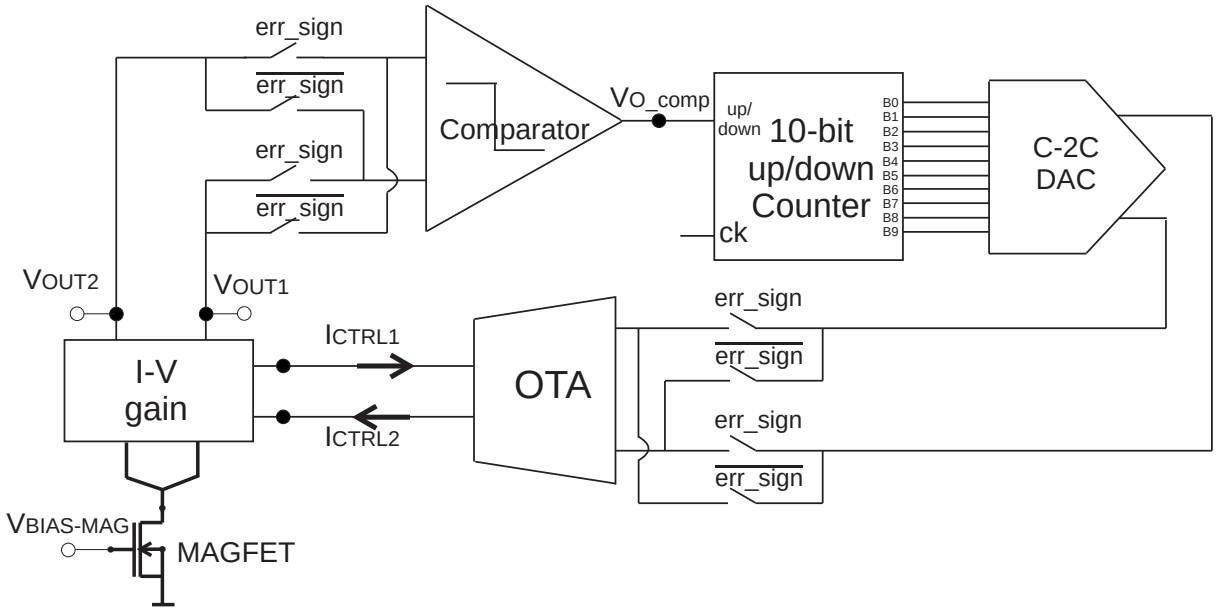

Fig. 5: Block diagram of the auxiliary circuit for compensating the trans-resistance amplifier output offset voltage.

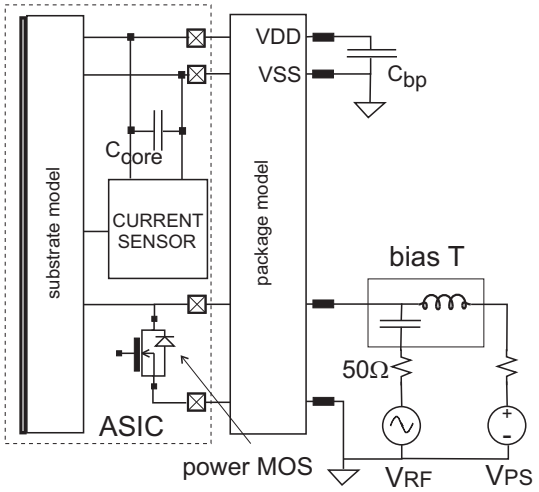

Fig. 6: Schematic view of the circuit including the current sensor, which has been considered for computer simulations. RFI is superimposed to the drain voltage using the DPI method.

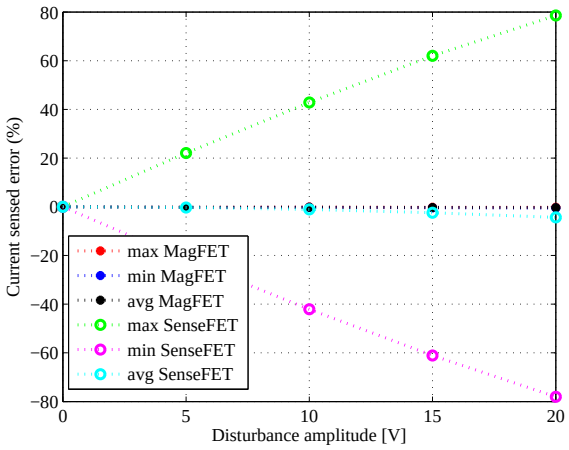

Fig. 7: Maximum, minimum and average value of the current-sensed error by MagFET and SenseFET versus RFI amplitude. CW interference at 20MHz.

4 SUSCEPTIBILITY TO RFI OF INTEGRATED CURRENT SENSORS

In this section the susceptibility to RFI of the above described current sensors added to the nominal signals of a power transistor is investigated. In particular, the case of a power transistor integrated in the same silicon die with a bunch of analog and digital blocks including a current sensor is considered, and it is assumed that all signal circuits share the same power supply rails. Analyses have been carried out referring to the schematic view of Fig. 6 that includes a 2 mm^2 power transistor, the substrate parasitic model, the package parasitic model and the schematic view of the current sensor under analysis. Furthermore, all circuits of the SoC except the power transistor and the current

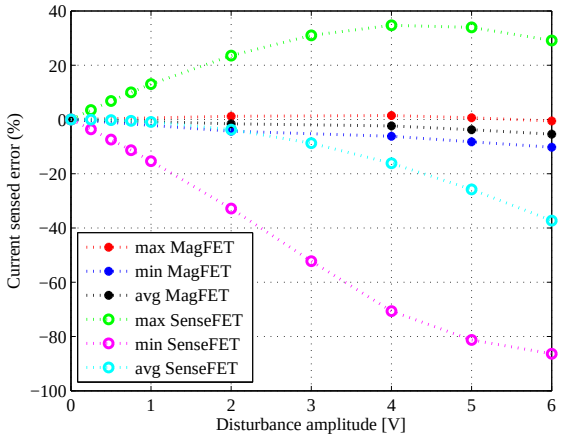

Fig. 8: Maximum, minimum and average value of the current-sensed error by MagFET and SenseFET versus RFI amplitude. CW interference at 100MHz.

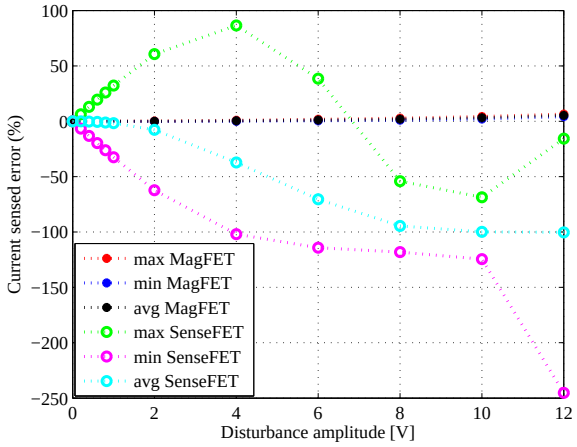

Fig. 9: Maximum, minimum and average value of the current-sensed error by MagFET and SenseFET versus RFI amplitude. CW interference at 200MHz.

sensor have been roughly modeled by an on-chip capacitance connected to the power supply and ground rails. Simulations have been carried out with the power transistor switched-on and the RFI added to the drain terminal using the direct power injection method [12]. In this framework, time domain simulations were performed using ELDO (a SPICE-like simulator) and the RFI-induced upset of the current sensor output signal (I_{sense} in the SenseFET circuit and the output voltage V_{OUT} of the MagFET trans-resistance amplifier) has been recorded. These simulation results are shown in Figs. 7, 8, 9 where the minimum, maximum and average value of the output signal RFI-induced upset versus RFI amplitude is reported. In particular, Figs. 7, 8, 9 have been obtained considering CW interference at 20MHz, 100MHz, 200MHz respectively. With reference to these results it can be concluded that the immunity of the MagFET-based current sensor (wireless sensor) is significantly

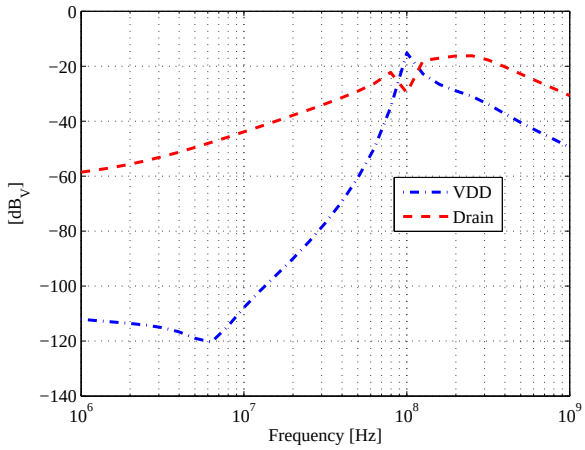

Fig. 10: AC analysis: RFI magnitude resulting at the switched-on power MOS drain terminal and at the current sensor power supply (VDD) referred to VSS.

greater than that of the SenseFET (wired sensor). However, it should be also noticed that both current sensors are more susceptibility to RFI in the frequency range around 100MHz. To this purpose, further analyses based on small-signal computer simulations have shown that RFI added to the power transistor drives the parallel resonance of the power supply package parasitic inductances (VDD-VSS) and the on-chip parasitic capacitance C_{CORE} (see Fig. 6).
Around this resonance (about 100MHz in the circuit under analysis) the amplitude of RFI that results added to the current sensor power-supply voltage takes magnitude comparable with that at the power transistor drain terminal, as it is highlighted by the plots in Fig. 10.

5 CONCLUSION

In this work, the susceptibility to RFI of integrated sensors for power transistor current monitoring has been discussed. To this purpose, a conventional current sensor, which is electrically connected by metal strips to the power transistor terminals, has been considered. Furthermore, a new wireless current sensor, which is based on the Hall effect in split-drain MOS transistor has been proposed and the susceptibility of these circuits have been investigated through time domain computer simulations. On the basis of these analyses it has been shown that the new MagFET-based solution (wireless sensing) is more immune to RFI than the wired counterpart.

6 ACKNOWLEDGEMENT

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