EMI-inducted failures in MOS power transistors

EMI-Inducted Failures in MOS Power Transistors

C. Bona[1] F. Fiori[2]

Abstract – **The present paper discusses the susceptibility of MOS power transistors to electromagnetic interference affecting the drain terminal. To this purpose, the Low Side configuration is considered and susceptibility analyses are carried out referring to simple small-signal models of the MOS transistor. The prediction of the susceptibility levels obtained in this way are validated through time domain simulations and experimental tests.**

1 INTRODUCTION

Power transistors are commonly employed as active switches in the power supply section and in the front-end circuits (electric motors and solenoids) of electronic equipments. Such components are preferred to their electro-mechanical counterpart for many reasons and in particular because they can be driven to switch faster aiming to improve power efficiency and reliability. However, fast switching circuits give rise to high frequency disturbances so that, most of the efforts of EMC engineers and researchers operating in this field have been aimed over the last decades to reduce the electromagnetic emissions originating from switching power circuits. Meanwhile, the wide diffusion of wireless systems in almost any field of human life has strongly increased the level of electromagnetic pollution, which could impair the operation of electronic systems. Such a topic is usually referred to as electromagnetic susceptibility (EMS) and it is of special interest for safety electronic equipments like those employed in automotive, avionic and industrial applications.

In the last decades several authors have investigated the susceptibility to Electro Magnetic Interference (EMI) of both analog and digital front-end receivers [1-2], while the effects of such disturbances on output buffers have not been covered yet. To this purpose, let's consider the simple circuit in Fig. 1, which includes a MOS power transistor, feeding an inductive load through cables. In such cases wiring harnesses behave like receiving antennas collecting interference (RFI) that corrupt nominal signals.

In this contest, the paper focuses on the susceptibility of MOS power transistors to radio frequency interference added to the drain-source terminals. In particular, Section 2 summaries the main criteria adopted in the design of MOS drivers while Section 3 shows how the susceptibility of

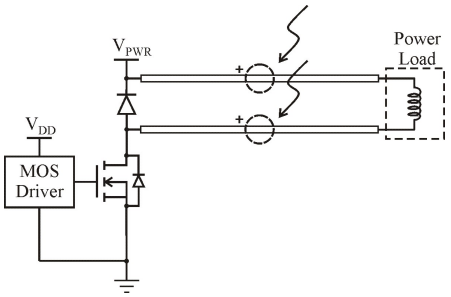

Figure 1: Low side topology with power transistor and inductive load connected through cables.

LS gate driven MOS can be investigated through small signal analysis. Finally, computer simulation and measurement results are shown in Section 4 and concluding remarks are drawn in Section 5.

2 MOS TRANSISTOR DRIVING

As mentioned in the introduction, power transistors are commonly used as active switches to supply energy to passive loads like solenoids, resistors and motors through cables. Switching power transistors are usually selected looking at the maximum operating voltage, the power dissipation (both static and dynamic) and the switching speed. Actually, the switching speed, namely the rise (t_r) and the fall time (t_f), affects in opposite way the power efficiency and the electromagnetic emission, implying to be among the designers' concerns. To this purpose, the rise and the fall time are usually kept below 5% of the switching period (T_s), which depends on the time constant of the transistor driving circuit. Actually, the transistor gate capacitance is not constant and it is a non linear function of the gate-source voltage, so that when performing the design of such circuits, it is quite common to refer to an effective gate capacitance ($C_{G\text{-}eff}$) [3]. Such a capacitance is charged up through the global gate resistance (R_{gate}), which includes the output driver resistance (R_d) and the intrinsic MOS polysilicon gate resistance (R_{poly}). Based on that, the rise time is usually expressed as

$$\tau_r = 1.6 R_{gate} C_{G-eff} = 1.6(R_d + R_{poly}) C_{G-eff} \quad (1)$$

and the driver resistance, which is needed to get the switching frequency f_s can be expressed as

[1] Istituto Superiore Mario Boella, EMC Competence Center, Via P. C. Boggio, 10129 Torino, Italy
e-mail: bona@ismb.it, tel.: +39 011 2276713
[2] Dipartimento di Elettronica, Politecnico di Torino, C.so Duca degli Abruzzi 24, 10129 Torino, Italy,
e-mail: franco.fiori@polito.it, tel.: +39 011 5644141.

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$$R_d \le \frac{\Delta t}{1.6 f_s C_{G-eff}} - R_{poly} \qquad (2)$$

where $\Delta t = \tau_r/T_s$ is the normalized rise time.

A similar reasoning can be also performed for the fall time, leading again to the above mentioned relationship.

Furthermore, EMI of significant strength can also arise from the resonance between the gate capacitance ($C_{G\text{-}eff}$) and the parasitic inductance (L_{par}), which results from the gate driver wiring interconnects (PCB traces, IC package lead-frame and bonding wires).

Being the self-resonance frequency of such a circuit

$$f_0 = \frac{1}{2\pi\sqrt{L_{par} C_{G-eff}}} \qquad (3)$$

and its quality factor

$$Q = \frac{2\pi f_0 L_{par}}{R_{gate}} = \frac{2\pi f_0 L_{par}}{R_d + R_{poly}} \qquad (4)$$

the output driver resistance R_d, which dumps the resonance ($Q \le 1/2$) can be expressed as

$$R_d \ge 2\sqrt{\frac{L_{par}}{C_{G-eff}}} - R_{poly} \qquad (5)$$

On the basis of these considerations, common design constraints can be expressed as follows

$$2\sqrt{\frac{L_{par}}{C_{G-eff}}} \le R_d + R_{poly} \le \frac{\Delta t}{1.6 f_s C_{G-eff}} \qquad (6)$$

Some numbers can help understanding the values of R_d we could have to deal with. To this purpose, let's consider a MOS transistor of drawing area equal to 2mm^2 having $C_{G\text{-}eff} = 3nF$ and $R_{poly} = 25\Omega$, with package parasitic self inductances of about $L_{par} = 16nH$.

Assuming the switching frequency $f_s = 200kHz$ and the normalized rise/fall time $\Delta t = 0.05$, the driver output resistance should drop in the range

$$0.9\Omega \le R_d + R_{poly} \le 52\Omega . \qquad (7)$$

However, such a design procedure does not take into account the effect of RFI on the operation of power transistors, and this issue is going to be addressed in the following of this paper.

3 SUSCEPTIBILITY OF SWITCHING MOS POWER TRANSISTOR TO EMI

The operation of switching power transistors can be affected by EMI because cables, that connect transistors to the power loads behave like unintentional antennas, so that transistor output port signals, i.e. the drain-to-source voltage and the drain current for MOS transistor, is affected by such a RFI. As a result, a transistor, which is driven at the gate-source port to be switched-off (on), can be switched-on (off) by RFI, resulting in unexpected dangerous failures. Such unwanted effects can be experienced when RFI added to the gate-source voltage takes amplitude such that the transistor can be alternatively switched-on and switched-off. In order to investigate the above mentioned effect a MOS transistor, which is connected in the low-side (LS) configuration with the drain-to-source nominal voltage affected by RFI has been considered. Analysis have been carried out with the transistor switched-off and switched-on, referring to the direct power injection method (see the schematic view in Fig.2), which requires adding RFI to nominal signals through bias tees [4]. In this work, such analysis has been limited to the static operation of the transistor whereas the switching transition has not been discussed.

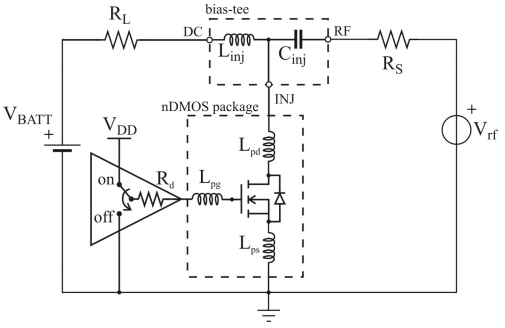

Figure 2: Schematic view of the Direct Power Injection test setup.

Although the problem of EMI-induced transistor switching involves non linear dynamic phenomena, several analysis and comments in the following of the paper are based on the results coming out from small signal analysis which in principle should be applied only to linear network. However, small-signal model parameters can be assumed to be constant with good approximation as far as the gate-source voltage does not cross the transistor threshold and the output state transition does not take place.

Based on that, the small-signal equivalent circuit of the power transistor switched-on (Fig. 3a) and switched-off (Fig. 3b) have been considered, and they have been employed in the small signal analysis of the circuit in Fig. 2, getting the transfer function V_{gs}/V_{rf}. To this purpose, the complete package model has been taken into account but here, for the sake of simplification, only the dominant components of such a model (bonding wire parasitic elements) are considered by means of the series inductances L_{px}.

Then, the gate driver is described by its Thevenin equivalent circuit while the drain DC bias network (biasing inductor and loading resistance (R_L)) has been modeled referring to the small signal equivalent

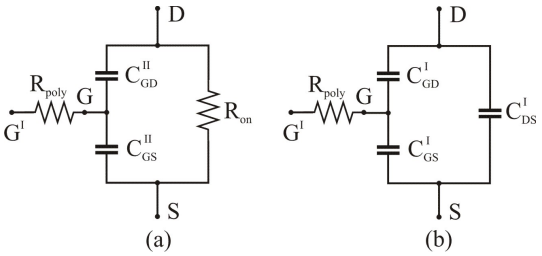

Figure 3: Power MOS small signal models in the *triode* region (a) and in the *off* state (b)

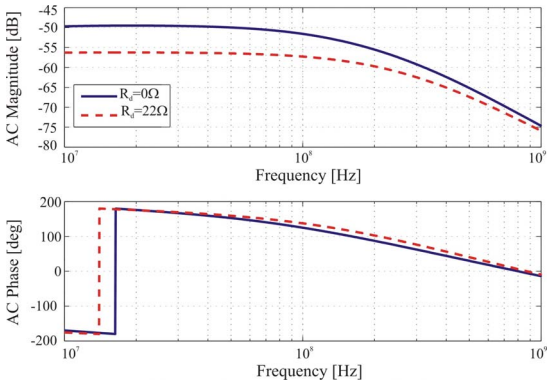

Figure 4: Transfer functions curves $V_{gs}(f)/V_{rf}(f)$ with the MOS biased in the *triode* region

circuit of each component over a wide frequency range. The results of the small-signal analyses reported so far have been obtained referring to the MOS power transistor introduced in Section 2.

3.1 LS power MOS driven in the triode region

Biasing the MOS power transistor in the deep-triode region the impedance at the drain terminal (INJ port in Fig. 2) is dominated by the drain-source resistance (R_{on}) so that a very little portion of the injected RFI propagates to the gate terminal.

This consideration has also been confirmed by the small signal analysis; the obtained V_{gs} transfer functions with respect to the injected signal V_{rf} referring to the considered example are plotted in Fig.4. From these results it turns out that, when the LS driver is biased in the *triode* region the maximum magnitude of the transfer function referring to a R_d of 0Ω is -49.5*dB* meaning that an injected disturbance of 1*V* involves a V_{gs} fluctuation of 3.3*mV*.

Overall, it can be concluded that a switched-on MOS power transistor can be difficultly switched-off by RFI.

3.2 LS power MOS driven in the off-state

Let's now consider the case of having the power transistor driven to be switched-off, and RFI is added

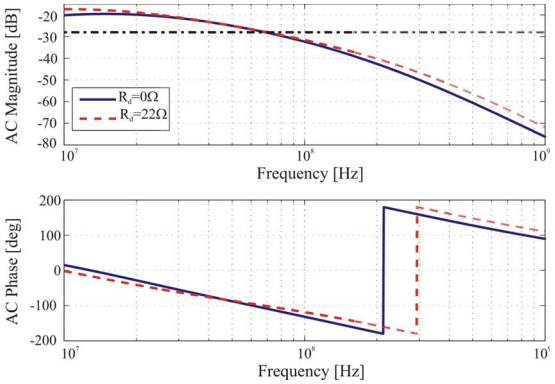

Figure 5: Transfer functions curves $V_{gs}(f)/V_{rf}(f)$ with the MOS transistor biased in the *off* state

to the drain terminal. In this case the gate-source voltage is affected by RFI because of the gate-drain parasitic capacitive coupling (C_{gd}) and in this case the attenuation of RFI from the drain to the gate terminal is lower than in the previous case with the transistor switched-on. Furthermore, being the MOS driver output resistor (R_d) a part of the drain-to-gate parasitic partitioning circuit, its value should affect the attenuation factor, leading to the definition of a design criteria.

Actually, as far as common power MOS transistors are concerned, the intrinsic gate resistance (R_{poly}) of common MOS power transistors takes value comparable with those usually chosen for R_d. Furthermore, the gate-source input loop is always affected by PCB and package parasitic elements so that RFI added to the transistor drain always reaches the gate-source port, even if the driver output resistance is set to zero.

These points has been confirmed by AC simulations, which have been carried out with several transistors of different size. Furthermore, it has been noticed that lower R_d resistance helps in getting higher immunity level only at low frequency (under a few tens MHz) whereas such effect becomes negligible at higher frequencies.

This result is also highlighted in Fig. 5 where the transfer function V_{gs}/V_{rf} for the circuit in Fig. 2 has been evaluated for the MOS transistor mentioned in Section 2 (R_{poly} = 25Ω) which is switched-off with R_d =0Ω (blue continuous line) and R_d =22Ω (red dashed line). In the same figure, the simulation results can be compared with the reference level of -28dB, that comes out for an input RFI with amplitude of 20V and transistor conduction threshold of 0.8 V.

In this case, the transistor is susceptible to RFI for frequency lower than 70MHz regardless the output driver resistance.

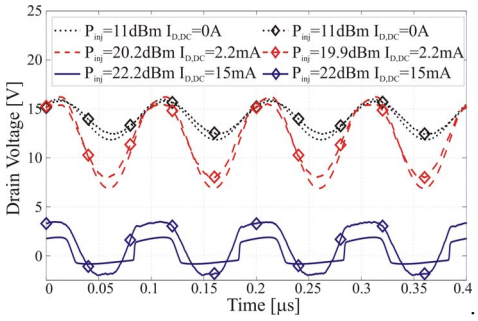

Figure 6: Drain voltage waveforms obtained by simulations and measurements (diamond markers) with R_d=22Ω at f=10MHz

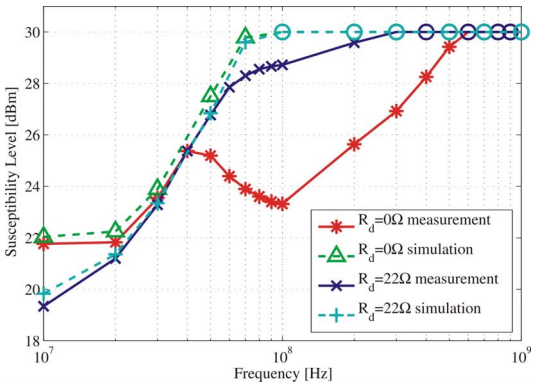

Figure 7: Susceptibility Level (I_D = 1mA). The "o" markers point out that no failure occurred.

4 MEASUREMENT AND SIMULATION RESULTS

The susceptibility of a DMOS power transistor to RFI superimposed to the drain source port has been evaluated referring to the schematic view of Fig. 2. Investigations have been carried out through time domain computer simulations and experimental tests, with the purpose of validating the analysis presented so far. In particular, Fig. 6 shows the waveforms of the drain voltage for RFI at 10MHz, which has been obtained through time domain simulations and measurements with the transistor driven to be switched-off. Here, it is pointed out that RFI with incident power greater than 11dBm drives the transistor to be gradually switched-on (look at the mean-value of voltages in Fig. 6). Furthermore, it is worth mentioning that in this case measurements and simulations are here in good agreement.

Similar measurements have been repeated to obtain the susceptibility profile of the DMOS transistor. Tests have been carried out in this way: once defined the frequency of the interfering signal, its amplitude has been increased step by step until a DC drain current of 1mA has been made flowing (susceptibility criterion). This procedure has been repeated for a set of interference frequency in the rage 10MHz-1GHz obtaining the results reported in Fig. 7. Furthermore, a maximum level of 30dBm for the incident power has been considered.

The curves in Fig.7 show that time domain simulations confirm the prediction of Section 3.2: from these results the power DMOS would be susceptible to the injected signal in the frequency band up to 70MHz regardless the output impedance driver. On the other hand, the measurements results in the frequencies above 40MHz do not confirm neither the prediction of small signal analysis nor those of time domain simulations. In particular, a much greater susceptibility to RFI is experienced and the susceptibility level depends on the output resistance of the gate driver (R_d).

Similar tests have been performed with the DMOS biased in the *deep triode* region but no failure has been never observed, confirming the conclusions reported in Section 3.1.

5 CONCLUSIONS

In this paper the susceptibility to RFI of power MOS transistors, connected in the low side configuration, has been investigated. Susceptibility analysis has been conducted referring to simplified small-signal models of the MOS transistor which have been validated through time-domain simulations and experimental test results. In particular it has been highlighted that a MOS transistor, which is biased in the deep triode region can be difficultly switched-off by RFI added to the drain-source terminals while a transistor driven to be switched-off can be switched-on by RFI.

Finally, it has been observed that neither the predictions of small signal analysis nor those of time domain simulations agrees with measurement results for frequencies above 40MHz, with the transistor driven to be switched-off.

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