Macromodels of IC Buffers Allowing for Large Power Supply Fluctuations

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Abstract: This paper addresses the generation of enhanced behavioral models for digital IC buffers. The proposed models can reproduce the behavior of real devices also for large fluctuations of the power supply voltage. The models can be easily estimated from port transient responses and can be effectively implemented in any commercial tool as SPICE subcircuits or VHDL-AMS descriptions.

1 Introduction

Nowadays, the models of I/O buffers of digital Integrated Circuits (ICs) are a key resource for the simulation of the signal integrity and electromagnetic compatibility effects of digital circuits.

Buffer macromodels are usually based on simplified equivalent circuits and the Input Output Buffer Information Specification (IBIS) [1]. Models based on IBIS data established as a standard widely used, are supported by manufacturers and accepted by most Electronic Design Automation (EDA) tools. Recently, other approaches to IC buffer macromodels, that supplement the IBIS resource and provide improved accuracy, have been proposed [2, 3, 6]. These approaches are based on system identification methods and parametric relations. They exploit a mathematical description of current and voltage evolution at the buffer port, possibly reproducing complicated dynamic nonlinear behaviors of the modeled devices. Of course, macromodels obtained by these parametric approaches remain almost as efficient as macromodels based on IBIS data and can be easily included in EDA tools as SPICE subcircuits or VHDL-AMS descriptions.

This paper is aimed at extending the modeling domain of both types of buffer macromodels. Present macromodels, either parametric or based on simplified equivalents, can allow only for limited variations of the power supply voltage, on the order of $10 \div 15\%$ of the nominal power supply voltage. For usual simulation problems, this limitation does not affect the accuracy of predictions. In fact, most application exploit single dye ICs and Printed Circuit Boards (PCBs) with decoupling caps and power planes that ensure small variations of the supply voltage. On the other hand, recent applications, like the stacked System in Package (SiP) devices, suffer from larger variation of the supply voltage and demand for buffer macromodels allowing for such large variations.

An example of the effects of supply voltage variations on macromodel accuracy is given in Fig. 1. The waveforms of this Figure are the responses of the buffer output and supply pin voltages for a device sending a pseudo-random bit sequence on a PCB interconnect. The solid line curves are the reference responses obtained by using a detailed device-level model of the buffer, whereas the dashed ones are the responses predicted by a state-of-the-art model of the buffer [2]. The current absorption and the impedance of the power supply network of this example are such that the

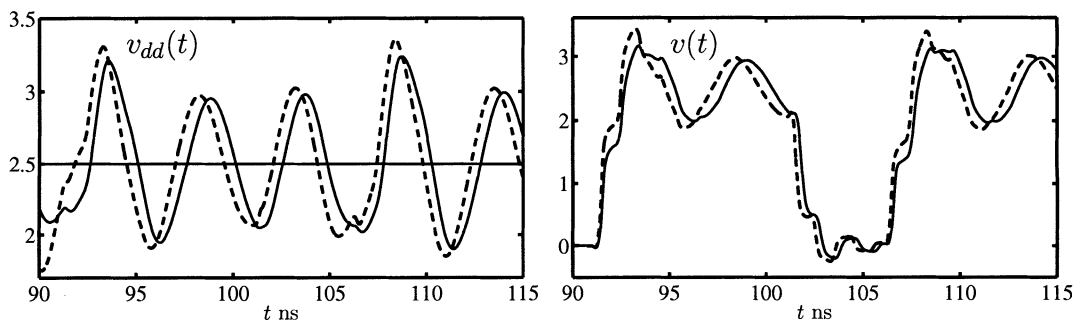

Figure 1: Output and supply port voltage waveforms ($v(t)$ and $v_{dd}(t)$, respectively) for the port of a digital IC energized by a real power supply network and driving a PCB interconnect (see text). Solid lines: reference; dashed lines: macromodel [2].

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supply voltage fluctuations are on the order of 40% of nominal power supply voltage. The response predicted by the model is affected by significant distortion and a timing error as large as the 10% of the bit time, thereby proving that so large variations of the supply voltage are outside the validity domain of the model.

Recently, preliminary studies on the extension of the current models based on IBIS to account for the large fluctuation of the supply voltage have been reported by ST microelectronics and Intel. A proposal based on these studies, that is named "Gate Modulation Effect", is currently in the evaluation process for its possible inclusion in the next version of the IBIS specification. More details can be found in the Buffer Issue Resolution Documents (BIRDs) [4, 5]. Here we elaborate on these results to achieve the required modeling domain extension.

2 IC buffer models

This Section briefly reviews the structure of macromodels for IC output buffers. For the sake of simplicity, the discussion is based on the output buffer of a single-ended device, whose structure is shown in Fig. 2. State-of-the-art macromodels for this structure are based on the following two-piece relation [1, 2]

$$i(t) = w_H(t) i_H(v(t), v_{dd}(t), d/dt) + w_L(t) i_L(v(t), v_{dd}(t), d/dt) \quad (1)$$

where i_H and i_L are submodels accounting for the device behavior in the logic high and low state, respectively, and the time-varying functions $w_H(t)$ and $w_L(t)$ provide the transition between the two submodels, i.e., the switching between the two logic states. A similar equation holds for the power supply current i_{dd}. Submodels i_H and i_L can be obtained from either simplified equivalent circuit representations (e.g., see IBIS [1]) or identification methods and parametric relations [2].

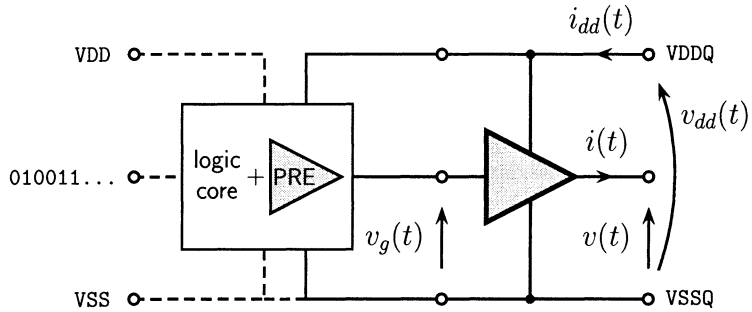

Figure 2: Structure of the output buffer of a digital integrated circuit with its relevant electrical variables. The bold triangle symbol indicates the last inverter stage and v_g its input voltage.

Present models (like the one used in the example of Fig. 1) are based on the simplifying assumption that the variations of the supply voltage are small. With this assumption, the weighting functions $w_H(t)$ and $w_L(t)$ are independent of the v_{dd} variable and the static characteristics of submodels i_H and i_L are those holding for the nominal value of v_{dd}.

3 Extended IC buffer models

This Section extends the basic model structure (1) to account for the large variations of the power supply voltage v_{dd}. For conciseness, the analysis focuses on models based on parametric relations only, as discussed in [2], where the submodels i_H and i_L are splitted into the sum of a static and a dynamic contribution (see the Appendix of [3]). The argument developed here, however, can be applied to any macromodel based on equation (1). The splitted structure for the submodel i_H writes

$$i_H(t) = i_{sH}(v_{dd}(t), v(t)) + i_{dH}(v(t)), v_{dd}(t), d/dt) \quad (2)$$

where i_{sH} is the static surface of the output current of the buffer at high output state and i_{dH} is a parametric model accounting for the nonlinear dynamic behavior of the output current. A similar equation holds for $i_L(t)$.

The extension of macromodels is illustrated for an example device that is a 8-bit bus transceiver with four independent buffers (model name SN74ALVCH16973, power supply voltage $V_{DDQ} = 2.5\,V$). The reference responses of this device are obtained by its HSPICE device-level model and are used for both the estimation of the parameters of our macromodel and for the assessment of its performance.

The static output characteristics of the example buffer are plotted in Fig. 3 for both logic states and for different v_{dd} values. In this Figure, v_{dd} is varied within the range [-30%,+30%] of V_{DDQ}. Present models use $i_{sH} = \hat{i}_{sH}(v_{dd} - v)$ and $i_{sL} = \hat{i}_{sH}(v)$, where $\hat{i}_{sH}$ and $\hat{i}_{sL}$ are the static characteristics of the output port current at high and low logic state for the nominal power supply voltage V_{DDQ}. In other words, present models identify i_{sH} and i_{sL} with the solid thick curves of Fig. 3, that is a rough approximation when the supply voltage variation is large. The proposal of [5] suggests to approximate the complete output port current surface by means of the following formula

$$\begin{cases} i_{sH}(v, v_{dd}) = \alpha(v_{dd}) \cdot \hat{i}_{sH}(v_{dd} - v) \\ i_{sL}(v, v_{dd}) = \beta(v_{dd}) \cdot \hat{i}_{sL}(v) \end{cases} \quad (3)$$

where coefficients α and β account for the variation of the supply voltage v_{dd} and are computed by matching the approximation to the actual surface for $v = 0$ and $v = V_{DDQ}$ (see the vertical gray lines of Fig. 3).

It is worth noting that, as any approximation defined along a line, this approximation is exact at $v = 0$ and $v = V_{DDQ}$ only. In actual operation, however, the domain of the output characteristic explored by i and v variables does not concentrate on $v = 0$ and $v = V_{DDQ}$, because i and v keep close to the buffer load lines. This property is demonstrated in Fig. 4, where some typical $i(t)$ and $v(t)$ trajectories are drawn on the static curves of Fig. 3. The plotted trajectories are obtained from the responses of the example device driving a transmission line with characteristic impedance $Z_0 = 50\,\Omega$. The trajectories develop along the load lines of the transmission line (gray straight lines of Fig. 4) and $v(t)$ is hardly close to the supply rails shown in Fig. 3. In order to account for this effect, we use (3) with α and β coefficients computed by matching the approximation and the real surface on the load lines of Fig. 4.

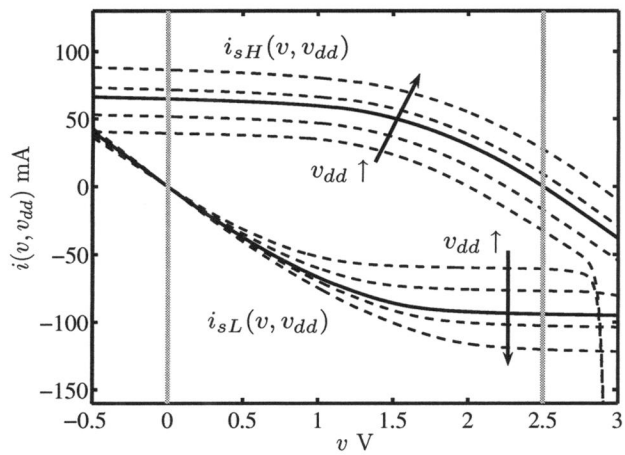

Figure 3: Solid-thick lines: DC output current of the example driver at fixed high and low output state and $v_{dd} = V_{DDQ}$; dashed-thin lines: DC output current for different values of the power supply voltage v_{dd}; vertical gray lines: power supply rails.

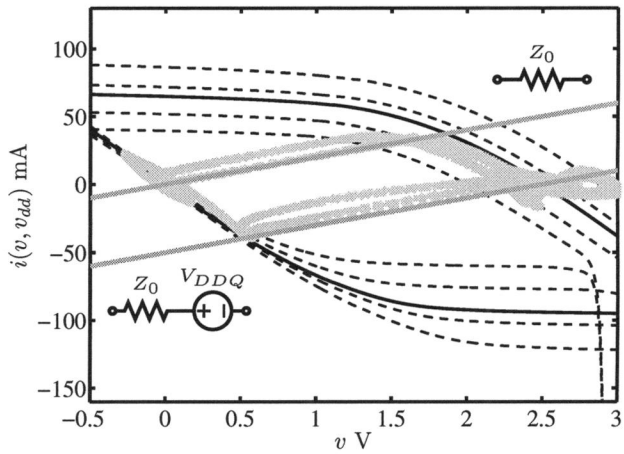

Figure 4: Solid-thick and dashed-thin lines: DC curves of Fig. 3; gray-line curves: samples of $i(t)$ and $v(t)$ waveforms for a 50 Ω transmission line load; straight gray lines: load lines of the transmission line.

The inclusion of supply voltage effects in the static characteristics of (1), however, is not sufficient to obtain a model for large supply voltage variations. Most of the error visible in Fig. 1, in fact, comes from timing effects due to the supply voltage variations. In order to allow for timing variations, the dependence of the weighting functions $w_H(t)$ and $w_L(t)$ on v_{dd} must be taken into account. In our model we identify the weighting function by combining functions obtained for different values of v_{dd} (*e.g.,* 70%, 100% and 130% of V_{DDQ}). More details on the computation of the weighting functions for constant supply voltages can be found in [2].

4 Numerical results

In this Section, the accuracy of different models based on equation (1) is assessed by comparing their responses to the reference response obtained by the device-level model of the example buffer. In particular, the following models are considered: the state-of-the art model of [2] used for the example of Fig. 1 (model #1 in the following), and the models defined by (3) with α and β coefficients computed either by matching on power supply rails (model #2) or by matching on the load lines of Fig. 4 (model #3). For both model #2 and model #3, the weighting functions w_H and w_L of (1) are parameterized on v_{dd} as outlined in the previous Section. All the models have been implemented in SPICE.

The transient responses predicted by the models for a circuit composed of the example buffer sending the `'010'` sequence on an open-ended ideal transmission line ($Z_0 = 50\,\Omega$, $T_d = 1ns$) are shown in Fig. 5. In this test the supply voltage of the buffer is kept constant at $v_{dd} = 0.7V_{DDQ}$ in order to highlight the ability of the models to yield accurate results also for supply voltages far from the nominal value. From this comparison, it is clear that the models #2 and #3 provide better results and that model #3 proposed in this paper offer a remarkable high accuracy level in extreme operating conditions as well.

A second test is defined by the same setup used for the example of Fig. 1. This setup is obtained by connecting the example buffer to a real power delivery network and by using the buffer to drive a transmission line with a 50-bit long pseudo-random binary sequence. The transmission line data are $Z_0 = 50\,\Omega$ and $T_d = 0.5$ ns, and the power delivery network is modeled by a lumped RL series connection ($R = 0.2\,\Omega$, $L = 10nH$). The large value of the inductor L

is chosen to cause the large fluctuations of the supply voltage v_{dd} shown in Fig. 1. The responses of model #1 and model #3 are shown in Fig. 6 and confirm the accuracy of the proposed model for simulations involving large supply voltage fluctuations.

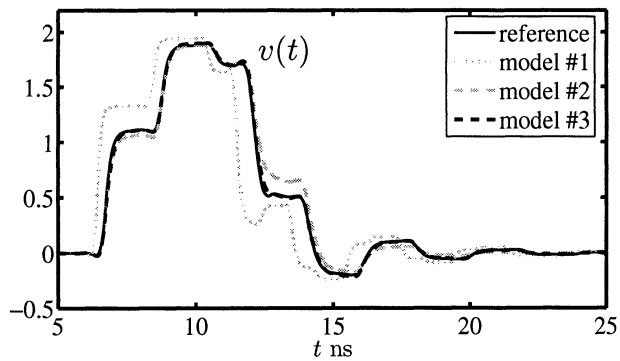

Figure 5: Output port voltage response $v(t)$ of the example buffer that applies the `'010'` bit stream to an ideal transmission line load while its supply pin is connected to a $70\%V_{DDQ}$ battery (see text for details).

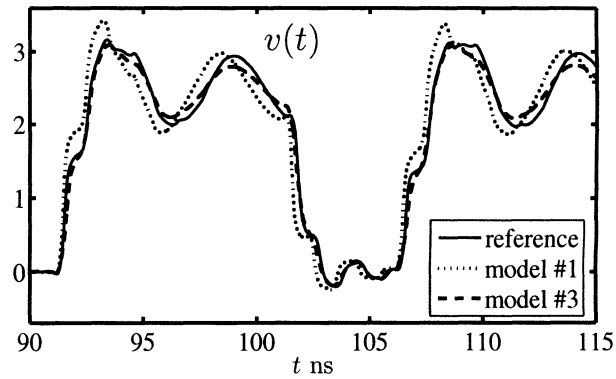

Figure 6: Part of the output port voltage response $v(t)$ of the example buffer loaded by a distibuted interconnect structure. The IC produces a peseudo-random bit stream and its supply pin is connected to a realistic power distribution network (see text for details).

5 Conclusions

This paper addresses the generation of a macromodel of digital IC buffers that overcomes the limitations of the existing models in accurately reproducing the device behavior for large variations of the power supply voltage. The proposed model is applied to a commercial device and its performance is assessed by simulating stiff test cases. The results confirm that the model can be effectively exploited for the assessment of signal integrity effects in a SiP design.

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