A Mixed-Signal Demodulator for a Low-Complexity IR-UWB Receiver: Methodology, Simulation and Design

A Mixed-Signal Demodulator for a Low-Complexity IR-UWB Receiver: Methodology, Simulation and Design

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Abstract

This works presents an integrated 0.18μm CMOS 2-PPM demodulator based on a switched capacitor network for an Energy Detection Impulse-Radio UWB receiver. The circuit has been designed using a top-down methodology that allows to discover the impact of low-level non-idealities on system-level performance. Through the use of a mixed signal simulation environment, performance figures have been obtained which helped evaluate the influence at system-level of the non-idealities of the most critical block. Results show that the circuit allows the replacement of the ADC typically employed in Energy Detection receivers and provides about infinite equivalent quantization resolution. The demodulator achieves 190 pJ/bit at 1.8V.

Key words: UWB Communications, Mixed-Signal Integrated Circuits, Design Methodology, Energy Detection, 2-PPM Modulation.

1 Introduction

The Impulse-Radio Ultrawideband (IR-UWB) technology is a promising solution for short-range indoor applications. It is particularly suited for applications aimed at connecting portable devices in Wireless Private Area Networks (WPAN) and for low-power sensor networks with low computational demands, reduced complexity transceivers and centralized control for multiple accesses. Generally, transceivers are designed to have high bandwidth, low peak powers

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at transmitters, low complexity and the flexibility of supporting different data rates. The "carrier-less" transmission relies on short duration pulses which satisfy FCC spectral requirements about both ultra-wide bandwidth occupations and low power spectral densities [1]. Thanks to these features, IR-UWB is particularly suited to low-power applications in which extended battery lives are a fundamental requirement [2].

For this kind of applications, low-complexity architectures must be employed in UWB receivers. Typically two approaches are used: The coherent and the non-coherent ones. The first perform demodulation by correlating the incoming UWB pulses with an internally generated waveform template. The second do not make any attempt to calculate the correlation of the incoming pulse, and perform demodulation without any a-priori information regarding the channel. The non-coherent receivers permit lower power consumption and lower complexities than in coherent receivers with a slight penalty in the Bit-Error-Rate (BER). This drawback is overcome in short-range applications in which the possibility of saving energy at the receiver side dominates the performance loss and the power budget at the transmitter. For low data rates coherent receivers generally have an energy per bit 10 times higher than for non-coherent receivers [3]. Among the various non-coherent alternatives, the Energy Detection (ED) approach is particularly interesting. Notwithstanding the 3 dB loss in the BER with respect to coherent receivers, the UWB modulated information is simply recovered by evaluating the received pulses energy. Due to the nature of ED schemes, receivers are insensitive to phase dependent modulations, thus data is transmitted according to time-based modulation schemes. Their low-power consumption is appealing in battery-powered short-range applications, in which full CMOS integration plays a crucial role for the overall device cost.

In typical implementations of Energy Detection receivers, energy is calculated after signal rectification by using Integrate-and-Dump (I & D) units. Such units, realized as open loop $Gm-C$ integrators for achieving large bandwidths [4], are typically followed by an Analog-to-Digital converter (ADC) and by a digital back-end that permits demodulation. Performance is affected by the ADC resolution and the features of the Integrator unit; in addition to this, the ADC represents one of the most power-hungry and silicon area-consuming blocks [5]. Since IR-UWB communication systems operate by means of time-domain modulations, it is possible to use ad-hoc solutions by reorganizing the general architectures thus eliminating the ADC and allowing low-power consumption. In the case of 2-PPM modulations, it is possible to replace the Analog-to-Digital conversion stage with simpler blocks which allow to compare the pulses energies in the analog domain [6], [7], therefore avoiding any quantization effect. With the aim of a low-power receiver and using a single comparator as in [6], this work presents an integrated differential 2-PPM CMOS demodulator formed by an open-loop $\mathrm{G_m - C}$ structure, called *Bi-*

phase integrator. It inherently provides Analog-to-Digital conversion without the use of any ADC, features offset rejection and exhibits nearly the same error-rate performance of an ideal Energy Detection receiver. The demodulator is composed of an Operational Transconductance Amplifier (OTA) and a differential switched capacitor network. The demodulator consumes $950\,\mu$W and achieves 190 pJ/bit at 5 Mbit/s.

The design and the simulation of the entire unit have been carried out with a design methodology based on different abstraction levels, the development of a proper VHDL-AMS simulation environment and the use of a mixed-signal simulation tool, ADVanceMS (ADMS, Mentor Graphics). Description levels with different degrees of accuracy allow to discover the impact of the abstraction refinement, thus help the designer trade between precision and simulation time [8]. For the low-level descriptions, the circuit building blocks have been designed in a mixed-mode UMC CMOS $0.18\,\mu m$ technology and simulated with SPICE BSIM3 transistor models. The design methodology combined to the simulation tool allowed to discover design weaknesses thus accurately predicting performance in presence of blocks non-idealities.

The paper is organized in the following parts: Section 2 introduces the principle of operation of the reduced complexity ED receiver which employs the Bi-phase demodulator, and highlights its differences with respect to the ordinary Energy Detection receivers. Section 3 introduces the successive refinement step design methodology. Section 4 introduces the Bi-phase demodulator unit and its main building blocks - the integrator and the comparator - explains the typical design issues and clarifies the trade-off between performance and low-power consumption. In addition, the section justifies the abstraction level required for simulating each of the two units. Section 5 reports both functional and system-level performance simulations. Finally, conclusions are drawn in section 6.

2 Low-complexity energy detection receiver

IR-UWB transmission is based on the use of short duration baseband pulses, on the order of one nanosecond, without the need of any carrier to provide bandwidth shifts. The Power-Spectral-Density (PSD) is very low with respect to narrowband and wideband modulations but the total transmitted power can be considerably high because of the very high bandwidth. The baseband pulses are phase-modulated, like in Bi-Phase Shift Keying (BPSK), or time-modulated, like in Pulse Position Modulation (PPM).

Typical Impulse Radio ED receivers front-ends include a Low-Noise-Amplifier (LNA), a Squaring Unit ($()^2$), an analog integrator and finally an A/D con-

verter, as figure 1 shows. Sophisticated operations other than simple demod-

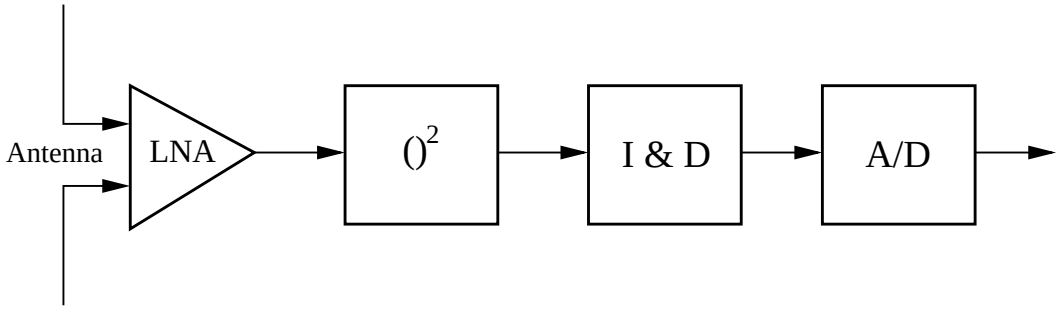

Fig. 1. Typical Energy Detection receiver

ulation, like for instance the synchronization, are typically done in the digital domain by elaborating the ADC output's raw data.

A typical modulation scheme is the 2-PPM (Bi-phase Pulse-Position-Modulation) in which the transmitted pulse is modulated according to its relative position within a time frame, as shown in figure 2. Whether a '0' is sent, the pulse is

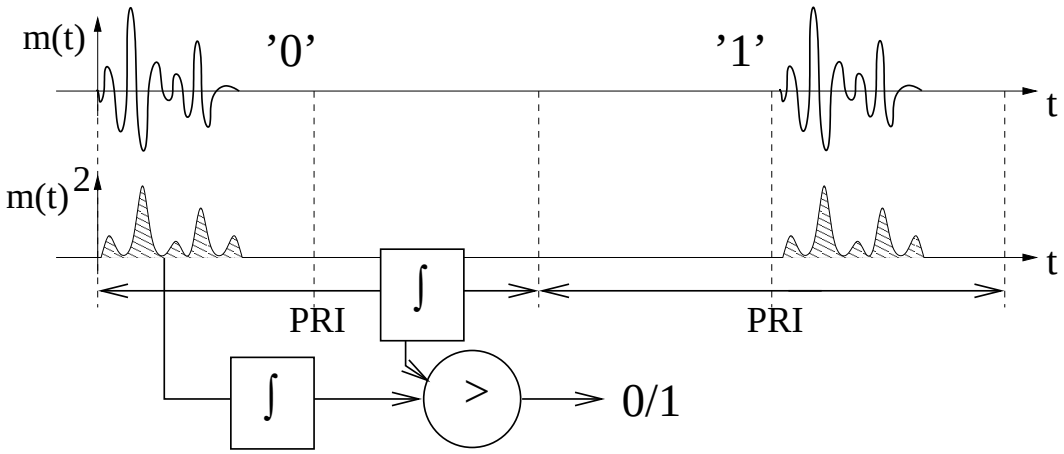

Fig. 2. 2-PPM modulation.

placed in the first half of a Pulse-Repetition-Interval (PRI), while in case of a '1', the pulse is placed in the second one. At the receiver, the UWB signal, rectified by the squarer, is integrated and dumped in the two PRI's halves by the I&D unit. The two obtained analog values represent the signal energies associated to the two PPM phases. After A/D conversion, data is demodulated by comparing the energies of the two PPM phases numerically.

With the intent of reducing complexity and power consumption, in this work we replace the ADC with a simple zero-threshold comparator by giving the analog integrator the capability to provide a voltage whose sign determines the information bit. We call this new receiver as *Bi-Phase Demodulator* and the reason of this name will be clear momentarily. The circuit is based upon the charge redistribution principle.

The Bi-phase demodulator shown in figure 3 is composed of two parts, the **Bi-phase integrator** and the **comparator**. The Bi-phase integrator recalls the

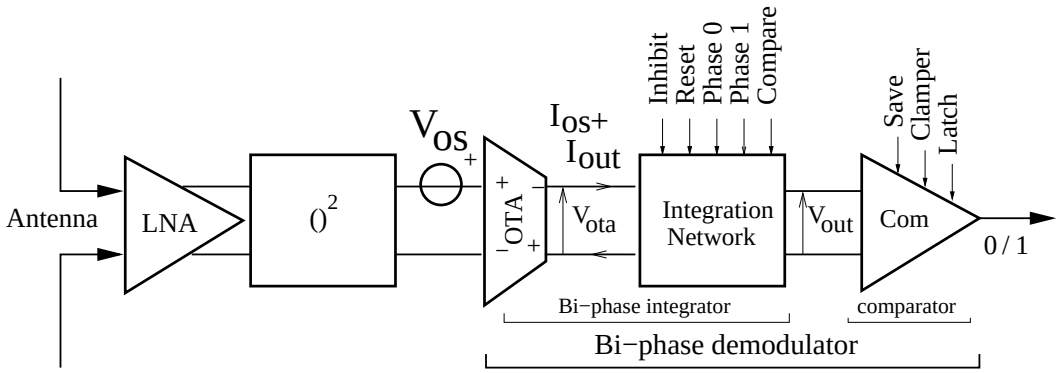

Fig. 3. Energy Detection receiver with Bi-phase demodulator

typical G_m-C integrator structures: It is composed of an open loop transconductor loaded with a capacitor contained in the integration network. After this first conditioning part which generates a modulation-dependent analog voltage, the result is processed by the zero-threshold comparator which converts the demodulation voltage into a binary digital quantity.

Differently from other works in which full receiver front-ends are presented, here the contribution is more focused on the design of a single unit of the demodulation chain and on how its non-idealities impact on system-level performance. With respect to [7], in which baseband processing relies on a single-ended inverter, here the demodulator is composed of a fully-differential Operational Transconductance Amplifier inclusive of common mode stabilization network. The circuit described in detail in section 4, is a mixed-signal device because the analog voltage processing in the integration network of figure 3 is controlled by switching transistors. Therefore, to obtain the impact at system level of a single block, a proper mixed-signal design methodology must be employed in the various design stages.

3 Design methodology

Hardware description languages like VHDL and Verilog are typically employed in digital design. With the introduction of VHDL-AMS, a superset of the VHDL language, it became possible to employ both continuous-time and digital descriptions in the same simulation, thus allowing true mixed-signal simulations in which analog and digital parts are simulated concurrently. The design and the simulation of the Bi-phase demodulator and of the receiver front-end need not only a proper language but also a design tool through which the description language can be "brought to life". An example is ADVanceMS (ADMS, Mentor graphics) which can simulate both VHDL-AMS and SPICE

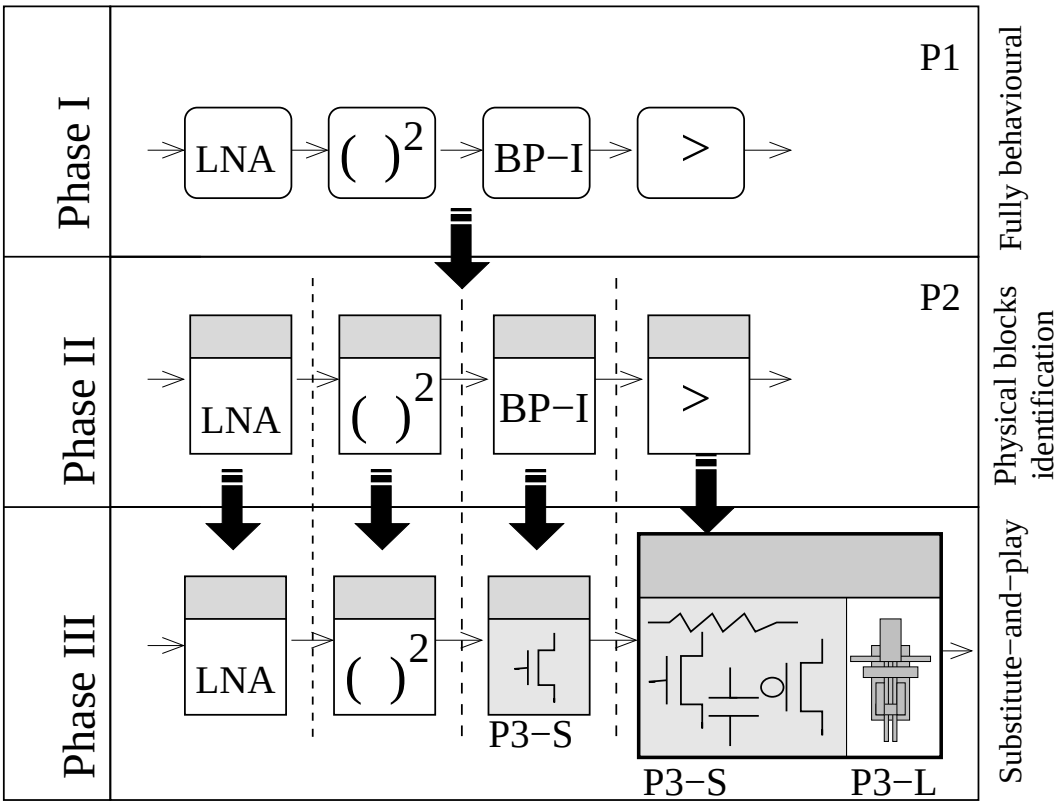

Fig. 4. Design flow phases using VHDL-AMS and ADMS.

descriptions. Interesting examples of the use of VHDL-AMS and the ADMS tool are [9], [10]. The language combined with the tool allows the designer to create an ad-hoc simulation environment in which the system functionalities can be tested. In addition, the possibility to use VHDL-AMS and SPICE description in the same environment allows to refine the blocks description from pure behavioral models down to circuit structural descriptions (e.g. transistor-level). In other words, top-down methodologies typical of the digital design can be also applied to the case of mixed-signal devices.

We adopted the design methodology outlined in [11] where we proposed a successive refinements-based approach. We took advantage of the inherent partitioning properties of the VHDL-AMS language, that is the possibility to assign each part of the design the description of its interface with the outer world, i.e. its `entity`, and the description of the reaction of its inner parts to the signals listed in the entity as well as to its internals states, i.e. its `architecture`. Our approach consists of three steps: *Phase I - Architectural description*, *Phase II - Partitioning* and *Phase III - Substitute-and-play*. In figure 4, the different block shapes in Phase II and III identify the entity/architecture partitioning. The block labeled as `BP-I` indicates the Bi-phase integrator.

During Phase I the general system architecture is conceived. This functional description does not necessarily assign each block of the architecture a specific

task but rather consider the system as a whole. In addition it is also possible to prove the coherence with other high-level languages such as Matlab [12].

During Phase II, the architecture is partitioned into single blocks, each with a proper VHDL-AMS entity and architecture. It is possible to partition the whole front-end in smaller units such as the LNA, the squarer and the Bi-phase demodulator. At this level electrical compatibility among the units must be provided. Each unit has its own terminals which identify inputs, outputs and power supply nets. The units are still behaviorally modeled but the description is detailed enough to let the designer consider the first macroscopic non-ideal parameters in the models, like saturation, slew-rates, input and output impedances et cetera. Since the testbenches are inherited from Phase I, it is possible to evaluate the effect of these non-idealities on the system performance. It is then now possible to investigate on the macroscopic front-end requirements for a single block (e.g. gain, linearity, bandwidth) and to derive constraints for the successive circuit-level design phases. In addition, it is possible to determine the most critical blocks through simulated performance figures or electrical-level considerations.

During Phase III, the description of one or more blocks is refined. For example, the Bi-Phase integrator, that was described in Phase II with VHDL-AMS equations, can be substituted with a transistor-level description. During this phase, the component instantiations are replaced without changing the upper level VHDL-AMS source code. This "painless" substitution, we call it *Substitute-and-Play*, is allowed by the partitioning done in Phase II since electrical terminals do not change once defined (the blocks interfaces, that it the "entities", are not modified). The substitution operation can be applied also to a subset of the blocks the designer considers relevant to understand its effect on the system. Typically, one or two blocks are replaced at at time. Whether the layout-extracted SPICE netlist is available, or the effect of parasitics is relevant for the system-level performance evaluation, the designer can import such low-level description of a block in the simulation environment. Whether the results obtained in Phase III do not differ from those obtained during Phase II, it is possible to simulate the system by using the simpler higher-level model (and this will save simulation time) and to focus on the refinement of the front-end units which have not been considered yet.

In the remainder of the paper we will use the following notation: `P1` - Conceptual Phase I, `P2` - Behavioral model - Phase II, `P3-S` - SPICE level - Phase III, `P3-L` - Layout level - Phase III.

4 Integrated demodulator

4.1 Bi-phase integrator

This subsection introduces the Bi-phase integrator unit. It is organized in two parts: The first one deals with the principle of operation whereas the second one focuses on the transistor-level design of the device.

Principle of operation

Figure 5 details the Bi-Phase integration network of figure 3. The integrator

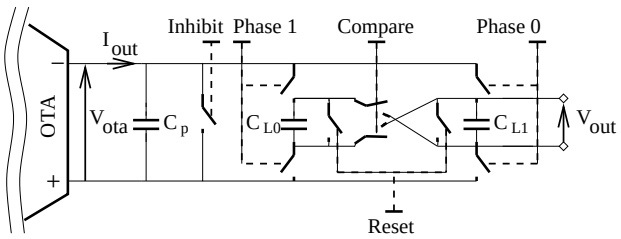

Fig. 5. Principle of the Bi-phase integrator

includes the transconductor, which consists of an Operational Transconductance Amplifier (OTA) [13], and a switched capacitor network [14]. The former transforms the input voltage variations V_{in} into current I_{out}, while the latter controls current injection in two identical integration capacitors C_{L0} and C_{L1} associated with the two PPM phases. The overall parasitic capacitance due to the integration network and the OTA output stage can be divided in two parts: the differential and the common mode capacitance. For this preliminary analysis we will consider only the differential capacitor modeled as C_p since the common mode parts have no effect. The Bi-phase integrator operates with five control signals, *Phase 0*, *Phase 1*, *Compare*, *Reset* and *Inhibit*. The first three control the integration of the incoming UWB pulses, the fourth one resets the state of the integrating capacitors and finally the fifth one shorts the differential output of the transconductance amplifier. As explained later, the whole demodulation process is based on the charge redistribution principle.

When the device is idle, signal *Inhibit* forces the differential output terminals of the transconductor to the same potential, then shorting parasitic capacitor C_p before starting the integration of the first PPM phase. When the first integration starts, *Inhibit* is deactivated and signal *Phase 0* is asserted forcing current I_{out} in the equivalent capacitance $C_{L0} + C_p$. When the first integration phase finishes, signal *Phase 0* is deactivated and *Inhibit* is asserted again. As a result, the charge in capacitor C_{L0}, now isolated from the rest of the circuit, remains (ideally) constant. When the second integration starts, signal *Inhibit*

is deactivated and *Phase 1* is asserted therefore forcing current in $C_{L1} + C_p$. In the end, the charge in C_{L0} and C_{L1} is proportional to the input signal: After the deactivation of *Phase 1* and the assertion of signal *Inhibit*, the final demodulation is possible by activating signal *Compare*. Charge redistribution principle is responsible for setting the sign of output voltage V_{out} according to the information bit. Whether the charge in C_{L0} is higher than the charge in C_{L1}, the voltage V_{out} will be positive, otherwise V_{out} will be negative. The comparator evaluates the information bit by comparing such voltage to zero. Finally, signal *Reset* zeroes the charge in C_{L0} and C_{L1} and another demodulation cycle is possible.

It is easy to understand that the device inherently provides offset rejection thanks to its fully balanced structure. In fact, if the sole offset voltage V_{OS} is present at the OTA input, the resulting offset current I_{OS} is fed alternatively in C_{L0} and C_{L1}: After the final charge redistribution the resulting output voltage is ideally zero.

The beneficial effect of the *Inhibit* switch can be better explained by analyzing in detail the operation of the device. On top of figure 6 the control phases signal activation and deactivation are schematized. When the receiver acquires modulated data, the demodulator operates in a "steady state" mode and integration control signals are asserted periodically. The figure shows different conditions (from A to F) according to the current operation phase and allows to follow voltage variations across C_p and integration capacitors C_{L0} and C_{L1}. With this scheme it is possible to focus our attention on the initial and final conditions across C_p, C_{L0} and C_{L1} and to understand how to combine them together to obtain the mathematical expression representing the influence of parasitics on V_{out}. Condition G represents the final charge redistribution after having completed the two demodulation phases.

We define T_i as the idle time between the deactivation of *Phase 0* and the activation of *Phase 1* and vice-versa.
In addition, we define the voltages $V_{i_{ph0}}^{p,(n)}$, $V_{f_{ph0}}^{p,(n)}$, $V_{i_{ph1}}^{p,(n)}$, $V_{f_{ph0}}^{p,(n)}$ across the capacitance C_p (superscript p), where n indicates the current demodulation period. The equations state how the initial and final conditions on voltage across C_p impact on C_{L0} and C_{L1} at the beginning and at the end of each demodulation phase. Subscripts i and f indicate the initial and final conditions across C_p during the idle period, for *Phase* 0 ($ph0$) and *Phase 1* ($ph1$) operation states, respectively.
To take into consideration the charge transfer it is also necessary to define the quantities $V_{i_{ph0}}^{(n)}$, $V_{f_{ph0}}^{(n)}$, $V_{i_{ph1}}^{(n)}$ and $V_{f_{ph1}}^{(n)}$ which represent the voltages across both C_{L0} and C_{L1} during the activation of the respective integration switches.
When signals *Phase 0* and *Phase 1* are asserted, the OTA integrates the UWB

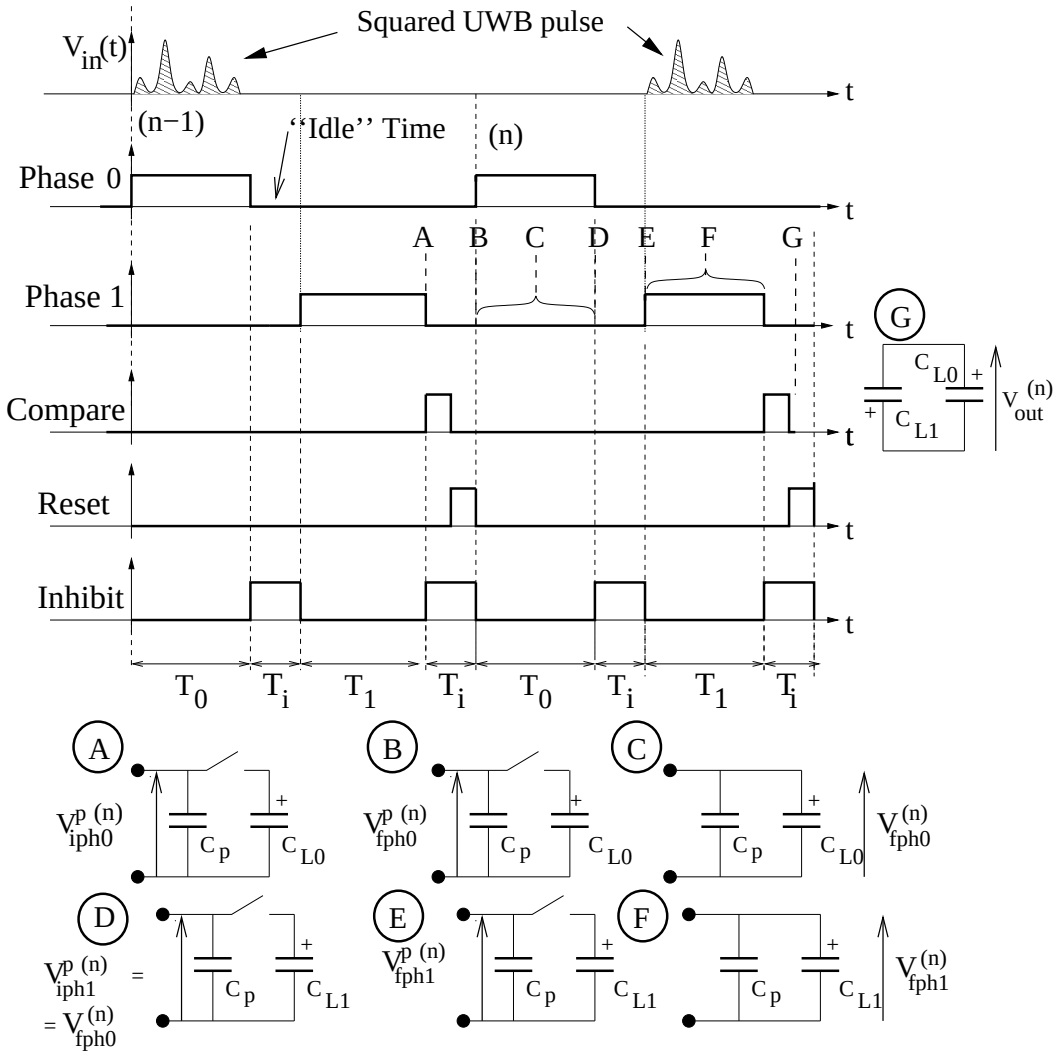

Fig. 6. Circuit operation scheme during demodulation

signal generating the information required for demodulation:

$$V_O^{(n)} = \frac{1}{C_p + C_{L0}} \int_{T_0^{(n)}} G_m V_{in}(t) \quad \text{and} \quad \mathrm{V_1^{(n)}} = \frac{1}{\mathrm{C_p + C_{L1}}} \int_{\mathrm{T_1^{(n)}}} \mathrm{G_m V_{in}(t)}$$

where T_0 and T_1 indicate the domains of integrations of equal duration for Phase 0 and Phase 1, respectively.

With these hypotheses it is possible to obtain equations 1-4 which model the operation of the device for the first of the two PPM integrations at time n in case the *Inhibit* signal is not used.

$$V_{f_{ph0}}^{p,(n)} = \frac{I_{OS}T_i}{C_p} + V_{i_{ph0}}^{p,(n)} + N_{f_{ph0}}^{p,(n)} \tag{1}$$

$$V_{i_{ph0}}^{(n)} = \frac{C_p}{C_p + C_{L0}} V_{f_{ph0}}^{p,(n)} \tag{2}$$

$$V_{f_{ph0}}^{(n)} = V_{i_{ph0}}^{(n)} + V_0^{(n)} \tag{3}$$

$$V_{i_{ph1}}^{p,(n)} = V_{f_{ph0}}^{(n)} \tag{4}$$

For the second PPM phase, it is possible to obtain a similar set of equations (not reported for sake of brevity). At activation of signal *Compare*, considering that the integration capacitors are equal ($C_{L0} = C_{L1} = C_L$), the final output voltage after the final charge redistribution is given by $V_{out}^{(n)} = \frac{1}{2}\{V_{f_{ph1}}^{(n)} - V_{f_{ph0}}^{(n)}\}$.

If we combine the two equations sets, we can express $V_{out}^{(n)}$ as a function of $V_{out}^{(n-1)}$ (equation 5).

$$\begin{aligned} V_{out}^{(n)} = \frac{1}{2}\{V_1^{(n)} - \frac{C_L}{C_p + C_L} V_0^{(n)} + \\ + \frac{C_p}{C_p + C_L}\{N_{f_{ph1}}^{p,(n)} - N_{f_{ph0}}^{p,(n)} - V_1^{(n-1)}\} + \\ + \frac{C_p^2}{(C_p + C_L)^2}\{V_{out}^{(n-1)} - N_{f_{ph1}}^{p,(n-1)} + N_{f_{ph0}}^{p,(n-1)}\}\} \end{aligned} \tag{5}$$

In the case in which no reset switches across C_p are employed, the differential output voltage for the $n-th$ integration $V_{out}^{(n)}$ depends on the stochastic processes $N_{f_{ph0}}^{p}$ and $N_{f_{ph1}}^{p}$ both for the n-th and the $(n-1)$-th demodulation phase. If C_p is zero, it is easy to demonstrate that demodulation voltage is ideal, that is

$$V_{out,ideal}^{(n)} = \frac{1}{2}\{V_1^{(n)} - V_0^{(n)}\}.$$

To obtain a similar effect in presence of parasitics, it is sufficient to reset the charge accumulated in C_p before a new phase starts with signal *Inhibit*. In this case, $V_{i_{ph0}}^{p,(n)} = V_{f_{ph1}}^{p,(n)} = 0$: That is, using the reset switches across C_p, the obtained output voltage is ideal.

In both cases, the equations presented show how the symmetric structure of the circuit completely eliminates the effect of offset contribution V_{OS}. In fact, the final output voltage does not depend on current I_{OS}. In summary, the possibility of resetting charge in C_p before starting a new demodulation and the offset rejection capabilities allows to obtain almost ideal demodulation performance.

Design

Figure 7 presents the overall schematic of the Bi-phase integrator. It shows the

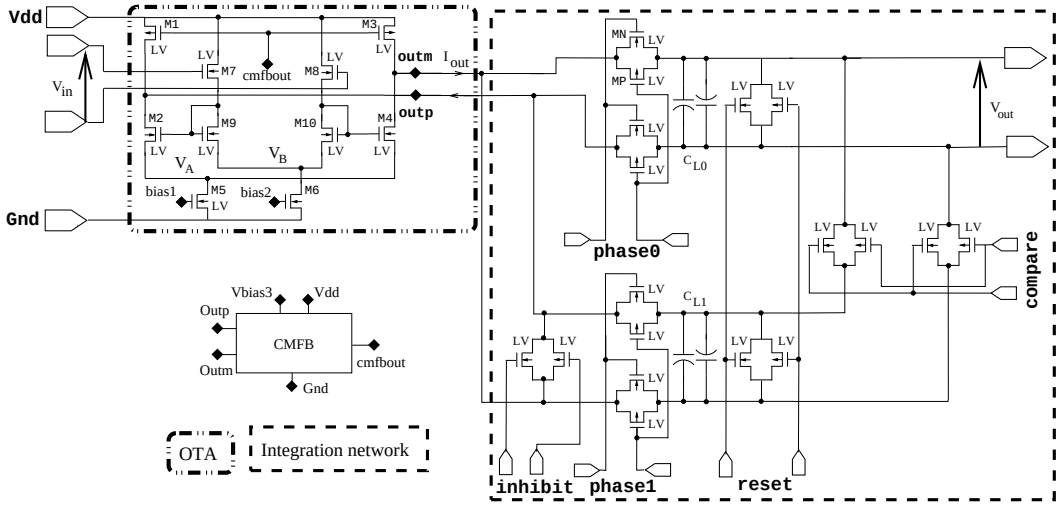

Fig. 7. Schematic of the Bi-phase integrator

internal Operational Transconductance Amplifier structure and the integration network. The circuit is fully differential and the OTA input stage consists of a source-follower differential configuration. Current variations at the input are mirrored in the output stage through a MOSFET configuration similar to a current mirror. The technology employed here is a mixed-mode CMOS 0.18 μm process. For enhancing the over-drive of some of the transistors, the Low-threshold Voltage (LV) process option has been employed.

The amplifier includes auto-biasing circuits and a simple Common Mode Feedback Network (CMFB) made up of a differential stage only. On the one hand, as clarified in [15], the use of a common mode stabilization network is mandatory for integrators employing open-loop transconductors: Thus a slight increase of the overall device power consumption is unavoidable. On the other hand, no precise control of output voltages is necessary in this case because demodulation is based on a relative voltage comparison. For the same reason, temperature drifts, aging and voltage supply variations are reflected in the two integrated voltages V_0 and V_1 in the same way: As a result, the OTA does not require any transconductance tuning [16].

The supply voltage is 1.8 V and the common mode input bias is 0.9 V. The dynamic input and output ranges were limited to 0 V-260 mV and $\pm$600 mV respectively in order to limit power consumption as much as possible [15]. The integrator has been simulated at different temperatures up to 90° C and for different corner conditions: The equivalent $G_m - C$ integrator gain, composed of the OTA and a load capacitor, decreases of approximately 5 dB in the worst conditions with respect to the nominal value (20 dB circa at 30° C, typical process) and greater self discharge in the load capacitors. Notwithstanding this,

demodulation performance is only marginally affected by this decrease: A gain fluctuation of circa 5 dB does not significantly corrupt the final demodulation voltage because the process relies on a relative comparison.

An important point is the OTA differential transconductance. The transistors aspect ratios are such that $M2 = M4$, $M3 = M1$, $M7 = M8$ and $M9 = M10$. If we analyze the small-signal equivalent model, neglecting drain-source resistances, it is possible to obtain a closed form of the equivalent OTA differential transconductance G_m,

$$G_m = \frac{g_{m2}}{2(1 + \frac{g_{m9}}{g_{m7}} + \frac{g_{mb7}}{g_{m7}})} \tag{6}$$

where g_{m2}, g_{m7}, g_{m9} are the equivalent transconductance of M2, M7 and M9, respectively. The quantity g_{mb7} is the body effect transconductance of M7. The gain can be improved by increasing M2 aspect ratio and by reducing M9's W/L with respect to M7. As shown in the formula, gain is only affected by the M7 body-effect transconductance. This is not surprising because the source terminals of the other transistors (i.e. M2, M4, M9 and M10) are not connected in a differential stage fashion. Although the input and output equivalent circuits cannot be formally considered as differential stages, voltages V_A and V_B shown in figure 7 do not vary with the differential input signal. This results in a "balanced" simplification of such effect on both left and right branches of the circuit. In this work G_m is 280 μS at 30 °C, with a resistive load of 10 KΩ at a frequency of 100 KHz.

By neglecting parasitic MOSFET capacitances and taking into account the drain-source resistances of the output stage, it is also possible to calculate the overall transfer function of the OTA, $\frac{I_{out}}{V_{in}}$, which depends on a generic load impedance Z_L,

$$\frac{I_{out}}{V_{in}} = -\frac{g_{m2}}{2(1 + \frac{g_{m9}}{g_{m7}} + \frac{g_{mb7}}{g_{m7}})(1 + \frac{Z_L}{r_{ds2}} + \frac{Z_L}{r_{ds1}})} \tag{7}$$

where r_{ds2} and r_{ds1} are the drain-source resistances of M2 and M1, respectively. The load impedance Z_L models the integration capacitances inclusive of parasitics. It is evident that if $Z_L = \frac{1}{s(C_L+C_p)}$, the output function $V_{out} = Z_L I_{out}$ presents a pole at low-frequency which, in the ideal case (that is $r_{ds1}, r_{ds2} \to \infty$) should be at $s = 0$. It is easy to note that the equivalent output impedance of the OTA, which depends on the above drain-source resistances, influences the cut-off frequency of the resulting first order pole.

Such pole at about 9 MHz in the transfer function limits the maximum integration time. Simulations show that integration windows longer than about 30 ns would cause unacceptable losses in the computed energies. The aspect ratios of MOSFET at the OTA output stage affect gain and bandwidth of

the transconductance amplifier: An increase of W/L has the effect of increasing the OTA gain and thus compensates for the various drops in the output switching network, but at the same time increases the frequency of the above mentioned pole. Moreover, the transistor sizing significantly influences other device characteristics: An increase of W/L mitigates distortions and increases gain but lead to a higher power consumption.

We have obtained the AC response of the OTA loaded by the integration capacitors by means of simulations. The results and the integration behavior is guaranteed up to several GHz. A second pole located at such high frequency does not affect the demodulation performance because the bandwidth of the useful signal at the squarer's output is within the integration frequency range.

Fortunately, non-coherent Energy Detection receivers do not require extremely precise pulse elaboration, thus allowing low W/L which help keep power at its lowest. Nonetheless, excessive distortion is certainly unacceptable. Table 1 reports the OTA Total-Harmonic-Distortion (THD) evaluated varying the signal amplitudes as suggested in [17]. The fundamental frequency is 100 MHz and up to the 40-th order harmonics have been considered in the analysis, ranging from 100 MHz to 4 GHz. Results show that for large input signal magnitudes the THD increases up to -20 dB. Although THD is worse than in [17], here extremely low THD values are not required because the OTA elaborates a signal which the squarer already predistorted "on purpose". Moreover, the demodulation consists, as discussed before, in a relative energy comparison that ends with a "hard" decision about the information bit: The pulse largest energy is in the first or in the second half of the PRI. The distortion of the squared signal produced by the OTA will not degrade appreciably the results (unless of course the signal level is such high that the OTA stages saturate). Simulation results validating this property are given in section 5.

Table 1
Transconductor THD for different differential inputs

V_{in} (mV_p)	50	100	150	200	250	300	350	400
THD (dB)	-26	-24.5	-23	-22.5	-22	-21.5	-20.5	-20

The demodulation performance is influenced by any asymmetry of the differential architecture and particularly of the output-to-ground parasitics in the two switching branches. The integration networks avoids this problem by intrinsically providing the symmetry required to keep these contributions balanced. Moreover, each of the two integration capacitors C_{L0} and C_{L1} are implemented as a pair of anti-parallel MIM capacitors. The integration capacitors are of about 200 fF each.
The integration switches, as shown in figure 7, consist of transmission gates that ensure very low dropouts during activation. Their aspect ratios (in this work on the order of 20) must be chosen to minimize the effects on integra-

tion gain: As W/L increases, drain-source resistance decreases but parasitics increase and may considerably reduce the integrator gain.

Table 2 shows a summary of the transistors aspect ratios for the proposed solution. To minimize short-channel effects, except for LV transistors, lengths have been kept higher than the minimum values. MP and MN aspect ratios refer to p-MOS and n-MOS of the transmission gates.

Table 2
Some of the aspect ratios of the MOSFET employed in the Bi-phase integrator.

MOSFET	M1	M2	M3	M4	M5	M6
$W/L\,(\mu\text{m}/\mu\text{m})$	$\frac{11.2}{0.24}$	$\frac{2.4}{0.24}$	$\frac{11.2}{0.24}$	$\frac{2.4}{0.24}$	$\frac{40}{10}$	$\frac{45}{5}$
MOSFET	M7	M8	M9	M10	MP	MN
$W/L\,(\mu\text{m}/\mu\text{m})$	$\frac{7.2}{0.24}$	$\frac{7.2}{0.24}$	$\frac{2.4}{0.24}$	$\frac{2.4}{0.24}$	$\frac{4.8}{0.24}$	$\frac{4.8}{0.24}$

One last remark is related to mismatch. Since switching transistors are susceptible to mismatch, and thus inject charge asymmetrically in the load capacitors, the output voltage can be affected by offsets.

4.2 Low-offset comparator

In order not to waste the robustness of the integrator against offset, the comparator which follows the Bi-Phase integrator must have excellent offset properties as well. Considering the wide literature about analog comparators and the importance of this unit for this work, we will start this subsection by revisiting some of the most important design issues from the Bi-phase demodulator point of view.

Preliminary analysis

Analog comparators are typically found in Analog-to-Digital converters in which low-power requirements, high sample rates and low-offsets represent their major design challenges. Several circuit topologies can be found in literature, but the majority of them are based on the use of two main building blocks, the preamplifier and the latch [18]. The preamplifier, a transconductor [19], elevates the input signal and amplifies it for a successive regeneration. The latch (a negative resistance or regenerative network) generates a full-swing digital signal through a positive feedback. Finally, some switches whose position and number depends on circuit topology, activate and deactivate the regenerative network and the preamplifier according to the device operation phases.

The two main non-ideality sources in analog comparator are input-referred offset and kickback noise. The former is due to mismatch properties of MOSFET transistor [20], and due to the non-perfect routing in the interconnection lines of the layout [21]. For this reason, in order not to neglect important geometrical effects, in our case it is necessary to include post-layout extracted netlists of the comparator in the simulation environment. The relevance of the offset problem has been shown in [22]: For a 0.6μm CMOS process, input-referred offset of a regenerative stage can vary from about -10 to 10 mV. Instead, the kickback noise is a phenomenon which depends on the capacitive coupling between the latch output and the preamplifier input [18]. This phenomenon is relevant for large equivalent output resistances of the preamplifier. The challenge in the present design is to keep offset contribution low rather than reducing kickback noise because the equivalent series resistance at the output of the Bi-phase integrator is reasonably small.

Depending on the type of preamplifier and latch employed in the design, different classes of comparators can be identified: the *Static* or Class-A, the *Class-AB* and the *Dynamic Latch* comparators [18]. The Class-A comparators are composed of a linear preamplifier and regenerative latch in cascaded configuration. Their power consumption is high because the preamplifier is always active during the whole comparison process. Typically, the regeneration process is slow due to the presence of two poles in the transfer function. Class AB latched comparators are faster because the preamplifier differential stage output is directly connected to the latch output formed by two cross-coupled inverters. These circuits typically have a single pole in their transfer function and the lowest power consumption with respect to the other two classes.

Various circuit level techniques are employed to eliminate offset. The Input-Offset-Storage (IOS) and Output-Offset-Storage (OOS) techniques are the most used [23], [24]. They consist of storing the offset voltage in a capacitor through the use of dedicated switches. The capacitors emulate a voltage source corresponding to the offset voltage at the input or at the output of the preamplifier. OOS technique is used to store the input-referred offset of the latch while the IOS one is used to store both the latch and the preamplifier offsets. Other offset reduction techniques consist of digital controlled circuitry which make use of Digital-to-Analog converters and programmable capacitive loads [25]. These approaches permit to compensate the regenerative network offset with an unbalanced capacitive trimming at the two latch output nodes.

In this work, the offset mitigation is achieved by employing three techniques: The use of the analog preamplifier, the use of a clamping switch in the regenerative network and the use of decoupling switches to insulate the differential input from the preamplifier. While the first technique is typically used in every low-offset comparator, the second technique, extrapolated from the considerations in [21], helps decrease the switching voltage of the latch by forcing the

regenerative inverters to saturation. The third technique, which works combined with the second one, let the circuit account for the input referred offset of the latch during the first operating phases. We did not employ any IOS and OOS technique not to increase much the circuit complexity and thus not to increase the number of control signals for circuit operation. Comparison time is not particularly relevant because the device operates slowly, thus we have not considered specific techniques like the use of inductive loads in the regenerative network [19]: The time between the comparison phase of the Bi-phase integrator and the successive demodulation phase is about 50 ns. Finally, since a single comparator is required in this design it is possible to relax the power consumption constraints and use an hybrid circuit topology which helps easily apply the offset reduction techniques.

Principle of operation

The adopted circuit topology is a hybrid between a class-A and a class-AB comparator (figure 8): The preamplifier, always active, and the latch are decoupled as in a class A comparator and the regenerative is composed of two cross-coupled inverters as in a class-AB one. The preamplifier stage is composed of a differential stage connected to the input terminals by two insulation switches M1, M2. The M3 switch forces the differential preamplifier input to zero which is insulated from the latch through two series switches, M14 and M15. The output voltage of the regenerative network is frozen by the switch M20. Switches M16 and M17 allow to activate and deactivate the latch according to the device operation phase. The comparator operation is organized in three steps: pre-comparison, pre-amplification and comparison. The pre-comparison phase mitigates the offset of the preamplifier and of the regenerative network, the pre-amplification phase amplifies the small input voltage for the latch and the comparison phase allows the full-swing signal regeneration. Aiming at reusing the same signals of the Bi-phase integrator properly combined together, the device uses three additional controls: `save`, `latch` and `clamper`. These can be generated from signals `inhibit`, and `compare` as $\texttt{save} = \overline{\texttt{inhibit}}$, $\texttt{latch} = \overline{\texttt{inhibit}} + \texttt{compare}$ and $\texttt{clamper} = \overline{\texttt{compare}}$.

During pre-comparison signal `save` is deactivated and the preamplifier is frozen by M3. Signal `clamper` is activated to force the comparator output at the switching voltage through M20 and signal `latch` is activated as well to turn on the latch and force inverters transistors M18, M19, M21 and M22 to saturation. During this phase the latch and the preamplifier are shorted by transistors M14 and M15. The `clamper` switch helps to lower the input-referred offset of the latch due to unbalanced routing interconnection and to mismatch. Ideally, the offset contribution is reduced if the initial voltage in

the latch approximates the switching voltage of the two inverters [1] [26]. Since M14 and M15 force the same voltage between the preamplifier and the latch output the transistors operating point is about the switching voltage, thus part of the offset contribution of both is lowered. During the pre-amplification phase signals `latch` and `save` are deactivated and the differential input signal across `Inp` and `Inn` is applied to the differential stage input. The preamplifier, whose response depends on the the time constant associated to the its pole, amplifies the signal. In the meantime, the output nodes are forced to the same voltage through signal `clamper` and the latch is turned off not to corrupt the preamplifier output voltage once enabled through M14 and M15. During the comparison phase signal `clamper` is deactivated and signal `latch` is asserted at the same time. The latch is thus activated and in the end, the full swing regenerated output is provided across terminals `out_rp` and `out_rm`.

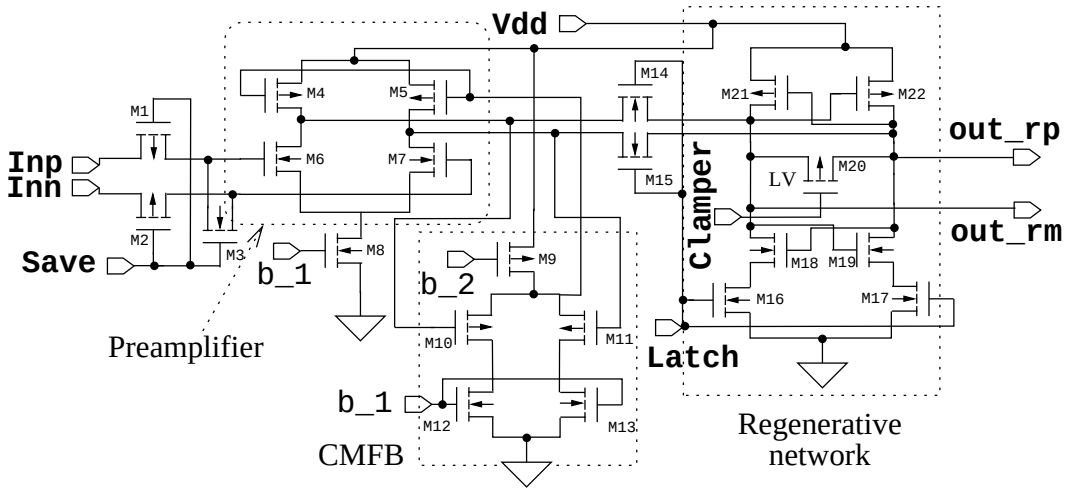

Fig. 8. Schematic of the low-offset comparator

Design

The clamper switch in the regenerative network consists of low threshold voltage (LV) transistors to ensure a very low equivalent resistance when activated. In this case we did not employ transmission gates in order not to increase the output nodes capacitance that would significantly reduce the circuit speed. The other switches employ transistors with standard threshold voltage. The preamplifier takes the bias voltages from the same biasing network of the Bi-phase integrator through terminals `b_1` and `b_2`. Its gain must be kept high enough to counter the effects of process corners and temperature variations. To guarantee sufficient amplification, it is necessary to track the differential input more than the time constant of the preamplifier pole. In our case, simulations

[1] This quantity is defined as the voltage across which the pMOS and the nMOS of the two inverters are perfectly saturated.

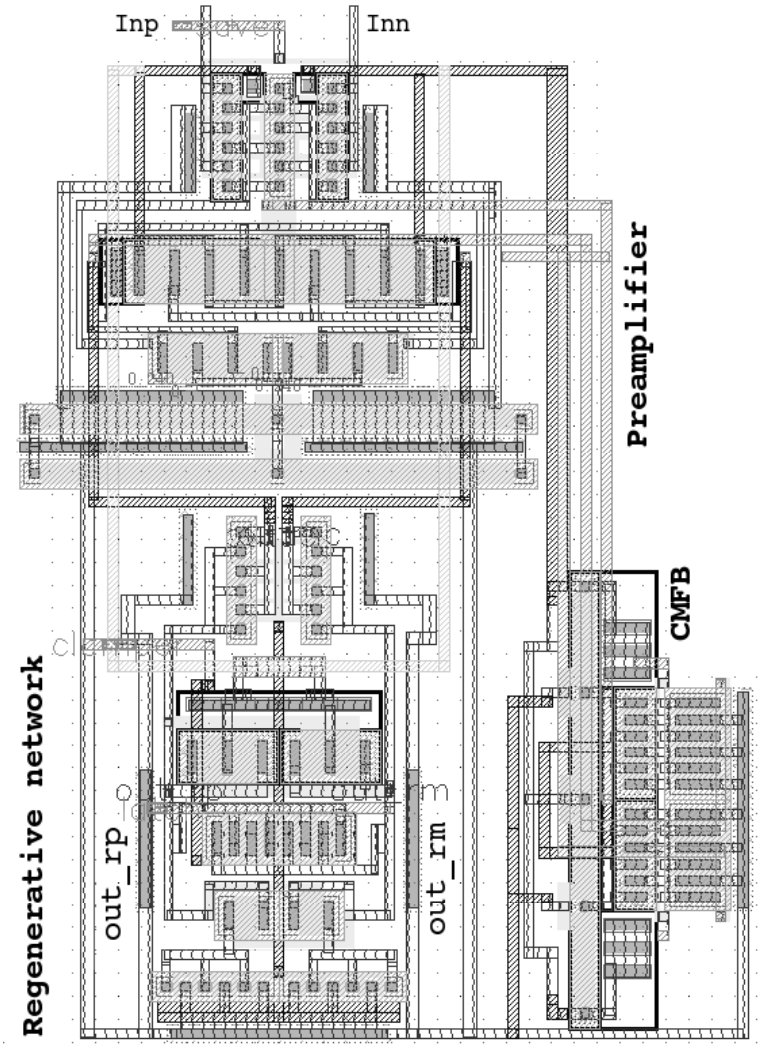

Fig. 9. Comparator layout

show that 10 ns are enough to ensure a gain of about 20. Since preamplifier gives the highest offset contribution, the dimensions of matched transistors M6 and M7 have been kept high. Typically, offset voltage is due to threshold voltage variations and position of transistors on the die. Since the first aspect is much more relevant, offset can be thus modeled with $\sigma_{V_{off}} \simeq A_{V_T}/\sqrt{WL}$, where A_{V_T} is on the order of 5 mV·μm for a typical 0.18 μm process [27]. This data is also in accordance with the matching characterization reports of our technology. In this design, aspect ratios of transistor M6 and M7 lead to an offset of $\sigma_{V_{off}} \simeq$2.5 mV. By estimating the other offset contributions we can derive a total value of about 3 mV.

Since the operating point of the preamplifier can vary with temperature and process corners, as for the Bi-phase integrator, we realized a very simple Common Mode Feed-Back (CMFB) circuit to keep the preamplifier operating point under control. As shown in figure 8, it consists of a differential stage which

Table 3
Aspect ratios of the MOSFET employed in the comparator.

MOSFET	M1	M2	M3	M4	M5
$W/L\,(\mu\text{m}/\mu\text{m})$	$\frac{1.8}{0.18}$	$\frac{1.8}{0.18}$	$\frac{1.8}{0.18}$	$\frac{8}{1}$	$\frac{8}{1}$
FN	5	5	5	4	4
MOSFET	M6	M7	M8	M9	M10/M11
$W/L\,(\mu\text{m}/\mu\text{m})$	$\frac{4}{1}$	$\frac{4}{1}$	$\frac{1}{10}$	$\frac{1}{4}$	$\frac{5}{0.18}$
FN	3	3	4	4	5
MOSFET	M12	M13	M14	M15	M16
$W/L\,(\mu\text{m}/\mu\text{m})$	$\frac{10}{0.18}$	$\frac{10}{0.18}$	$\frac{1.2}{0.24}$	$\frac{1.2}{0.24}$	$\frac{1.8}{0.18}$
FN	5	5	5	5	5
MOSFET	M17	M18	M19	M20	M21/M22
$W/L\,(\mu\text{m}/\mu\text{m})$	$\frac{1.8}{0.18}$	$\frac{1.3}{1}$	$\frac{1.3}{1}$	$\frac{1.5}{0.24}$	$\frac{3}{1}$
FN	5	1	1	7	3

acquires differential voltage from the preamplifier output and derives a control voltage from the transistor pairs sources. This analog voltage is used to bias the active loads of the preamplifier and to adjust the common mode. Transistors M12 and M13 are biased in linear region, in order not to make the network sensitive to mismatches. This solution is quite far from the typical common mode feedback circuits but represents a good compromise for transistor number and robustness.

As said before it is of utmost importance that the design non-idealities do not affect the comparator performance. We have thus detailed the design of this block down to the layout level and analyzed the parasitic effects on system level performance thanks to the *substitute-and-play* methodology previously discussed. Table 3 summarizes the transistors aspect ratios and, considering the layout realization, also the finger numbers (FN). Figure 9 shows the comparator layout. It is possible to identify the common-mode feedback unit on the right-bottom side, the preamplifier on the top and the regenerative latch in the bottom of the figure. Here, for sake of brevity, the biasing stage has not been shown as well as the power supply and the Bi-phase integrator metal interconnections. In this layout we particularly cured the MOSFET placement in order to maximize matching: The matching properties of a transistor pair depend mostly on their mutual position in the layout [28],[20]. Here, each MOSFET in the differential pass transistors has been placed next to each other in a parallel geometry [2]. All the transistors have been fingered because

[2] We define as "parallel pass transistors" two MOSFET's which connect a differ-

this technique allows to lower mismatch sources by a factor $\sqrt{n}$ where n is the finger number [20]. We have chosen an odd finger number in order to balance the parasitic interconnection resistance and capacitance of each source-drain pair. In the latch stage (which is most sensitive to mismatch and potentially the biggest source of offset), perfectly balanced power supply routing is also necessary. In particular, the supply vias have been placed in the center of the metal lines which connects the two anti-symmetric inverters in order to balance the parasitic resistance in each branch. In the layout, the `save` and the `latch` switches have been placed next to each other to minimize mismatch. Switching transistors efficiency also depends on the substrate resistance and on the number of substrate contacts placed in their surroundings. This implies that the substrate contacts must be placed as close to each switch as possible.

Imperfect metal routing can lead to input-referred offsets on the order of several hundreds of millivolts [21], hence we privileged the placement of the matched transistors in such a way that vertical symmetry is ensured. The symmetry inherently provides the same environment for the matched transistors at sources and drains, thus lowering mismatch. In the cases designs require multiple comparators, the layout of a single device is also important to minimize global die variations. For example in flash Analog-to-Digital Converters the comparator layout must be as much regular as possible, in such a way that the combination of multiple units leads to a common centroid [29]. Since here, only one comparator is required, this last aspect can be relaxed.

5 Simulations

The simulation environment includes some features which make simulation as much close to a realistic setting as possible. It includes Additive White Gaussian Noise (AWGN) and multipath diversity as an IEEE 802.15.4a waveform database of measured channel responses for an indoor multipath environment [2]: This allows extensive BER simulations with the possibility of varying the noise level. The bits are modulated with a Pulse Repetition Interval (PRI) of 200 ns and an integration time of 30 ns is used for both PPM phases. The most important entries of system's link budget are shown in table 4.

Functional simulations

Before entering into the discussion of system-level performance we present, through figure 10, the operation of the device employing the same notations of figure 4. The figure shows the complete operation of the circuit including both

ential input to a differential output, i.e. M14-M15 or M1-M2.

Table 4
Link budget

Parameter	**Value**
Geometric center frequency (f_c')	3.94 GHz
Average TX power (P_T)	-8.5 dBm
RX noise figure (NF)	7 dB
Minimum E_b/N_0 for $BER = 10^{-3}$ (S)	17 dB
Implementation loss (I)	1 dB
Link margin (@ $d_{max} = 26$ m)	1.22 dB
Minimum RX Sensitivity level	-87 dBm

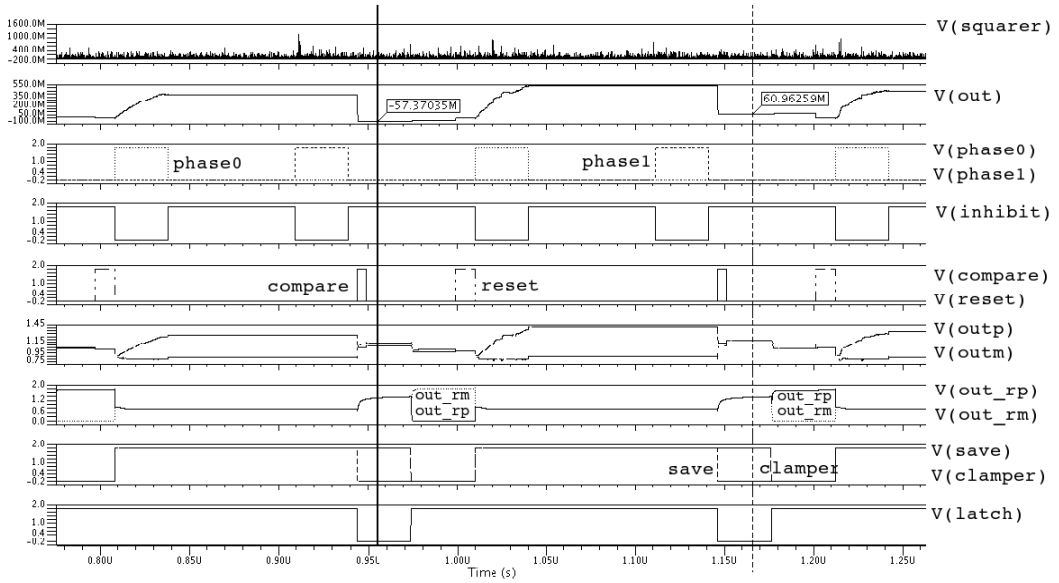

Fig. 10. Transient simulation of the Bi-phase demodulator

the integrator and the analog comparator. In these post-layout simulations we used the schematic view of the Bi-phase integrator and the comparator netlist extracted from the layout. All the signals are expressed with the notation `V()` to suggest that the plotted waveforms are voltages extracted from a terminal. For sake of simplicity all control signals, albeit differential, are presented as single ended.

The output of the ideal squarer is given by signal `V(squarer)`. This signal is composed of both UWB signals and AWGN noise with an equivalent bandwidth of 1.9 GHz. Signal `V(out)`, defined as `V(Inp)-V(Inn)` where `Inp` and `Inn` are the input terminals of the comparator, represents the Bi-phase integrator output. After resetting the charge in the capacitors with signal `reset`, the first integration is performed by asserting signal `phase0` and by deactivating signal `inhibit` which enables the OTA output to follow the input signal

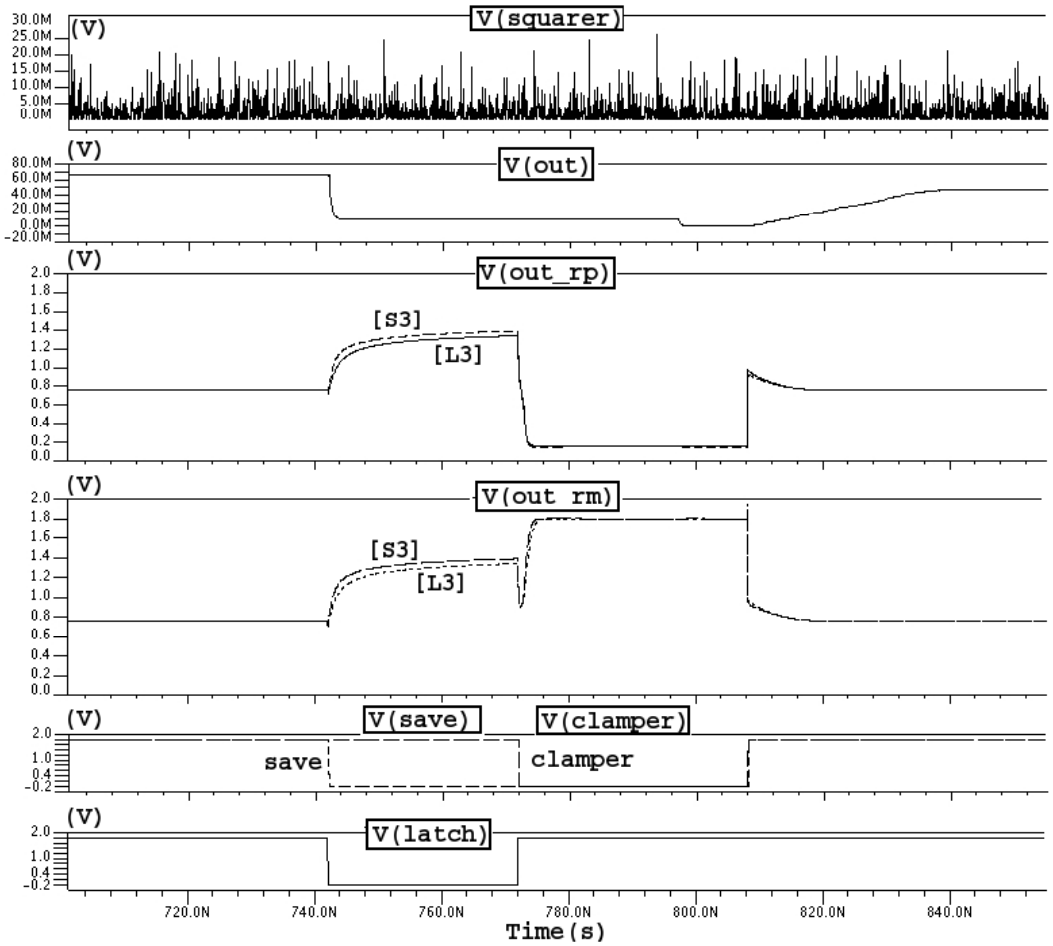

Fig. 11. Comparison between the circuit and post-layout level of the comparator unit

variations. After this, signal `inhibit` is asserted again. Then the same iteration is performed for the `phase1` signal, and afterwards the comparison is executed by rising signal `compare`. In the meantime all comparator signals (`save`, `clamper` and `latch`) are kept high. After the charge redistribution, the comparator is activated in the same way as described in section 4-C. The cycle ends with the assertion of signal `reset` that prepares the device to the next demodulation process. It is also possible to identify the CMFB operation by observing waveforms `V(outp)` and `V(outm)`. The common mode of the signal is about 1 V during all device operation. The two markers in figure show two different demodulation conditions: The marker on the left indicates a demodulation voltage of about -57 mV, while the one on the right identifies a demodulation voltage of about 60 mV. The two cases represent two different information bits, '1' and '0', respectively. Correspondingly, the outputs of the comparator `out_rp` and `out_rm` switch oppositely.

It is interesting to compare the functional simulations at schematic and layout-level. Figure 11 shows the analog comparator operation in the `S3` and `L3`

cases. The differences between the two abstraction levels are not particularly significant.

System-level performance simulations

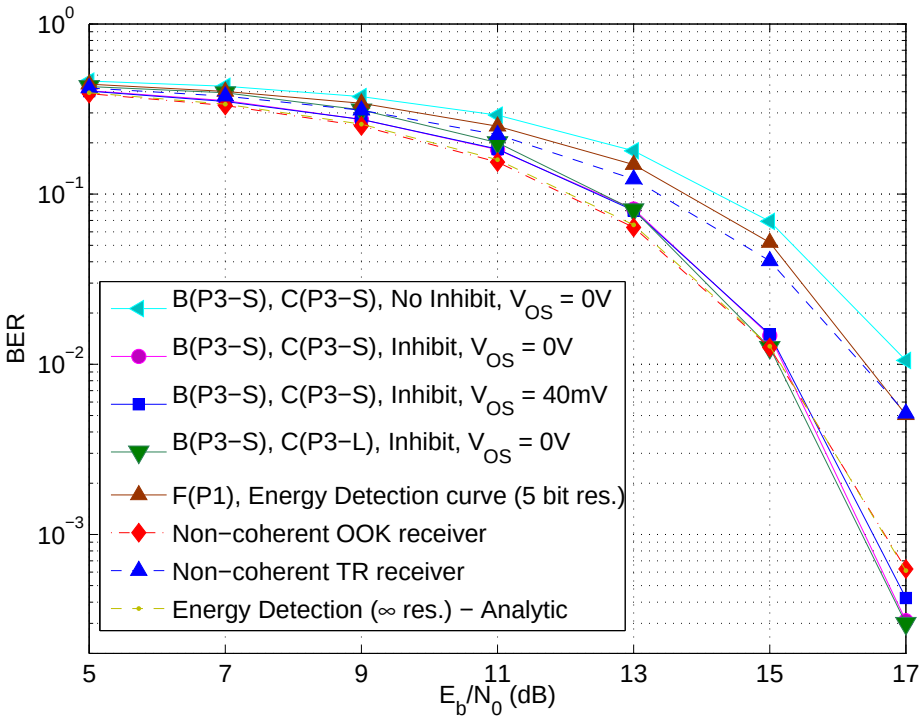

Fig. 12. BER curves comparison at different abstraction levels

Figure 12 shows a collection of BER curves in various conditions and for various receiver types. The simulations aimed at two aspects: The correctness of the hypotheses used in the Bi-phase integrator design and the performance figure of the device with different abstraction levels. First, we show the system-level performance degradation due to the absence of the `inhibit` switch in the integrator unit. Then, by using the full Spice-level unit integrator with the `inhibit` switch we analyze the second aspect, that is the impact of the comparator low-level non-idealities on system-level performance. As an overall result, it is possible to infer important considerations about the required models for the successive design stages. The analises have been carried out through a comparison among the obtained BER and the ideal performance figures of an Energy Detection receiver. In the figure we use a symbolic notation to denote the modeling levels for the receiver blocks. The front-end, the comparator and the Bi-phase integrator are represented by symbols `F`, `C` and `B`, while the values in brackets for these symbols, as defined in section 3, represent the abstraction level: `P1` - Conceptual Phase I, `P2` - Behavioral Phase II, `P3-S` - Spice-level Phase III, `P3-L` - Post-layout level Phase III.

The "Analytic" curve refers to a theoretical Energy Detection receiver with infinite quantization resolution [30]. The `F(P1)` curve refers to a quantization resolution of 5 bits. The other cases refer to the reduced complexity receiver described by a `B(P3-S)` Bi-phase integrator for different abstraction levels of the comparator. In all these cases, the demodulator input range is 160 mV. In case no reset switches across C_p are considered, performance degrades significantly. As previously shown in (5), demodulation is affected by the voltage across C_p stored in each operation phase and by the output voltage of the previous demodulation cycle. If in the integrator no `inhibit` signal is used, the terms $N_{f_{ph0}}^{p,(n)}$ for the first integration phase and the corresponding $N_{f_{ph1}}^{p,(n)}$ for the second one corrupt the final demodulation voltage: Thus, demodulation performance decreases even with an ideal `P2` comparator. In fact, figure shows that the equivalent quantization resolution is worse than an ideal receiver with a 5 bit resolution A/D. On the other hand, thanks to the *Inhibit* switches, the Bi-phase integrator can approximately reach the performance of the theoretical Energy Detection receiver (BER curves overlap). The offset rejection feature of the device is also proven because BER remains almost unvaried if an input referred offset V_{OS} of 40 mV is included in the simulations. These important results permit to verify the correctness of the previously presented theory.

For completeness, figure 12 includes other Impulse-Radio receiver types, Transmitted Reference (TR) and On-Off Keying (OOK) [31]. The curves show better BER performance of ED compared to TR in which no threshold set is required for demodulation. In the case of OOK receivers setting a threshold is mandatory and affects performance. In this case it has slightly worse performance than Energy Detection even though the optimal threshold was chosen.

It is possible to note that the curves `B(P3-S)-C(P3-L)` and `B(P3-S)-C(P3-S)` comparator models differ slightly especially for low SNR. Since the Bi-phase integrator output voltage is low and comparable to the input-referred offset of the comparator stage, for low E_b/N_0 the non-perfect routing in the comparator interconnections generate an input-referred offset which slightly increases the error-rate. For higher E_b/N_0 this unbalanced routing do not influence system level performance because the final demodulation voltage after charge redistribution is higher.

Figure 13 shows the BER of the demodulator at $E_b/N0$=17 dB – which corresponds to an acceptably low BER – as a function of the OTA input signal amplitude. For input signals lower than input range of the OTA (on the order of 250 mV), the BER does not change. Whether the input signal becomes larger, the BER performance decreases. As anticipated in section 4, this distortion does not degrade much the BER figure because OTA saturates only for very short times, corresponding to the duration of the peaks of the UWB signal exceeding the input range. This leads only to a slight degradation of

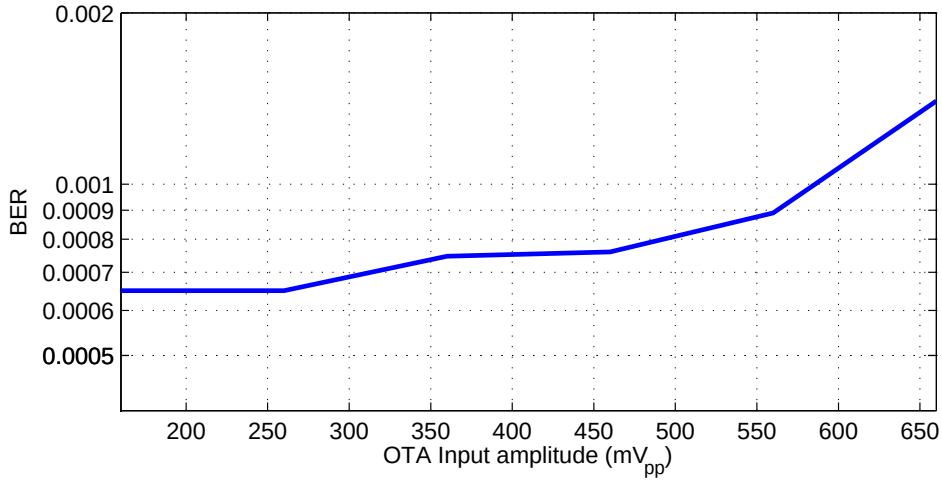

Fig. 13. BER at $E_b/N0$=17 dB for various input amplitudes

the BER. For example an increase of input amplitude from 250 mV to 450 mV leads to a BER degradation of 10^{-4}. As input signal further increases, this effect becomes more relevant, especially at very low signal-to-noise ratios.

The most important non-ideal effect which degrades demodulator performance is related to the input-referred offset of the comparator due to transistor mismatch. Especially at low SNR, since noise power level is comparable to UWB signal strength, the output voltage of the integrator is comparable to the input-referred offset of the comparator. The simulation with input offset voltage up to 10 mV do not show BER degradation if the input signal level is sufficiently high. This requires having an overall gain of the front-end before the OTA of 40 dB, which is compatible with other works [7].

The curves of figures 12-13 identify the limits below which the receiver works almost ideally. If input signal's amplitude is below 250 mV and input-referred offset is less than 40 mV, the results are more or less the same regardless of the abstraction level used for the various blocks, that is AMS, schematic or layout level. Therefore, in order to save simulation time, it is possible to design the remaining part and simulate the whole receiver's front end by using a P2 view of the already designed blocks. A summary of the obtained results both at circuit and system level is shown in table 5. As far as performance in concerned, there is no BER degradation with respect to the ideal case using a P1 or P2 description, as physical effects are abstracted away. On the contrary, schematic and layout level P3 descriptions allow to include and evaluate such effects.

Table 5 also summarized power consumption figures that can be evaluated in P3. When the device is idle and no signal is present at the input, the quiescent power consumption P_Q, inclusive of biasing circuit, is 400μ W. During normal operation, the power consumption P_D, averaged on 4 ms of demodulation ac-

Table 5
Results obtained during the refinement phases P1, P2 and P3

	P1	**P2**
Circuit-level	None	Block identification
System-level (BER)	Ideal ED receiver	Ideal ED receiver
	P3-S	**P3-L (Hybrid P3-S/P3-L)**
Circuit-level	P_Q=400μ W, P_D=1 mW	P_Q=400μ W, P_D=950μ W
System-level (BER)	Fig. 12, `B(P3-S)-C(P3-S)`, almost ideal	Fig. 13, 10^{-4} loss at 450 mV swing

tivity, is 1 mW in P3-S and 950 μW in P3-L because the optimized layout has smaller parasitics than the overestimated ones of the schematic level. With respect to [7], in which the overall receiver consumes 2.5 nJ/bit at 16.7 Mbit/s V_{al}=0.65V, here the energy spent by the demodulator is 190 pJ/bit at 5 Mbit/s and $E_b/N0$ =15 dB, V_{al}=1.8V.

Typical UWB receiver implementations have power consumption ranging from 1 mW to 330 mW. This huge diversity is due to the transmission technology used, Multi Band-OFDM or Impulse-Radio and to the technology process. For the Impulse-Radio PPM receivers power consumption is in the range 30-40 mW and energy per bit varies between 1 and 3 nJ/bit. The highest power contribution is due to the front-end units, which must provide a gain of about 40 dB [7]. Supposing the power gain of a single LNA cannot exceed 20 dB in the best case, the required front-end gain can be obtained by cascading one LNA with other gain stages. Typically the LNAs for Impulse-radio would consume 9 mW [32]. Since our demodulator consumes only 1 mW and its area is way smaller than the first RF front-end units, it contributes only for a small portion of the power-area budget. Wrapping up the obtained results with other data from the literature we can expect a peak power of 15-20 mW for the overall receiver. Moreover, it is understood that wireless applications in which IR-UWB is bound to be employed will work at extremely low duty-cycles, thus allowing to switch off the front-end blocks during idle times therefore reducing power to a few percent of the peak [33].

Another important consideration regarding the performance of Energy Detection UWB receivers is narrow-band interference.The BER performance depends on the strength, number and physical position of the transmitters [34]. Provided that the receiver front-end does not saturate, since the demodulator has about ideal performance, the effect of interference is about the same as for ideal Energy Detection receivers. Hence, for decreasing interference sensitivity we address the reader to the specific literature. For instance, in TR receivers attenuating in-band interference by using notch filters or increasing Signal-to-Interference ratios (SIR) by using feedback loop mechanisms are standard techniques [35].

It is also fundamental that receiver can recover synchronization in presence of such a simplified hardware. We demonstrated in [36] how to achieve synchronization with this simple Bi-phase demodulator. The synchronization functionality is obtained using only the 1-bit output of the comparator and a searchback algorithm applied on an ordered collection of differential energies: These are obtained by delaying the `Phase 0` and `Phase 1` windows and by shifting the integrations linearly within the PRI.

6 Conclusions

This paper presented a new CMOS 0.18 μm 2-PPM demodulator architecture based on a $G_m - C$ open loop integrator, a switched capacitor network and an analog comparator. The circuit has been designed and simulated using an ad-hoc methodology based on a "substitute-and-play" approach which allows to change the abstraction level in the simulations. Thanks to an ad-hoc testbed and the simulation tool ADVanceMS, it is possible to change the block descriptions and modify the simulation accuracy. The environment employs a realistic channel model and offers the possibility to include both BSIM3 MOSFET and layout backannotated models with distributed RC parasitics. BER results show that the device has about the same performance of an ideal Energy Detection receiver employing infinite A/D resolution.

Once the circuit layout has been fully completed, mixed-signal insulation techniques will be essential to prevent that the other front-end devices compromise the transconductor and the comparator operations. Considering the results obtained in this work, final design steps such as layout of the Bi-phase integrator and silicon fabrication are worthy of consideration, and we plan to focus on that our forthcoming work.

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