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Behavioral Models of Input/Output Buffers Including Core Noise Coupling

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Abstract

This paper addresses the generation of enhanced models of the input/output buffers of digital integrated circuits. The proposed models overcome the current limitations of the state-of-the-art models and can be obtained from device port transient responses only. They can be effectively implemented as SPICE subcircuits in any commercial tool for signal integrity or core noise simulations.

Introduction

Nowadays, the assessment of signal integrity and electromagnetic compatibility effects of digital circuits via numerical simulation is required at the early stage of their design. In this scenario, the availability of accurate and efficient models of the ports of the active components, as the Input/Output (I/O) buffers of digital Integrated Circuits (ICs) is a key resource for accurate predictions.

Traditionally, buffer macromodels are based on simplified equivalent circuits and the Input Output Buffer Information Specification (IBIS) [1]. IBIS models are widely supported by manufacturers and accepted by most Electronic Design Automation (EDA) tools, despite some limitations. Recently, other approaches to IC buffer macromodels, that supplement the IBIS resource and provide improved accuracy, have been proposed [2, 3]. These approaches are based on system identification methods and parametric relations [4,5]. They exploit a mathematical description of current and voltage evolution at the buffer port, possibly reproducing complicated dynamic nonlinear behaviors of the modeled devices.

Even if in principle an I/O buffer cell is a simple circuit designed to interface internal logical signals of the IC core to the external interconnect, the complexity of these devices has recently increased. The I/O cells include a pre-buffer stage, a level-shifter (to allow for different supply voltage values) and possible additional blocks for enhanced features like pre-emphasis. The complexity along with the lack of accuracy of the state-of-the-art models in reproducing the rich dynamical behavior of these devices demand for the refinement of the existing models to generate accurate and efficient multiport dynamical models of the buffer circuits. This paper presents a possible solution of this problem based on parametric relations [2]. Additionally, macromodels obtained by this parametric approach remain almost as efficient as macromodels based on IBIS data and can be easily included in EDA tools.

Basic Structure of I/O Buffer models

This Section briefly reviews the basic structure of the macromodels for I/O buffers. For the sake of simplicity, the discussion is based on the output buffer of a single-ended device, whose simplified scheme is shown in Fig. 1. For this structure, present macromodels provide the behavioral

description of the output section only under the simplifying assumption of an ideal pre-driver stage. They concentrate on the description of the output and the external supply port currents $i_1(t)$ and $i_2(t)$, respectively. As an example, the model structure of the output port current is based on the following two-piece model representation

$$i_1(t) = w_H(v_1, v_2, t) i_H(v_1, v_2, t) + w_L(v_1, v_2, t) i_L(v_1, v_2, t) \quad (1)$$

where i_H and i_L are submodels accounting for the device behavior in the logic high and low state, respectively, and the time-varying functions $w_H(t)$ and $w_L(t)$ play the role of the input signal $v_4(t)$ and provide the transition between the two submodels, i.e., the switching between the two logic states. A similar relation holds for the supply current $i_2(t)$. Submodels i_H and i_L can be obtained from either simplified equivalent circuit representations (e.g., see IBIS [1]) or identification methods and parametric relations [2,3].

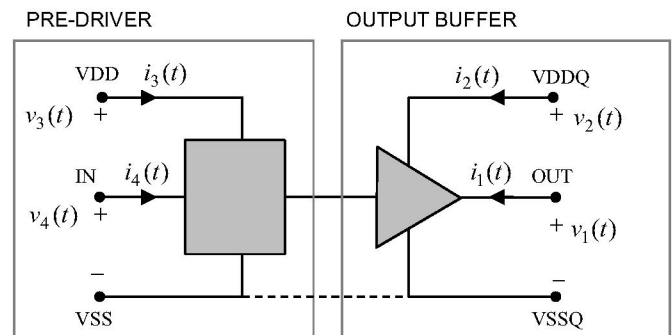


Fig. 1 Structure of the output buffer of a digital integrated circuit with its relevant electrical variables.

The current models have been proven to be effectively used for system-level signal integrity simulations at PCB level [2]. However, the lack of a detailed description of the pre-driver stage and of the possible dynamical effects of the coupling among the functional and supply ports of the two blocks of Fig. 1 prevent the use of these models for different applications, like the core noise simulations. Furthermore, the models are based on the simplifying assumption that the variations of the external supply voltage is small, thus not allowing the simulation of stacked System in Package (SiP) devices, where the voltage fluctuations can be on the order of 30% of the nominal supply voltage values.

Enhanced models

In order to provide an enhanced behavioral multiport model for the basic structure of Fig. 1, the following general representation is considered

$$\begin{cases} i_1(t) = F_1(v_1, v_2, v_3, v_4, t) \\ i_2(t) = F_2(v_1, v_2, v_3, v_4, t) \\ i_3(t) = F_3(v_1, v_2, v_3, v_4, t) \\ i_4(t) = F_4(v_1, v_2, v_3, v_4, t) \end{cases} \quad (2)$$

where

- F_1 and F_2 account for the nonlinear dynamical behavior of the output stage of the buffer. They are described by model representations like the one of eq. (1) where the different parts, i.e., the submodels i_H and i_L and the weighting signals w_H and w_L , have been suitably modified as suggested in [3] to account for the large fluctuations of the power supply voltage values. In addition, the dependence of the possible different shapes of the input signal are embedded in the definition of the weighting signals w_H and w_L . A threshold detection mechanism is also introduced to synchronize the effects of the static power supply values on state switching events.
- F_3 and F_4 account for the supply current and the input port current of the pre-driver stage and are defined by dynamical parametric models like these used for the submodels of (1). Preliminary results on the modeling of the input port of a driver can be found in [2].

Once the model structure defined by the nonlinear multivariate equation defined by (2) has been assumed, the parameters of the different representations defining F_3 , F_4 and the submodels in F_2 and F_3 are estimated by fitting the model responses to suitable device transient responses. The model parameters are computed by minimizing a suitable error function between the voltage and current waveforms of the model and of the real device. Specific algorithms are available to solve this problem, depending on the choice of the family of basis functions used to define the parametric models. As an example, the method collected in [6] can be used for LLSS representations, that have been successfully used for IC macromodels [3]. More details on the generation of the device responses for parameter estimation are in [2,3].

Model validation

In this Section, the proposed modeling approach is applied to a single-ended CMOS driver with pre-emphasis. The nominal values of the power supply voltages are $VDDQ=1.8V$ and $VDD=1.5V$ and the approximate device switching time is $0.5ns$. The reference responses of the HSPICE detailed transistor-level description of the device are used for both the generation of the device port responses required by the modeling procedure outlined in the previous Section and for model validation.

Test case #1: ideal supply voltages and different v_{IN}

As a first validation, a test setup consisting of the example device producing a '010' bit sequence on an open-ended ideal transmission line (characteristic impedance $Z_0 = 50\Omega$, delay $T_d = 1ns$) is considered. In this test, the supply voltages of the buffer are kept constant at their nominal values and three different input signals $v_{IN}(t)$ are considered. The three inputs are defined by a trapezoidal voltage source with different rise/fall times. Figure 2 shows the input signals $v_{IN}(t)$ and the device port voltage response $v_{OUT}(t)$, thus highlighting the

accuracy of the proposed model to account for the different shapes of the input signals. For the three sets of responses, the timing errors of the curves of the bottom panel of Fig. 2 are less than 15ps, for both the up and the down state transitions. The timing error is defined as the maximum delay between the reference and the model responses measured for voltage v_{OUT} crossing a threshold set at 1V.

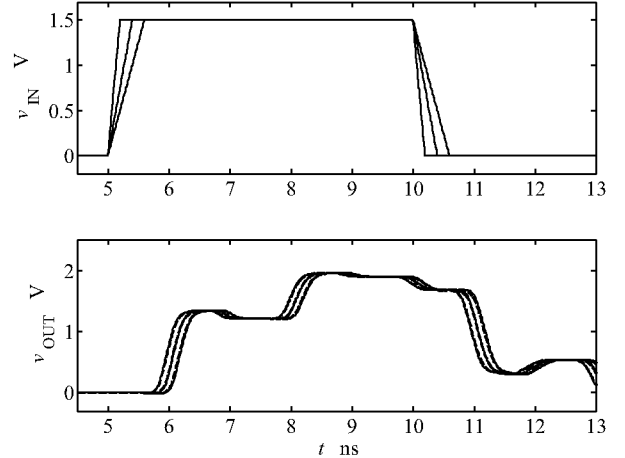


Fig. 2 Test case #1: device port voltage responses $v_{OUT}(t)$ (bottom panel) computed for three different input signals $v_{IN}(t)$ (top panel) defined by a trapezoidal waveform with 0.2ns, 0.4ns and 0.6ns transition times. Solid line: reference, dashed line: macromodel.

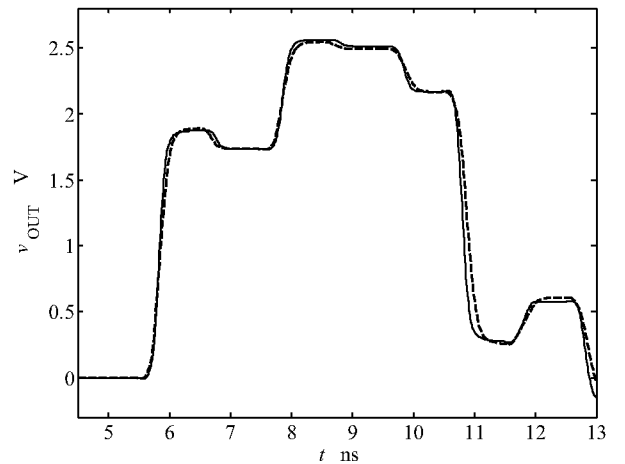


Fig. 3 Device port voltage response $v_{OUT}(t)$ of the example device for the validation test case #2 (see text). Solid line: reference, dashed line: macromodel.

Test case #2: large static variation of $VDDQ$

As a second validation, a test setup consisting of the example device driving an open-ended transmission line ($Z_0 = 50\Omega$, $T_d = 1ns$) and supplied by an ideal battery connected at the $VDDQ$ pin. The supply voltage is 130% of the nominal $VDDQ$ value. Figure 3 shows the device output port response $v_{OUT}(t)$ for this test case. Even for this extreme condition, the model provides a very good replica of the reference response, with timing errors of 20ps and 70ps for the up and the down transitions, respectively. This comparison highlights the ability of the model to yield good results also for supply

voltage levels very far from the normal operation of the device.

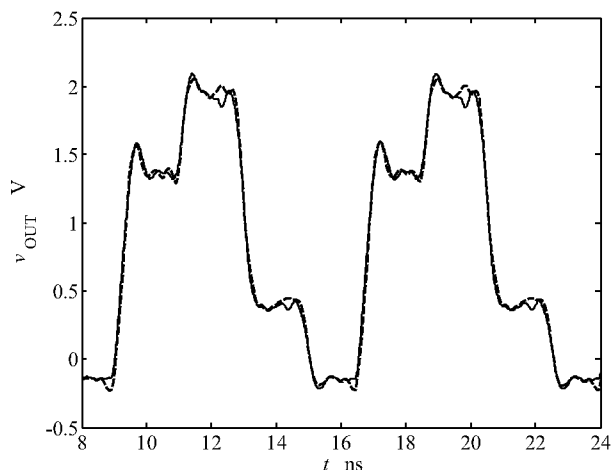


Fig. 4 Device port voltage response $v_{OUT}(t)$ of the example device for the validation test case #3 (see text). Solid line: reference, dashed line: macromodel.

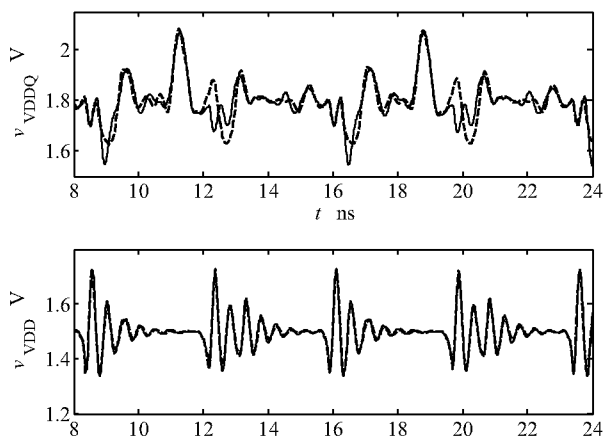


Fig. 5 Supply voltage fluctuations $v_{VDDQ}(t)$ and $v_{VDD}(t)$ of the example device for the validation the test case #3 (see text). Solid line: reference, dashed line: macromodel.

Test case #3: non-ideal power distribution

As a final validation, we propose a test case where the power supply pins VDD and VDDQ of the example device are connected to their respective supply batteries through lumped RLC equivalents of the distribution networks ($R=100\text{m}\Omega$, $L=3\text{nH}$, $C=0.5\text{pF}$). Again, the device produces a pulse on an ideal open-ended transmission line load ($Z_0 = 50\Omega$, $T_d = 1\text{ns}$). Figure 4 and Figure 5 show the output power supply port voltage responses, thus highlighting the accuracy of the proposed models in reproducing both the functional signals and the powers supply fluctuations. The timing errors of the curves of Fig. 4 are less than 10ps.

Application

In this Section, the proposed models are used for a more realistic application that involves both quiet and switching devices that are energized by common supply networks. The assessment includes both the prediction of the effects of the

power supply and device activities and of the coupling between the VDD and the VDDQ power distribution networks. A test circuit composed by four identical open-ended transmission lines ($Z_0 = 50\Omega$, $T_d = 1\text{ns}$) driven by four replicas of the modeled device is considered. The power supply pins of every driver is connected to a common power supply structure that is modeled by a lumped RLC structure ($R=100\text{m}\Omega$, $L=3\text{nH}$, $C=0.5\text{pF}$) connected to the corresponding 1.8 V and 1.5 V supply batteries. Two devices are driven to switch simultaneously (random bit stream "01010..."), while the other two devices are kept to the fixed logic high and low state.

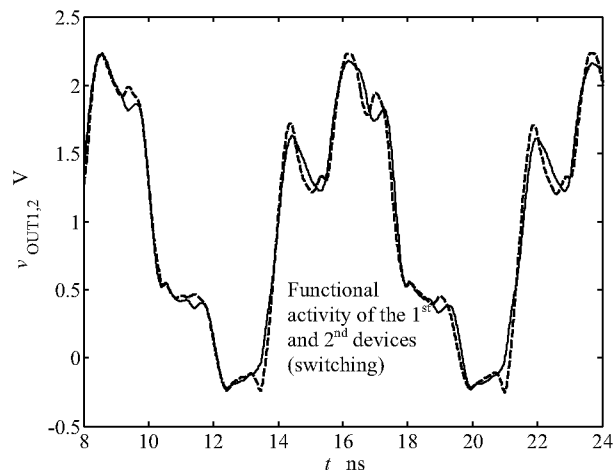


Fig. 6 Device port voltage response of the two active devices for the application test case (see text). Solid line: reference, dashed line: macromodels.

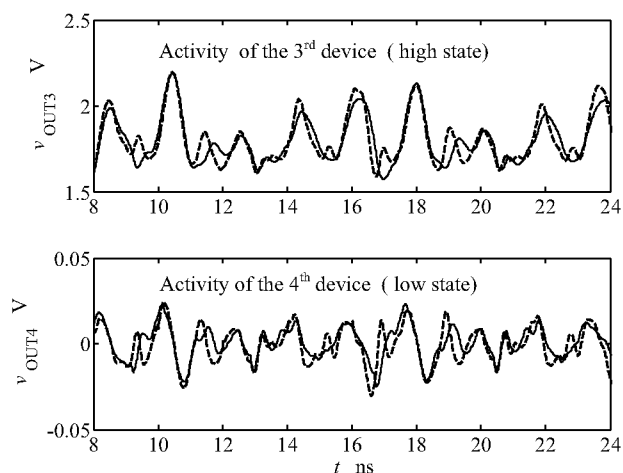


Fig. 7 Device port voltage responses of two devices kept in a fixed state for the application test case (see text). Solid line: reference, dashed line: macromodels.

Figures 6 and 7 show the comparison between the reference and the predicted functional voltage waveforms at the output pin of the four devices. The model predictions and the reference responses are in good agreement, thus leading to timing errors less than 70ps and a good accuracy in reproducing the rich dynamical voltage ripple of the output voltage of the quiet devices. Figure 8 shows the total power

supply voltage fluctuations. From this comparison, it is clear that the proposed models can be effectively used to predict both the functional signals of devices and their supply voltage fluctuations, possibly due to the coupling among the different supply and output pins of the devices.

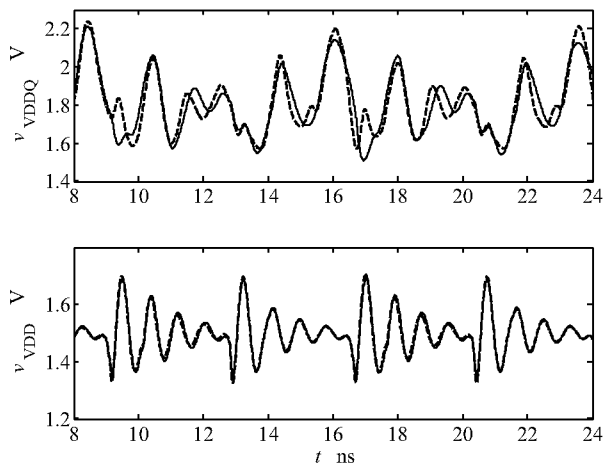


Fig. 8 The total power supply voltage fluctuations of the common reference voltages VDD and VDDQ for the application test case (see text). Solid line: reference, dashed line: macromodels.

Conclusions

This paper addresses the generation of enhanced models of the I/O buffers of digital ICs. The proposed models are a multiport mathematical description of the buffer circuits. They overcome the current limitations of the state-of-the-art models in reproducing the behavior of real devices for large fluctuations of the supply voltages; also they include the coupling among all the different supply pins of the device and can be driven by input signals with arbitrary shapes.

The models can be easily estimated from port transient responses and can be effectively implemented in any commercial tool for signal integrity or core noise coupling simulations.

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