Behavioral Models of IC Output Buffers from on-the-fly measurements

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Igor S. Stievano, *Member, IEEE*, Ivan A. Maio, *Member, IEEE*, and Flavio G. Canavero, *Fellow, IEEE*

***Abstract*—This paper addresses the development of accurate and efficient models of the output ports of digital integrated circuits (ICs). The proposed approach is based on the estimation of suitable mathematical relations reproducing the external behavior of devices. Device models are obtained through a well-established procedure from port transient voltage and current responses recorded during the normal activity of the IC mounted on a real board, thus avoiding specific modeling setup and test fixtures. The efficiency of the approach is demonstrated on real devices from both numerical simulations and actual measurements.**

***Index Terms*—Circuit modeling, digital integrated circuits (ICs), electromagnetic compatibility, input–output ports, macromodeling, signal integrity, system identification.**

I. Introduction

THE DESIGN of modern electronic equipment operating in the gigahertz range requires, at the early stage of the design process, the assessment of signal integrity/electromagnetic compatibility effects on critical interconnect paths. Such an assessment, which is achieved by the simulation of signals propagating on interconnect structures like the one sketched in Fig. 1, relies on the availability of accurate and efficient behavioral models (or macromodels) of the ports of digital integrated circuits (ICs) that act as the nonlinear terminations of interconnects. As an example, a behavioral model for the output buffer in Fig. 1 is represented by a suitable nonlinear dynamic relation between the voltage v and the current i of the device port.

Different approaches are used to obtain IC port models. The most common approach is based on simplified equivalent circuits derived from the internal structure of the modeled devices. This approach leads to the I/O Buffer Information Specification [1], which is widely supported by electronic design automation tools and dominates modeling applications. More recent approaches are based on the use of parametric relations to approximate the device port equations and on the identification of their parameters from device responses [2]–[6]. These approaches offer enhanced modeling capabilities, which facilitate and improve the modeling of recent devices, such as preemphasis drivers [7].

For both approaches, however, the generation of models requires the availability of transistor-level models of the device or the capability to control the device operation, i.e., the use of dedicated test fixtures to stimulate and measure specific device behaviors. As an example, the estimation of parametric models for the output buffer in Fig. 1 exploits port responses recorded while the buffer is forced (e.g., through the internal logic signal v_i) in a fixed logic state or is forced to perform complete state switchings [3]–[5] on suitable test loads. As a result, the model generation of real devices with a complex core becomes impractical. The logic state of the buffers, in fact, cannot be easily controlled since it is decided by the specific software code running only on the IC core.

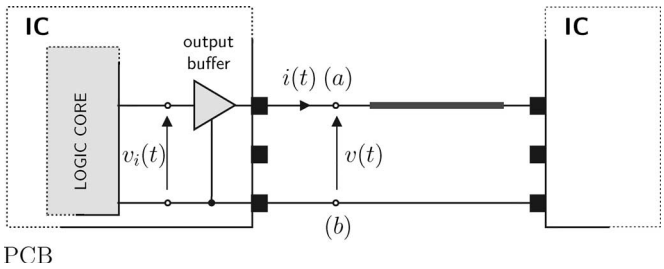

Fig. 1. Typical interconnect structure with the main IC blocks and the relevant electrical variables.

In this paper, the technique recently proposed in [2] has been applied to the generation of behavioral models of real devices from actual measurements, avoiding the need for dedicated test fixtures and device control. The models are obtained from device port transient responses measured on a real board with devices operating in normal conditions, as in the simplified scheme in Fig. 1.

II. Model Structure and Estimation

Behavioral models of the output buffers of digital ICs exploit the following two-piece parametric relation:

$$i(t) = w_H(t) i_H(v, d/dt) + w_L(t) i_L(v, d/dt) \qquad (1)$$

where w_H and w_L are switching signals accounting for the device state transitions and playing the same role as the internal voltage v_i in Fig. 1, and i_H and i_L are nonlinear parametric relations accounting for the device behavior in the fixed high and low logic states, respectively [9]. More details on the model representation (1) and on the use of parametric relations for the modeling of IC ports can be found in [3] and references therein.

The estimation of model (1) amounts to computing the parameters of submodels i_H and i_L and the weighting signals w_H and w_L from suitable port voltage $v(t)$ and current $i(t)$ responses. Model parameters are computed by minimizing

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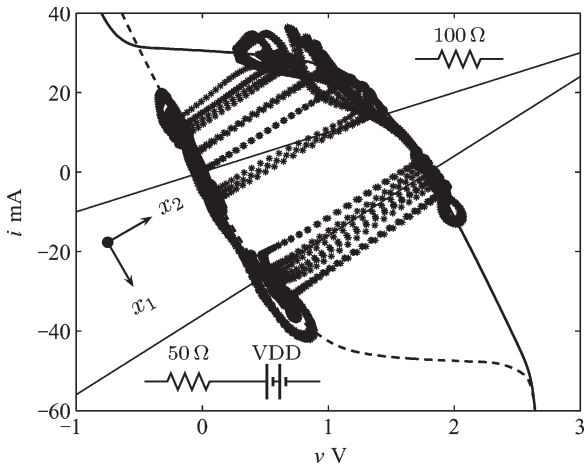

Fig. 2. Static characteristics of the example driver in the (solid thick line) fixed high state and (dashed thick line) low state superimposed on the characteristics of two lumped resistive loads and the (star line) samples $\{v(t), i(t)\}$ of the port transient responses in Fig. 3.

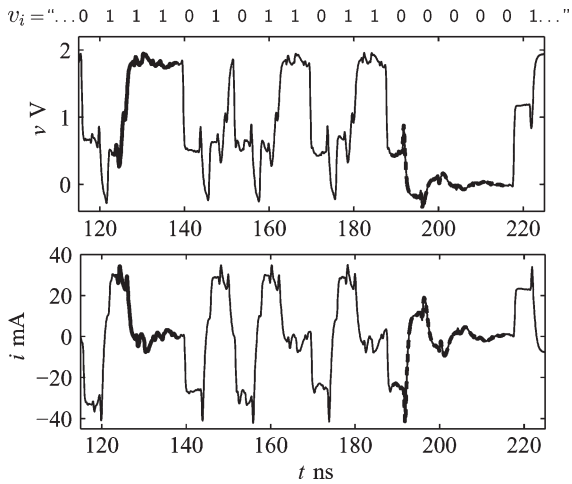

Fig. 3. Output port voltage $v(t)$ and current $i(t)$ responses computed for the example driver connected as in Fig. 1 with a mismatching stub placed between terminals (a) and (b) (see text). The thick parts of the $v(t)$ and $i(t)$ signals are the waveforms used for the estimation of submodels i_H and i_L in (1) (see text for details).

suitable error functions between the model responses and the measured port responses, which are used as references to be fitted [9], [10].

The problem addressed in this paper is how to obtain device responses useful for model parameter estimation while the device is mounted on an application board and operates in normal mode. For the sake of simplicity, the discussion is based on the output port of a commercial Texas Instruments transceiver, whose HSPICE transistor-level description is available from the official website of the vendor. The example device is an 8-bit bus transceiver with four independent buffers (model name SN74ALVCH16973 and power supply voltage $V_{DD} = 1.8$ V). The example device operates at 167 Mb/s, i.e., the bit time is 6 ns, and is driven to produce a 2048-long pseudorandom bit stream. The HSPICE simulations of the transistor-level model of the driver are assumed as the reference curves hereafter.

Fig. 2 shows the static characteristics of the example device and trajectories of device transient response in the output voltage and current plane. The upper (lower) curve is the device output static characteristic when the device is in the high (low) logic state, and the clouds of dots are samples of output current and voltage transient responses recorded during ordinary switching operations. The output transient responses leading to the trajectories in Fig. 2 are shown in Fig. 3 and are recorded while the device is connected as in Fig. 1. This circuit is composed of a standard point-to-point topology augmented by a shunting stub connected between terminals (a) and (b). From the experimental point of view, this circuit can be easily obtained by shunting the proper trace of an application board. Fig. 2 highlights that the transient responses obtained with the shunting stub can densely explore the portion of voltage and current plane around the device static output characteristics. Hence, they are good candidates to serve as the identification of model parameters. In contrast, transient responses obtained by connecting different loads, such as simple resistors, cannot be effectively used for the estimation of model parameters. These responses, which explore a very small portion of the output variables, do not exhibit the rich dynamical behavior shown in Fig. 2, which is extremely important during the estimation phase to obtain accurate models including all the relevant dynamics of the original device.

These observations suggest a two-step procedure for the estimation of model (1).

1) *Estimation of submodels:* As in [3], the parametric models used for i_H and i_L in (1) are discrete-time parametric representations based on sigmoidal expansions [9], whose parameters can be estimated by standard algorithms as in [10]. The waveforms for the estimation of submodel $i_H(i_L)$ must be sampled voltage and current transient responses containing enough information on the port dynamic behavior while the device is in the high (low) logic state. For the example device, the estimation waveforms of i_H can be obtained from the solid thick parts of the signals $v(t)$ and $i(t)$ in Fig. 3. These signals are obtained by considering the slice of the port responses recorded while the device is kept through the internal (nonaccessible) input signal v_i in the fixed high state for a number of consecutive logic states. Similarly, the estimation waveforms of submodel i_L can be the dashed thick parts in Fig. 3.

   To facilitate the modeling process, the estimation of submodels is carried out in terms of the auxiliary variables (x_1, x_2) defined by the following linear transformation:

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 1 & -Z_0 \\ 1 & Z_0 \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} \tag{2}$$

   where Z_0 corresponds to the approximate value of the characteristic impedance of the typical interconnect structures loading the device. For the example in Fig. 2, $Z_0 = 50\ \Omega$. Submodels i_H and i_L, in fact, must be defined over the same range of the (voltage) input variable values. In the (x_1, x_2) plane, the trajectory of state transitions have nearly constant x_1 values (see Fig. 2), thereby leading to a reduced modeling range for the x_1 input variable.

2) *Computation of weighting signals:* The weighting signals w_H and w_L are computed after the estimation of submodels i_H and i_L from port responses occurring during state switchings, as discussed in [3]. In our problem, this amounts to solving the single linear (1), where v and i are the voltage and current responses recorded during single transition events while the device operates in regular conditions as in Fig. 1, and w_L is assumed to be $w_L = (1 - w_H)$. In principle, such an assumption can be removed, and two sets of port responses can be used to compute two independent w_H and w_L signals. However, the latter simplification benefits the quality of the complete model since it reduces possible ill conditioning or inaccuracies of the solution of the linear problem arising from noisy measured data or from the approximated responses of submodels i_H and i_L.

Once all model parameters are computed, the model equations are converted into a macromodel to be plugged in a standard simulation environment, e.g., SPICE or any hardware description language allowing for analog parts. Implementation details are described in [3].

III. Validation Results

In this section, the proposed on-the-fly methodology has been validated by applying it to the modeling of the output ports of two examples from device port responses obtained by means of SPICE simulations or actual measurements. The examples considered in the paper are the same transceiver SN74ALVCH16973 as in the previous section, i.e., a virtual device defined by its detailed SPICE transistor-level model, and the HC7404 IC.

Example 1: As a first example, which is devised to assess the feasibility of the approach, the device-level model of the transceiver SN74ALVCH16973 is considered. The behavioral model of the output port of this example has been obtained by applying the proposed modeling procedure as outlined in the previous section. In summary, parts of the sampled port voltage and current responses shown in Fig. 3 are used to estimate model parameters. The port responses are recorded while the device operates in normal mode as in Fig. 1, and a perturbing element is connected between terminals (a) and (b). For the simulations in Fig. 2, the perturbing element is a stub modeled as an ideal transmission line (characteristic impedance $Z_0 = 50\ \Omega$ and time delay $T_d = 2$ ns) loaded by a 10-pF capacitor. The sampling period used to sample the port responses is 20 ps, and the parametric models estimated for i_H and i_L in (1) turn out to have both a dynamic order of three and are composed of two and three sigmoidal terms, respectively [3]. Once the submodels i_H and i_L in (1) are estimated, the weighting signals w_H and w_L are computed by linear inversion of the model equation as detailed in [3]–[5] from the same thick parts of the up and down voltage and current transitions shown in Fig. 3.

The complete two-piece model (1) has been validated by comparing its static characteristics and transient responses to suitable test loads with those obtained from the reference transistor-level model of the example driver. All the responses of the reference model and of the SPICE-type implementation of the macromodel are computed by means of HSPICE.

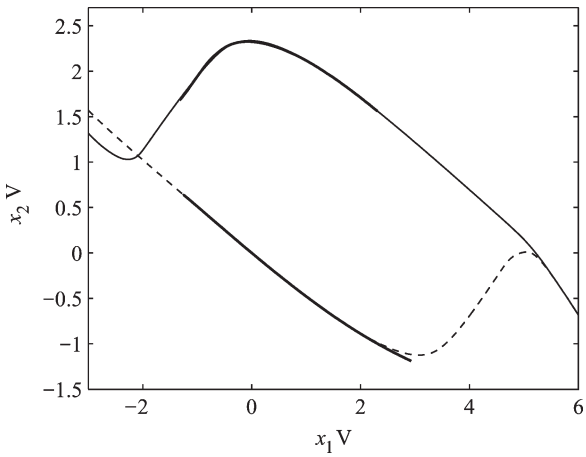

Fig. 4. Static characteristics of (solid thick curves) submodels i_H and i_L in (1) superimposed on the actual characteristics of the (solid line) example driver in the fixed high state and (dashed line) low state.

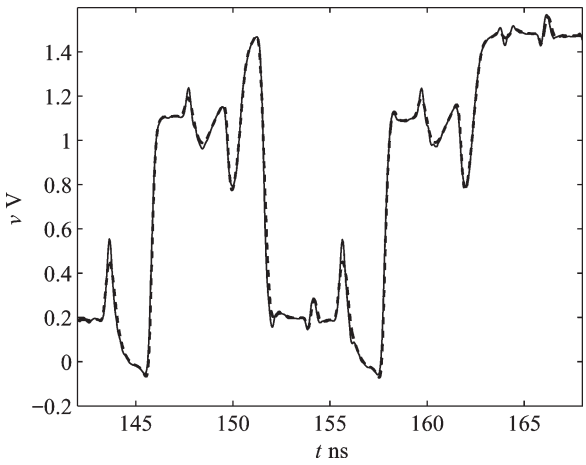

Fig. 5. Port voltage $v(t)$ response computed for the example driver connected to an ideal transmission line load (characteristic impedance $Z_0 = 50\ \Omega$ and time delay $T_d = 1$ ns) loaded by the shunt connection of a 100-Ω resistor and a 5-pF capacitor.

As a first test, Fig. 4 shows the comparison of the actual static characteristics of the device and the static characteristics of submodels i_H and i_L. This comparison confirms the accuracy of the estimated models to capture the static information of the device. Additionally, Fig. 5 shows part of the port voltage waveform $v(t)$ computed by the reference transistor-level model and the macromodel and recorded while the driver is connected to a distributed load different from the one used in the estimation process. The validation load is an ideal transmission line (characteristic impedance $Z_0 = 50\ \Omega$ and time delay $T_d = 1$ ns) loaded by the connection of a 100-Ω resistor and a 5-pF capacitor. The comparison in Fig. 5 highlights the high accuracy of the complete macromodel running in normal operation conditions.

As a second and more realistic test, which is aimed at verifying the feasibility of the proposed approach for the generation of macromodels from actual measurements, the estimation of

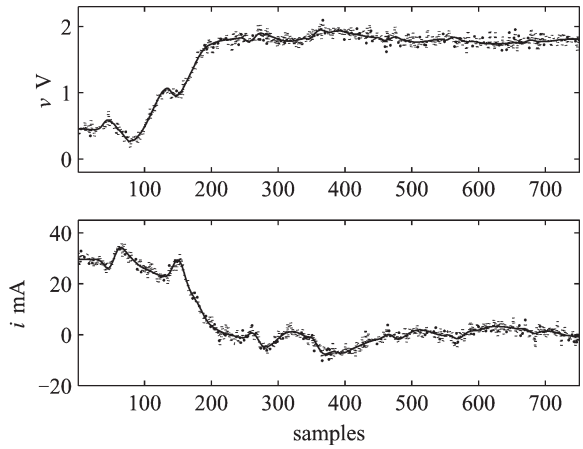

Fig. 6. Port voltage $v(t)$ and current $i(t)$ signals used for the estimation of submodel i_H, i.e., the solid thick signals in Fig. 3, with a superimposed Gaussian white noise with standard deviation $\sigma = 4\%$ of the voltage and current swing.

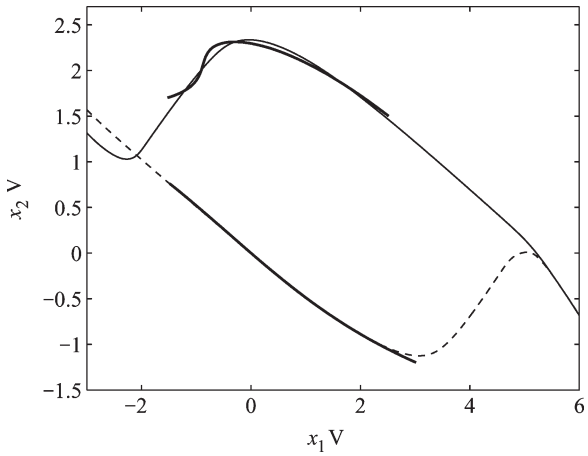

Fig. 7. Static characteristics of (solid thick curves) submodels i_H and i_L in (1) estimated from noisy signals superimposed on the actual characteristics of the example driver in the (solid line) fixed high state and (dashed line) low state.

submodels i_H and i_L has been carried out from noisy measurements. For this second test case, the estimation of submodel parameters is carried out by means of the algorithm [11]. The aforementioned algorithm is a modification of the basic version [10] used for the noiseless case in which a suitable penalty function is introduced in the minimization scheme to average the effects of noise and, thus, to avoid problems of spurious dynamics of estimated models. As an example, Fig. 6 shows the transient responses used for the estimation of submodel i_H that are corrupted by a superimposed Gaussian white noise with standard deviation $\sigma = 4\%$ of the voltage and current swing. Fig. 7 shows the comparison of the actual static characteristics of the device and the static characteristics of submodels i_H and i_L, whereas Fig. 8 shows part of the port voltage waveform $v(t)$ computed by the reference transistor-level model and the macromodel and recorded while the driver is connected to the same validation load of the previous test. The comparison carried out in this second test highlights the robustness of the proposed estimation procedure and the good accuracy of the complete macromodel estimated from online measured data.

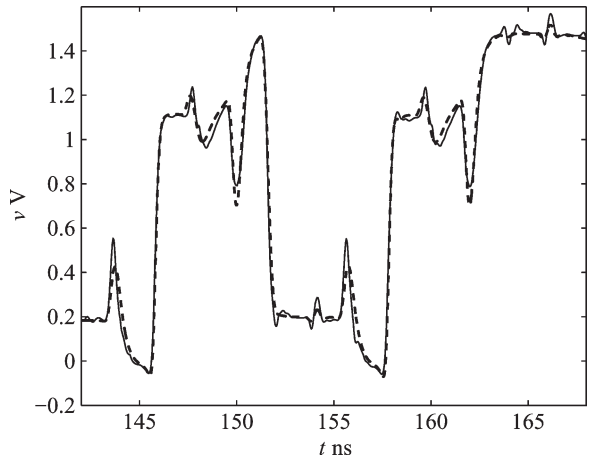

Fig. 8. Port voltage $v(t)$ response computed for the example driver connected to an ideal transmission line load (characteristic impedance $Z_0 = 50\ \Omega$ and time delay $T_d = 1$ ns) loaded by the shunt connection of a 100-Ω resistor and a 5-pF capacitor. Solid line: Reference. Dashed line: Macromodel estimated from noisy signals.

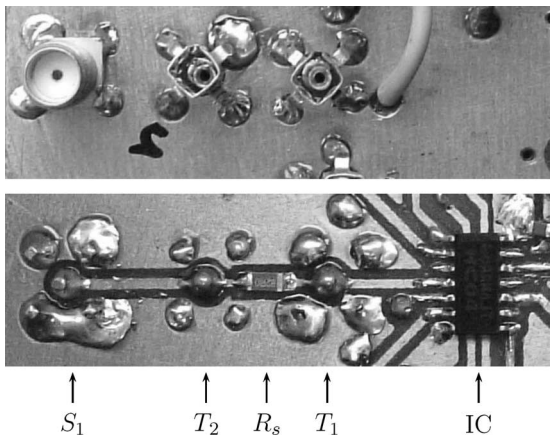

Fig. 9. Test fixture for the experimental characterization of the output port of the HC7404 IC. (Top panel) Back. (Bottom panel) Front. $R_s = 82.6\ \Omega$ is an SMD resistor connected in series to the output port; T_1 and T_2 and S_1 are the terminals shown in the equivalent circuit in Fig. 10 and correspond to two probe tips (T_1 and T_2) and to an SMA connector (S_1) mounted on the back side of the board.

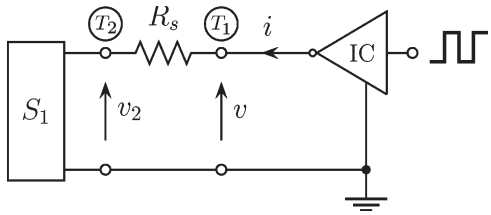

Fig. 10. Equivalent circuit of the identification setup.

Example 2: As a second example, which is devised to test the application of the modeling approach on a real device, an HC7404 IC is considered. Such a device is both simple and representative to be an easy and significant test case. In this example, the signals required by the estimation of model (1) are obtained by means of the test fixture in Fig. 9, whose equivalent circuit is shown in Fig. 10. In this equivalent circuit, terminals T_1 and T_2 are the pin of the port under modeling and the far-end terminal of the series resistor R_s, respectively. Terminals T_1

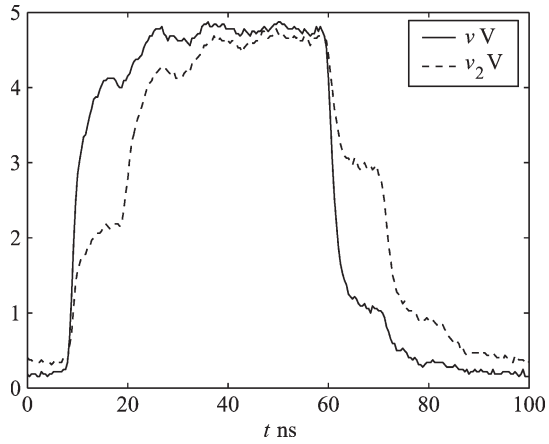

Fig. 11. Measured voltage responses $v(t)$ and $v_2(t)$ obtained by means of the test fixture in Fig. 9 and used for the estimation of model parameters (see text and the equivalent circuit of the test fixture in Fig. 10 for details).

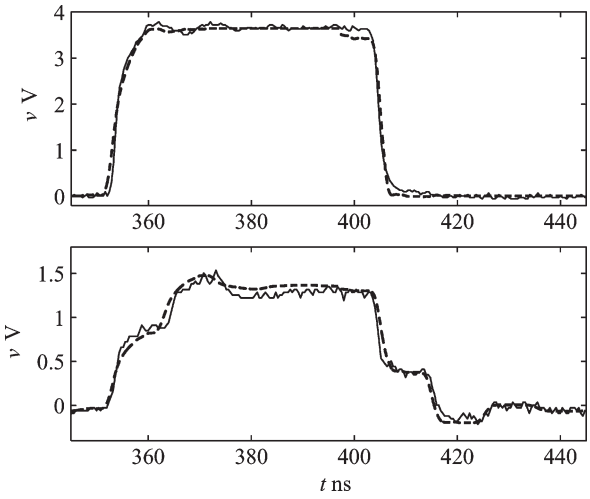

Fig. 12. (Top panel) Output port voltage waveforms of the HC7404 IC driving the series connection of R_s and a 50-Ω SMA adapter and (bottom panel) the series connection of R_s and the shunt connection between a 50-Ω resistor and a transmission line load; see text. Solid line: Measured reference response. Dashed line: Model response.

and T_2 correspond to probe tips on the back of the board that are used to record the port voltage responses $v(t)$ and $v_2(t)$, as shown in the top panel in Fig. 9. The surface-mounted device (SMD) resistor R_s has been included in the board design to allow the simplest way of computing the port current $i(t)$ from the voltage drop on a series resistor (see Fig. 10). The scope used for the transient voltage measurements is a Tektronix TDS380 with a 400-MHz bandwidth (2-Gs/s sampling rate), and the probes are passive voltage probes P6114B. In this application, the port switching times are sufficiently slow to allow the modeling of the SMD resistor by means of the ideal element R_s. However, an accurate characterization of the series resistor by means of a network analyzer is needed for devices that exhibit faster transition times. It is also worth noting that the curves required for model estimation arise from a set of perturbed port voltage and current responses and that the value of the resistor R_s has been chosen large enough to allow the computation of the voltage drop by using single-ended voltage probes. If a differential probe would be available, even a smaller, e.g., 1 Ω, resistor can be effectively used.

The signals required by the on-the-fly model estimation are obtained as follows: For the sake of simplicity, the IC is driven by means of a 10-MHz square-wave generator with adequate duty cycle, offset, and amplitude connected to its input pin (see the white wire in Fig. 9, top panel). It is worth to remark that in a real board with a more complex IC, the bit pattern produced by the output port under modeling is decided by the IC internal activity, and no signal generators are required. As outlined in the previous section, a suitable perturbing element is connected to terminal S_1, and the recorded port responses $v(t)$ and $i(t) = (v(t) - v_2(t))/R_s$ are used in place of the signals in Fig. 2 for the generation of model parameters. The perturbing element is a 77-cm-long CX 179 miniature coaxial cable (characteristic impedance $Z_0 = 75\ \Omega$) loaded by a 20-pF capacitor. Fig. 11 shows the voltage waveforms $v(t)$ and $v_2(t)$ for the aforementioned situation. The sampling period used to sample the port responses is 200 ps, and the parametric models estimated for i_H and i_L in (1) turn out to have both a dynamic order of four and are composed of three and four sigmoidal terms [3]. As in the previous example, the model is implemented as a SPICE subcircuit and is validated by predicting the responses of test circuits different from those involved in model generation.

As an example, Fig. 12 shows the measured and the predicted responses of the modeled port when the IC sends a pulse on the series connection of R_s and two different loads. In the top panel of the figure, the load considered is a simple 50-Ω surface-mounted assembly (SMA) adapter connected to terminal S_1. Similarly, in the bottom panel, the load is a 50-Ω SMA adapter shunted by an open-ended 77-cm-long CX 179 cable. The accuracy of the model is clearly appreciable. These results show that the estimated model performs at a good accuracy level, even if the measurement of identification signals and the validation are based on a rather idealized equivalent circuit of the test fixture.

IV. Conclusion

In this paper, a methodology for the development of accurate and efficient behavioral models of the output ports of digital ICs is presented. The proposed approach is based on the estimation of mathematical parametric relations reproducing the external behavior of devices from transient port voltage and current responses recorded during the normal activity of the ICs. The advocated procedure is aimed at allowing the modeling of devices from actual measurements performed on a real board, without the need for dedicated test fixtures and device control. The efficiency of the approach is demonstrated on real devices through either numerical simulations or actual measurements.

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