Behavioral Modelling of Digital Devices Via Composite Local-Linear State-Space Relations

Behavioral Modeling of Digital Devices Via Composite Local Linear State–Space Relations

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***Abstract*—This paper addresses the generation of accurate and efficient behavioral models of digital ICs. The proposed approach is based on the approximation of the device port characteristics by means of composite local linear state–space relations whose parameters can effectively be estimated from device port transient responses via well-established system identification techniques. The proposed models have been proven to overcome some inherent limitations of the state-of-the-art models used so far, and they can effectively be implemented in any commercial tool as Simulation Program with Integrated Circuit Emphasis (SPICE) subcircuits or VHDL-AMS hardware descriptions. A systematic study of the performances of the proposed state–space models is carried out on a synthetic test device. The effectiveness of the proposed approach has been demonstrated on a real application problem involving commercial devices and a data link of a mobile phone.**

***Index Terms*—Circuit modeling, digital ICs, electromagnetic compatibility (EMC), I/O ports, macromodeling, signal integrity, system identification.**

I. Introduction

NOWADAYS, the design of modern high-performance electronic systems requires, in the early stage of the design process, the accurate prediction of signals propagating on system interconnects. Such a prediction, which allows designers to perform both signal integrity analyses and electromagnetic compatibility assessments, is mainly carried out via the numerical simulation of critical interconnection paths such as high-speed serial links. Within this framework, the availability of accurate and efficient models of digital ICs plays a key role. IC port behavior can neither be considered ideal any longer nor be represented by a lumped linear termination. Hence, suitable behavioral models (or macromodels) accounting for the nonideal analog operation of device ports are required.

Device models are currently based on equivalent circuits representing a simplification of their internal structure, as suggested by the I/O Information Specification (IBIS) [1]. Recently, other approaches to IC macromodeling that complement the IBIS resource and provide improved accuracy for recent device technologies have been proposed [2], [3]. These approaches are based on the estimation of parametric relations from port voltage and current responses to a suitable set of stimuli applied to the IC ports. The parametric relations used so far for the generation of IC models have been sought for within the class of discrete-time Nonlinear Auto Regressive with eXtra input (NARX) parametric relations expressed in terms of Gaussian or sigmoidal expansions. This choice arises from the large availability of methods for parameter estimation, as well as from the nice features of these models to approximate *almost any* nonlinear dynamical system [6]. NARX parametric relations have been proven to accurately reproduce the behavior of a wide class of commercial devices [2], [3]. In addition, they turn out to be very compact, i.e., leading to models with a very small size. Owing to this, the estimated models, which were implemented in a simulation environment, are very efficient.

They allow one to speed up the simulation of the devices, with simulation times that are 10 to 1000 times faster than the those required to simulate the transistor-level models of devices. In spite of these advantages, NARX relations have some inherent limitations: 1) The stability of the models cannot easily be imposed *a priori* or even during the training process without impact on model accuracy. It is worth remarking that locally unstable models must be avoided, even if they reproduce the reference responses used in the model estimation well. In fact, numerical simulation of these models for different signal and load conditions may lead to poor results. 2) Fully nonlinear optimization algorithms are required for the computation of model parameters, and model accuracy depends on the initial guess of parameters and on the local minima of the cost function. 3) Higher order dynamical effects may not readily be represented by these models. 4) Model estimation for real devices with multiple ports is troublesome and has an impact on the quality of the estimated models. As an example, the generation of device port models, including the effects of the neighboring ports, suffers from the increase in complexity of the approximation problem.

To address the previous limitations, along with the requirement of avoiding the use of complex model structures, which have an impact on the simulation efficiency, model representations based on composite local linear state–space (LLSS) models [12] are assessed. LLSS models are nonlinear discrete-time state–space parametric equations defined by a weighted sum of linear state–space models that can effectively be used to approximate the port behavior of a nonlinear dynamic system and whose parameters can automatically be computed from system responses only. LLSS models provide a very good compromise between model accuracy and model efficiency for the modeling of real systems with a complex dynamic behavior and are good candidates to be used for the modeling problem at hand. Preliminary results on the application of LLSS models for the behavioral modeling of digital devices are reported in [16].

Manuscript received July 5, 2007; revised April 10, 2008.
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Digital Object Identifier 10.1109/TIM.2008.925343

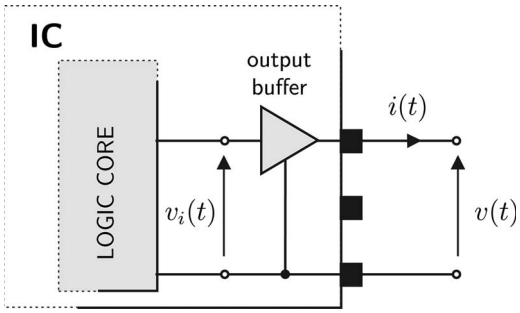

Fig. 1. Typical IC output buffer with its relevant electrical variables.

The rest of this paper is organized as follows: Section II introduces the model structures suggested in the literature for the behavioral characterization of the IC ports. Section III briefly reviews the basic theory of local linear state–space models applied to system identification problems. Section IV deals with the systematic analysis of the performances of the state-of-the art NARX relations considered so far and of the proposed state–space relations in approximating the port behavior of a test device. Finally, Section V summarizes the results on the application of the proposed approach to a real application problem involving commercial devices and a typical mobile data link. Summary and conclusions are given in Section VI.

II. Model Structure

For the sake of simplicity, the following discussion is based on single-ended output buffers, such as those shown in Fig. 1. The results, however, are extensible to input and supply ports and different device technologies [2]–[4]. A macromodel for output buffers reproduces the electric behavior of the port current $i(t)$ and voltage $v(t)$ variables and is defined by the following two-piece relation [2], [3]:

$$i(t) = w_H(t) i_H\left(v(t), d/dt\right) + w_L(t) i_L\left(v(t), d/dt\right) \qquad (1)$$

where i_H and i_L are submodels describing the nonlinear dynamic behavior of the port in the fixed high and low logic states, respectively, and w_H and w_L are weighting signals describing state transitions (they play the same role as internal nonmeasurable variables driving the buffer state).

The estimation of model (1) amounts to selecting a model representation for submodels i_H and i_L and computing the model parameters. It is worth noting that the selection of the model representation, along with a good algorithm for the estimation of model parameters, is the most critical step of the modeling process. Many possible choices are available in the literature, as shown in the succeeding sections and in past contributions on the modeling of digital devices [2]–[4].

Once the model representation for submodels i_H and i_L is selected, the model parameters are obtained by fitting the model responses to the reference device responses. As an example, Fig. 2 shows the ideal setup required to collect the device port responses carrying the information on the device behavior at fixed high output state, thus allowing the computation of the model parameters of i_H. The port responses are computed while the driver is forced in fixed high output state, and as

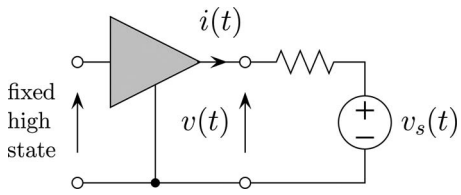

Fig. 2. Ideal setup for generation of the port responses required by the estimation of submodel i_H of (1).

suggested in the system identification literature [9], a noisy multilevel signal is used for voltage source $v_s(t)$. More details on the proper design of the estimation signals for this class of devices are out of the scope of this paper and can be found in [3].

When the submodels are identified, the computation of weighting coefficients w_H and w_L in (1) is carried out by a simple linear inversion of the model equation. This is done from voltage and current waveforms recorded during state transitions events, as suggested in [2].

Finally, the last step of the modeling process amounts to coding the model equations in a simulation environment. This can be done by representing (1) in terms of an equivalent circuit and then implementing the equivalent as a Simulation Program with Integrated Circuit Emphasis (SPICE)-like subcircuit. The circuit interpretation of model equations is a standard procedure that is based on the use of resistors, capacitors, and controlled source elements. As an example, the SPICE-like implementation of a generic nonlinear dynamic parametric model is discussed in [2] and [3]. As an alternative, model (1) can directly be plugged into a mixed-signal simulation environment by describing model equations via hardware description languages such as Verilog-AMS or VHDL-AMS.

As outlined in the introduction, NARX relations based on gaussian or sigmoidal expansions have widely been used for submodels i_H and i_L in (1). They have successfully been applied to real application problems, as demonstrated by the results published in [2]–[4]. However, to address the inherent limitations of this class of representations, the LLSS models are considered to possibly be good candidates to complement the previous relations and thus to improve the estimated models for the applications at hand.

III. LLSSs

The idea underlying the LLSS modeling methodology is the approximation of the complex dynamic behavior of a nonlinear dynamic system by means of the composition of local linear models [11], [12]. The whole operating range of the system is partitioned into smaller operating regions, where the system behavior is approximated by a linear state–space equation. Even if this idea is not completely new and has already been investigated in past literature, the implementation of [11] and [12] has several strengths, including the nice feature of providing the automatic computation of local linear models, as well as the generation of the weights for the local models from I/O system responses only.

As an example, for submodel $i_H(v(t), d/dt)$ in (1), an LLSS representation is defined by the following discrete-time

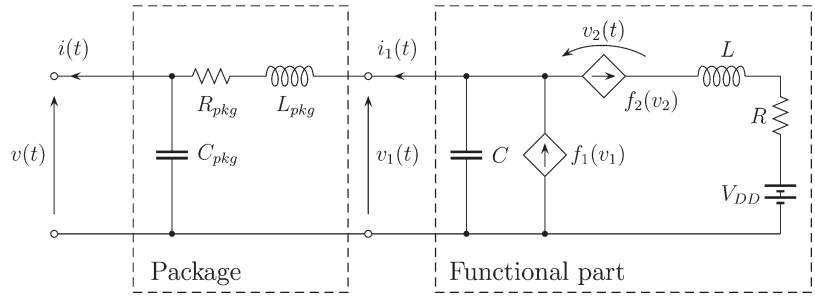

Fig. 3. Equivalent circuit defining the one-port nonlinear dynamic modeling test case in Section IV.

state–space equation:

$$\begin{cases} \mathbf{x}(k) = \sum_{j=1}^{p} \rho_j\left(\mathbf{s}(k-1)\right)\left(\mathbf{A}_j\mathbf{x}(k-1) + \mathbf{b}_j v(k-1) + \mathbf{o}_j\right) \\ i_H(k) = \sum_{j=1}^{p} \rho_j\left(\mathbf{s}(k)\right)\left(\mathbf{c}_j^T\mathbf{x}(k) + d_j v(k) + q_j\right) \end{cases} \tag{2}$$

where p is the number of local linear models, and $\rho_j(\cdot)$ is the weighting coefficient of the jth local state–space model. Each local model is defined by state matrix $\mathbf{A}_j$; vectors $\mathbf{b}_j$, $\mathbf{o}_j$, and $\mathbf{c}_j$; and scalar coefficients d_j and q_j. Vector $\mathbf{x} = [x_1, \ldots, x_n]^T$ defines the n internal states of the state–space relation. The argument of the weights, i.e., scheduling vector $\mathbf{s}(k)$, corresponds to the operating point of the system and is, in general, a function of both the input and state variables. Among the possible choices for $\mathbf{s}(k)$, a common solution in local linear modeling (also used in [11] and [12]) amounts to collecting the present and past samples of input sequence $v(k)$ only as follows:

$$\mathbf{s}(k) = [v(k), v(k-1), \ldots, v(k-r)]^T \tag{3}$$

where r is the number of past samples of the input variable. In this paper, the scheduling vector (3) of the LLSS models is chosen to be the simplest possible vector, which turns out to be composed of the present sample of the input signal only (i.e., $r = 0$).

In addition, as suggested in [11] and [12], the following normalized radial basis functions are considered for weight coefficients $\rho_j(\mathbf{s}(k))$:

$$\rho_j\left(\mathbf{s}(k)\right) = \frac{\phi_j\left(\mathbf{s}(k)\right)}{\sum_{i=1}^{p} \phi_i\left(\mathbf{s}(k)\right)} \tag{4}$$

where $\phi_j(\cdot)$ is the jth radial basis function defined as

$$\phi_j\left(\mathbf{s}(k)\right) = \exp\left(-\frac{\|\mathbf{s}(k) - \mathbf{t}_j\|^2}{\beta_j^2}\right). \tag{5}$$

Each coefficient defined by (4) varies between zero and one, and their sum is forced to be one at each operation point of the system. From (5), the parameters defining each radial basis function are its position in the space of the scheduling vector (center $\mathbf{t}_j$) and its spreading (scale parameter β_j).

Since the computation of model parameters in (2), i.e., the local model parameters in (2) and the parameters defining the weights in (5), requires the solution of a nonlinear nonconvex approximation problem, a modified version of the Levenberg–Marquardt (LM) iterative method is proposed in [12]. The basic version of this algorithm has suitably been modified to handle the nonuniqueness of a state–space representation that may cause ill conditioning of matrices during model estimation. Parameter initialization is carried out by means of a deterministic procedure, thus avoiding the dependence of the estimated model to the initial guess of parameters. In addition, the initial guess of the matrices defining the local models is set equal to the matrices of a single global stable linear model. The parameters of the global linear model are computed by means of the application of an efficient subspace identification method of the state–space subspace system identification (4SID) class [13], [14]. The latter subspace method also provides automatic computation of the number of internal state variables, i.e., the size of vector $\mathbf{x}$ in (2). In addition, the initial radial weighting functions ρ_i are uniformly distributed over the range of the input sequence. It is worth remarking that, in the proposed implementation of the algorithm, no additional constraints are included to enforce stable models during the training phase, and stability is only verified *a posteriori*. However, for the modeling problems at hand, the proposed approach has been verified to generate stable models. This is a practical advantage when the models are estimated from real measured data, where the measurement errors or possible perturbations of the measurement setup might increase the risk of obtaining unstable models exhibiting unphysical dynamical behaviors.

IV. Model Assessment

This section summarizes the results of the assessment of the performances of different possible parametric model representations that can be used for submodels i_H and i_L in (1). The representations we considered in this paper are the state-of-the-art NARX parametric relations expressed in terms of sigmoidal expansions [3], [6] (SBF models hereinafter) and the LLSS relations introduced in Section III.

The assessment is based on the synthetic one-port test device shown in Fig. 3. This example test case has been devised as a simplified device port equivalent circuit where the parameters can be tuned to create a stiff modeling example. The example test circuit behaves like a driver in a fixed high state, and it can be represented by submodel i_H in (1) only. The results of these

modeling experiments, however, apply to both submodels of the two-piece structure (1).

The reference responses of the circuit in Fig. 3, which are used for both computation of model parameters and model validation, are obtained via the implementation of the circuit equations as ordinary differential equations and the use of the standard integration functions available in the Matlab environment.

A. One-Port Test Device

The one-port test device in Fig. 3 is composed of the cascade connection of a two-port element representing a realistic package of a digital IC and a one-port element representing the nonlinear functional part of the driver circuit. The external port voltage and current variables v and i play the same role as the voltage and current signals of the output port of a driver. The package is modeled by a lumped network of elements $R_{\rm pkg}$, $L_{\rm pkg}$, and $C_{\rm pkg}$, whose values are representative for a standard package of the class TSSOP48. On the other hand, the functional part is mainly characterized by voltage-controlled current source $f_1(v_1)$, accounting for the static characteristic of the output port of a driver in a fixed high logic state. Voltage-controlled current source $f_2(v_2)$ accounts for the protection circuitry. In a real device, f_2 is a diode that contributes to reduce output current i_1 whenever port voltage v_1 is larger than power supply battery V_{DD}. Finally, capacitor C represents the equivalent port capacitance of the silicon part of the device, and R and L account for the bonding wire link between battery V_{DD} and f_2.

For the sake of simplicity, we considered $V_{DD} = 1$ V and the static characteristics f_1 and f_2 defined by the following functions:

$$\begin{cases} f_1(v_1) = a_1 - a_2 e^{-a_3 v_1} - a_4 v_1 \\ f_2(v_2) = b_1 e^{b_2 (v_2 - V_{DD})} \end{cases} \tag{6}$$

where parameters $a_{1,2,3,4}$ and $b_{1,2}$ have been tuned to approximate the characteristics of a real digital device used in high-speed data communication links (see Fig. 4). It is also worth noting that the static curve defining $f_1(v_1)$ does not include the actual behavior of real devices for voltages $v_1 < 0$ V. This simplified assumption is done since, in a real operating condition, a device in the high logic state has voltage values $v(t)$ [or, equivalently, $v_1(t)$] of larger than zero and, in general, in a region close to the V_{DD} value. To allow one to reproduce the results of this section, Table I collects the values of the parameters defining the static characteristics f_1 and f_2 of (6) and of the passive circuit elements of the test circuit.

B. Modeling Setup

Once the test circuit has completely been defined, the different selected model representations can be estimated by fitting the model responses to the reference responses. As outlined in Section II, the reference port transient responses are obtained by means of the test setup in Fig. 2, where the driver in high state is replaced by the one-port circuit element. Voltage source v_s is a multilevel signal with superimposed small noise

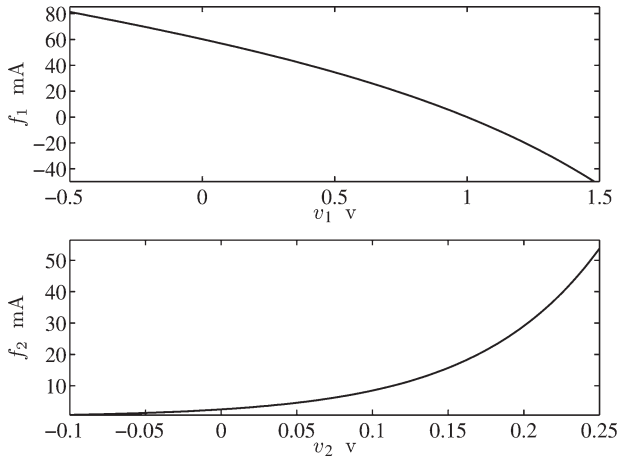

Fig. 4. Characteristics of the voltage-controlled current sources of the one-port test device in Fig. 3. (Top) $f_1(v_1)$ and (Bottom) $f_2(v_2)$ are defined by (6) and the values in Table I.

TABLE I
VALUES OF THE PARAMETERS IN (6) AND OF THE PASSIVE COMPONENTS COMPOSING THE TEST DEVICE IN FIG. 3

Parameter	Value	Element	Value
a_1	70 mA	R_{pkg}	0.5 Ω
a_2	10 mA	L_{pkg}	3 nH
a_3	1.35 V^{-1}	C_{pkg}	0.1 pF
a_4	30 $\mathrm{m}\Omega^{-1}$	R	0.1 Ω
b_1	550 A	C	5 pF
b_2	12 V^{-1}	L	1.5 nH

exciting the dynamic behavior of the device for values within all possible operating voltages. For this test, $R_s = 50\ \Omega$, and voltage source v_s is composed of 30 levels spanning the range $[0\ \mathrm{V}, V_{DD} + \Delta]$, where $\Delta = 0.5$ V is the accepted overvoltage. The superimposed signal is a white Gaussian noise with a standard deviation of 0.1 mV. The flat parts of the signal last 6 ns, which is a sufficient duration to allow the port to reach steady-state operation. The duration of different transitions is instead set to 200 ps, i.e., a typical value for the switching time of modern high-speed devices. Finally, the sampling period used to discretize the signals is $T_s = 10$ ps. Fig. 5 shows the waveform of the multilevel voltage source v_s and the corresponding device port voltage and current signals used for model parameter estimation. It is worth remarking that the values of the port voltage response $v(t)$ are within the range [0.4,1.3] V, thus confirming the hypothesis that the device is stimulated in a realistic operation region, with voltage values larger than zero and around the nominal power supply value V_{DD}.

As outlined in [3], the design of a multilevel stimulus required by the identification of nonlinear dynamical systems is a matter of repeated experiments. For the modeling of digital devices, we performed a systematic set of experiments that confirms that the quality of the estimated models is weakly sensitive to the parameters defining the multilevel signals [5]. As an example, a number of levels in the range of five to some

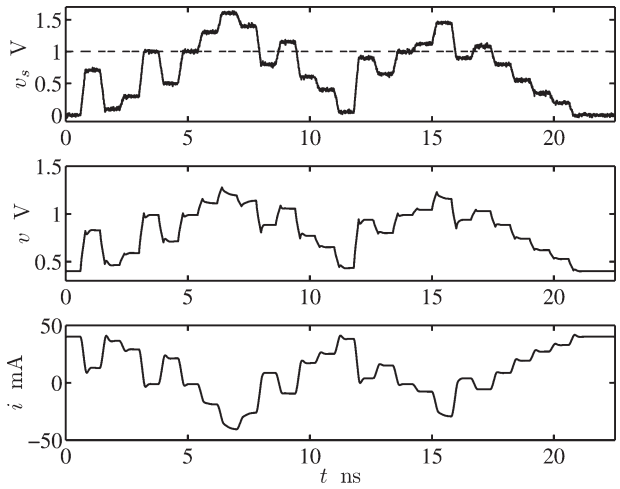

Fig. 5. (Top) Voltage signal $v_s(t)$ of the Thevenin source (estimation test) applied to the one-port test circuit in Fig. 3 and the corresponding (middle) port voltage $v_s(t)$ and (bottom) current $i(t)$ responses used for model estimation.

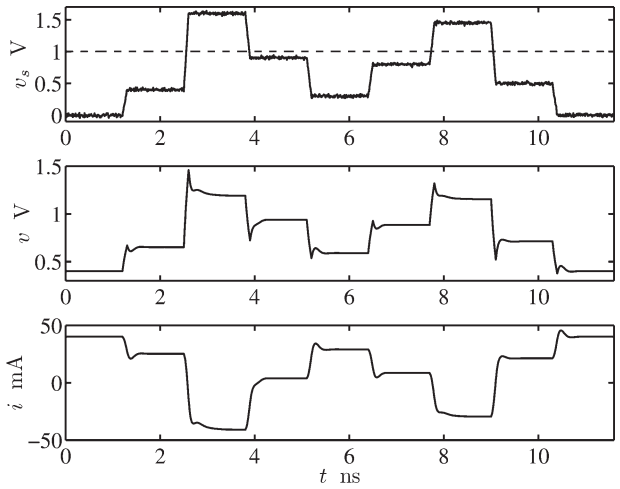

Fig. 6. (Top) Voltage signal $v_s(t)$ of the Thevenin source (validation test) applied to the one-port test circuit in Fig. 3 and the corresponding (middle) port voltage $v_s(t)$ and (bottom) current $i(t)$ responses.

tens are sufficient to yield accurate models reproducing the original system response well.

C. Parameter Estimation and Performance Assessment

The parameters of the different models have been computed from the identification voltage and current responses shown in Fig. 5 by means of the application of standard estimation algorithms selected among those available in the literature. In particular, the SBF models are obtained by applying either a static [7] or a dynamic [8] estimation routine. On the other hand, the LLSS models are obtained via the modified version of the LM algorithm outlined in Section III.

To assess the quality of the obtained models, the same test circuit in Fig. 2 is considered, where the voltage source produces a multilevel signal that is different from the one used for the estimation of model parameters. Fig. 6 shows the waveform of the multilevel stimulus $v_s(t)$ and of the corresponding port voltage and the current waveforms used as the reference signals for model validation.

As first comparison, Fig. 7 shows the reference port current response in Fig. 6 and the responses of 20 NARX models (whose estimation differs only for the random initialization of model parameters and the application of the different estimation algorithms [7], [8]). From this first test, it is clear that the SBF models produce a band of waveforms around the reference response. Even if the quality of the best model in reproducing the reference behavior of the system is good, the variability of the curves is an indication of the strong dependence of the model quality to the initial guess of model parameters. In a similar way, Fig. 8 shows the same comparison for the case of the LLSS model, thus highlighting the good accuracy of LLSS models in reproducing the reference responses of the system. For the latter case, the initialization of model parameters for the estimation of the LLSS models relies on a deterministic initialization (4SID methods [13], [14]), and the solution of the optimization problem is unique.

To point out the differences among the estimated models, Table II collects the main figures of the performances related

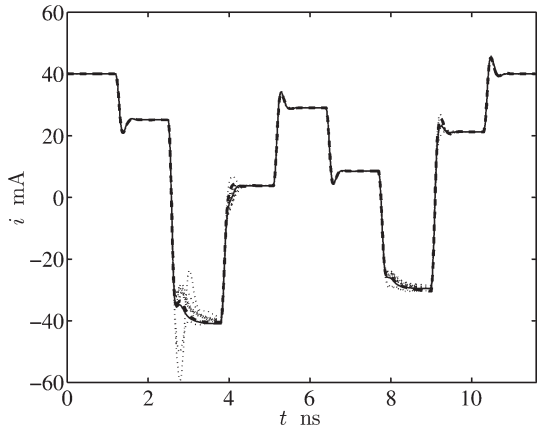

Fig. 7. SBF model validation. (Solid lines) Reference current response in Fig. 6 and responses of the 20 different SBF models in Table II (dashed line: SBF model (#3), dotted line: other SBF models).

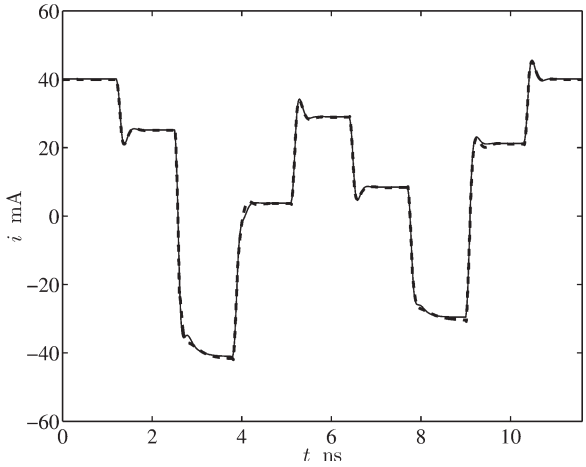

Fig. 8. LLSS model validation. (Solid line) Reference current response in Fig. 6 and (dashed line) response of LLSS model #21 in Table II.

to either the SBF or the LLSS model. Table II is organized as follows: The first two columns report the label of the estimated models (#1 to #21), the model class (SBF or LLSS), and the estimation algorithm used to compute the model parameters.

TABLE II
SBF AND LLSS MODEL PERFORMANCES. THE DIFFERENT COLUMNS (FROM LEFT TO RIGHT) CORRESPOND TO THE RUN NUMBER, MODEL CLASS, AND ESTIMATION ALGORITHM; MODEL SIZE p, i.e., THE NUMBER OF BASIS FUNCTIONS IN THE MODEL (SBF CLASS) OR THE NUMBER OF LOCAL LINEAR MODELS (LLSS CLASS); MSE BETWEEN THE REFERENCE AND MODEL RESPONSES FOR THE ESTIMATION AND VALIDATION CASES; CPU TIME REQUIRED FOR MODEL ESTIMATION; AND PERCENTAGE OF POLES WITHIN THE UNITARY CIRCLE (LOCAL STABILITY ANALYSIS [17]). THE BEST SBF MODEL #3 AND LLSS MODEL #21 ARE HIGHLIGHTED IN BOLD TEXT

Model #	Class, estim. algorithm	p	MSE (estimation)	MSE (validation)	CPU time [s] estimation	Local stability index [%]
#1	SBF, [7]	6	5.85e-9	1.12e-5	1.7	96.8
#2	SBF, [7]	10	5.46e-9	1.97e-6	15.3	99.8
#3	**SBF, [7]**	**6**	**2.02e-8**	**3.32e-7**	**22.0**	**99.7**
#4	SBF, [7]	7	2.65e-9	3.01e-6	3.0	99.1
#5	SBF, [7]	6	1.81e-8	9.90e-7	1.4	98.3
#6	SBF, [7]	9	2.93e-8	6.19e-7	15.1	99.9
#7	SBF, [7]	7	2.45e-8	1.91e-6	20.2	99.1
#8	SBF, [7]	7	2.17e-9	9.50e-7	3.6	99.7
#9	SBF, [7]	8	5.96e-9	1.22e-6	5.0	99.5
#10	SBF, [8]	9	3.58e-9	9.36e-7	2.8	98.4
#11	SBF, [8]	10	2.07e-8	1.70e-4	88.4	12.9
#12	SBF, [8]	10	1.77e-8	2.86e-5	181.5	96.5
#13	SBF, [8]	7	2.22e-8	1.26e-6	157.6	99.8
#14	SBF, [8]	10	8.56e-8	3.47e-6	91.1	37.7
#15	SBF, [8]	4	2.00e-8	3.58e-6	59.1	98.8
#16	SBF, [8]	6	2.81e-8	1.55e-6	83.2	99.7
#17	SBF, [8]	10	1.56e-8	1.62e-6	186.8	99.5
#18	SBF, [8]	9	1.80e-8	1.49e-6	175.0	98.6
#19	SBF, [8]	7	1.90e-8	7.49e-7	67.2	99.4
#20	SBF, [8]	5	5.22e-8	1.02e-6	70.3	76.6
#21	**LLSS, [12]**	**5**	**4.68e-8**	**3.24e-7**	**64.2**	**100**

The third column collects the number of sigmoidal basis functions included in the model for the SBF class or the number of local state–space models for the alternate LLSS class. It is worth noting that the number of the internal states of the LLSS model has automatically been computed during the initialization phase via the 4SID routine and turns out to be 4. The fourth and fifth columns quantify the model accuracy in reproducing the identification and the validation signals shown in Figs. 5 and 6, respectively. The accuracy is quantified by the mean square errors (MSEs) between the reference responses of the example circuit and the predicted responses. The sixth column collects the CPU time required for the model estimation (all the estimation algorithms have been implemented in Matlab on a desktop PC running at 2 GHz). Finally, the last column provides an additional performance evaluation, which is aimed at the assessment of model stability. This is done by means of the analysis of the eigenvalues of the linearized model equations. The eigenvalues are computed for each point explored by the voltage and current responses during the transient simulations of the validation test, as suggested by [17] (see the Appendix for more details). The index in Table II shows the percentage of the poles within the unitary circle of the real-imaginary plot and provides an indication on the local stability of models.

The figures in Table II highlight that the random initialization of the SBF algorithms does not affect the estimation accuracy of the SBF models since all the models have comparable values of the MSE in the estimation phase. On the contrary, the column of the MSE values computed from the validation responses shows how the pseudorandom initialization affects the accuracy of the models when they are driven by a signal that is different from the one used for the model estimation. This remark is confirmed by the validation curves in Fig. 7. For the alternate LLSS models, the very good accuracy of the estimated model is confirmed by the corresponding MSE values in Table II.

The last column, which collects the percentage of model eigenvalues outside the unitary circle, highlights that all the

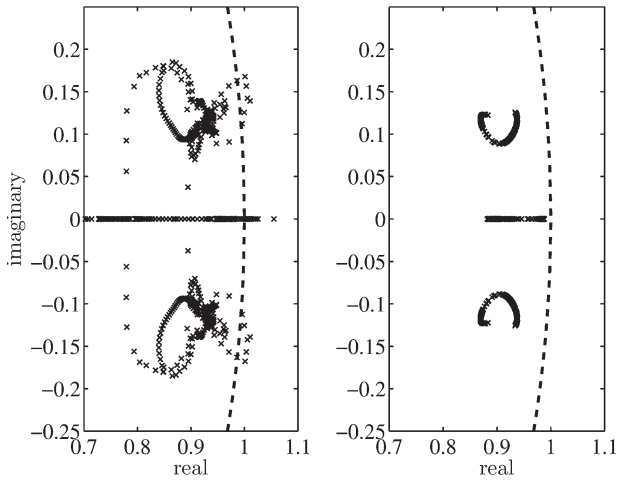

Fig. 9. (Left) Eigenvalues of linearized SBF model #3 providing the prediction shown in Fig. 7. (Right) Eigenvalues of the linearized LLSS model providing the prediction shown in Fig. 8.

TABLE III
MODEL EFFICIENCY: MATLAB SIMULATION TIME FOR THE TRANSIENT SIMULATION OF THE CURVES IN FIGS. 7 AND 8 AND THE SPEEDUP INTRODUCED BY THE SBF AND LLSS MODELS

model	simulation time	speed-up
reference	40 s	x1
SBF #3	0.2 s	x200
LLSS #21	0.35 s	x114

estimated SBF models exhibit a potential local instability during transient simulation. As an example, Fig. 9 compares the eigenloci of the linearized model equation for (left) the best SBF model labeled as #3 in Table II and (right) for the LLSS model. As expected by the indexes in the table, it turns out that all the eigenvalues of the LLSS model are located within the unitary circle and that the best SBF model has some eigenvalues lying outside the unitary circle.

The efficiency of the different models has been quantified by the CPU time required for the computation of the reference and model responses shown in Figs. 7 and 8. Table III collects the figures on the efficiency of SBF model #3 and of the LLSS model, thus confirming that both representations provide a significant speedup with respect to the reference model. On the other hand, it is worth remarking that the size (and, therefore, the efficiency) of the two classes of models is comparable (see the third column in Table II).

As a final remark, the additional strengths of the LLSS models are worth discussing. Mainly, the state–space nature of this class of representations benefits the approximation of devices with multiple inputs. This feature is extremely important for the modeling of digital ICs since the models must account for the effects of additional signals such as the enable or control voltages and the power supply voltages. Furthermore, the LLSS models have been proven to be effective for the characterization of the strongly nonlinear behavior of real devices, possibly with higher order dynamical effects [16]. These additional strengths, along with the results collected in this section, confirm the interest of applying the LLSS modeling methodology to the generation of device models that can effectively be used in a simulation environment to replace transistor-level models of devices and, thus, speed up the simulation of realistic structures.

V. APPLICATION EXAMPLE

In this section, the LLSS modeling methodology is applied to the characterization of two commercial devices involved in a real communication link. The idealized structure of the link is shown in Fig. 10. It represents an RF-to-digital communication link[1] of a mobile phone and consists of (left) a driver IC that communicates with (right) a receiver IC via a distributed interconnect and is energized by a common power supply network. A high-speed Nokia CMOS single-ended transceiver ($V_{DD} = 1.8$ V) is used for both the active devices in the figure. The interconnect is a 3-cm-long multichip module land, which is modeled as an ideal transmission line whose parameters are obtained from the information on the geometry of the structure and on the substrate information (the characteristic impedance is $Z_c = 100\ \Omega$ and the p.u.l. capacitance is $C = 5$ pF/m). The power supply network is modeled by a lumped equivalent, and no transitions or junctions are included in the transmission path, for the sake of simplicity. In the example test case considered in this application, the IC driver produces a data pattern composed of a 50-bit-long sequence with a bit time of 5 ns and a rise time of 500 ps.

Specialized macromodels for both the devices in Fig. 10 are estimated, as suggested in Section II. More details on the specific model structures for single-ended drivers and receivers, possibly including the power supply voltage fluctuations, can be found in [3]. As an example, for the driver case, the inclusion of the power supply voltage in the driver model leads to a two-piece model structure such as (1) for both the output and the supply port current, where each submodel such as i_H and i_L in (1) includes an additional input accounting for the supply voltage variable. In this paper, the macromodels are obtained from the responses of the transistor-level descriptions of the devices via SPICE simulations (the Mentor Graphics Eldo-SPICE has been used for this example). However, it is worth remarking that the modeling methodology can effectively be applied to real devices from the actual measurements of the their port transient responses, as already demonstrated in [2].

To assess the accuracy and the efficiency of the proposed models in predicting the transient voltage waveforms on the system interconnect and the supply voltage variations, the complete structure in Fig. 10 is simulated by using either the reference transistor-level models or the LLSS macromodels.

As a first test, Figs. 11 and 12 show the comparison between the reference and predicted functional voltage signals at the near and far ends of the system interconnect, respectively. Figs. 11 and 12 show part of the voltage responses picked from the complete 50-bit-long sequence. This comparison highlights the very good correlation between the reference and predicted responses, thus confirming the accuracy of the proposed models

[1]Courtesy of Nokia Research Center, Radio Technologies Laboratory, Helsinki, Finland.

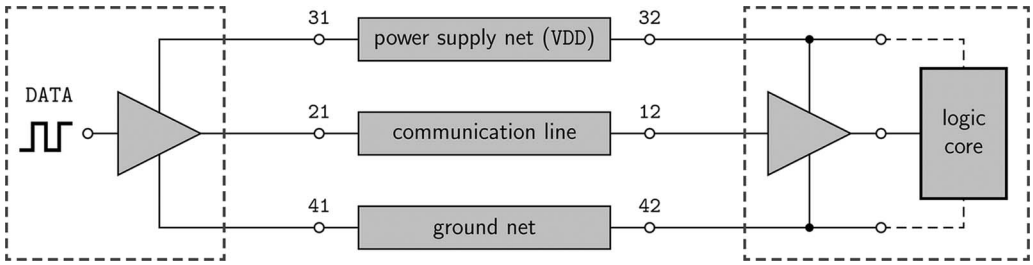

Fig. 10. Structure the application mobile data link considered in Section V.

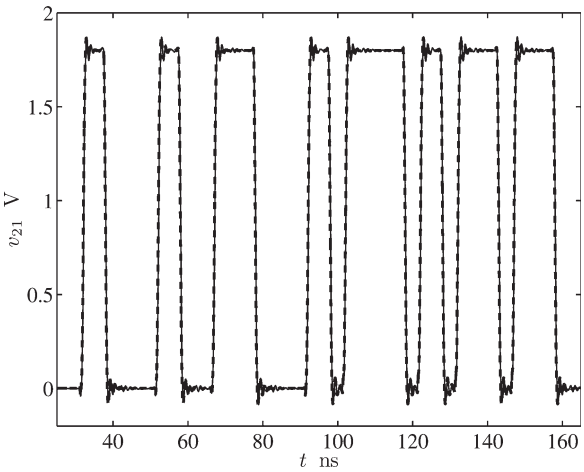

Fig. 11. Output port voltage waveform v_{21} of the driver in Fig. 10 (Solid line: reference, dashed line: prediction via LLSS macromodels).

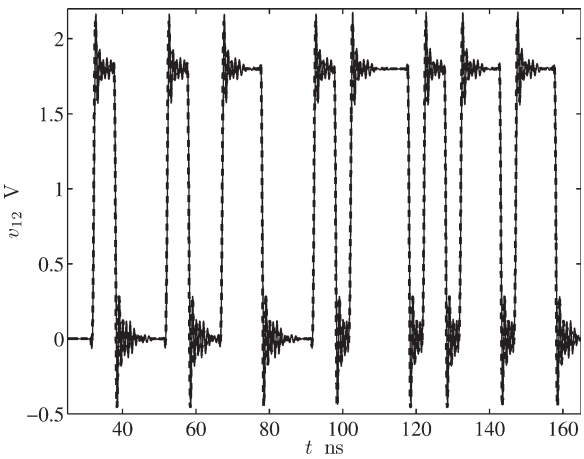

Fig. 12. Input port voltage waveform v_{12} of the receiver in Fig. 10 (Solid line: reference, dashed line: prediction via LLSS macromodels).

in reproducing the functional signals of a high-performance interconnect. It is also worth noting that the LLSS macromodels provide accurate timing information, i.e., the timing error computed as the maximum delay between the reference and predicted v_{21} and v_{12} curves in crossing the 0.9-V threshold turns out to be always less than 2% of the bit time. As an additional test, Fig. 13 shows the reference and predicted fluctuations of supply voltage signal v_{31}, thus also confirming a good agreement of the predictions for the assessment of power-bounce analysis.

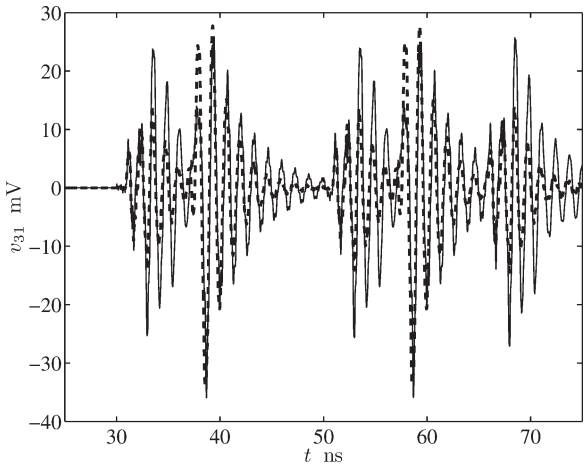

Fig. 13. Fluctuation of power supply voltage v_{31} of the driver in Fig. 10 (Solid line: reference, dashed line: prediction via LLSS macromodels).

TABLE IV
CPU TIME REQUIRED BY THE SIMULATION OF THE SETUP IN FIG. 10 (SEE TEXT FOR DETAILS)

Macromodel (Eldo)	Simulation time
Transistor-level	36 min 26 sec
LLSS Macromodels	1 min 45 sec

Finally, Table IV collects the CPU time required by the Eldo simulation of the structure in Fig. 10, where the devices are represented by either the reference transistor-level models of devices or the proposed macromodels. From this comparison, it is worth remarking that the LLSS macromodels can effectively be used to handle the complexity of realistic structures. For this example application, they introduce a simulation speedup of 30× with respect to the transistor-level models.

VI. CONCLUSION

This paper addresses the generation of accurate and efficient behavioral models of digital devices. The nonlinear dynamic port behavior of a digital IC is approximated by means of composite local linear state–space models, whose parameters are computed from device responses via a well-established technique. The obtained models are implemented as SPICE subcircuits or hardware descriptions such as VHDL-AMS. A systematic study aimed at the assessment of model performances is carried out on a synthetic test device, and the feasibility of the approach for the modeling of real devices

has been demonstrated by applying it to the characterization of commercial devices used in a mobile data link.

APPENDIX

This Appendix briefly summarizes the local stability analysis of the discrete-time LLSS models defined by (2). A similar procedure can be applied to the alternate class of NARX models defined by sigmoidal expansions [3], [6]. For conciseness, the discussion is based on the LLSS model only. Starting from the state–space relation (2), a first-order Taylor approximation of the state equation is computed:

$$\mathbf{x}(k) \approx \mathbf{x}(k) + \mathbf{A}\Delta\mathbf{x} \tag{7}$$

where $\mathbf{x}(k)$ is the state vector at the current time sample, $\Delta\mathbf{x}$ is a generic incremental vector, and $\mathbf{A}$ is the square matrix describing the first-order term, which is given by

$$\mathbf{A} = \sum_{j=1}^{p} \rho_j \left(\mathbf{s}(k-1)\right) \mathbf{A}_j. \tag{8}$$

It is worth noting that (8) is valid under the assumption that only the present and past samples of the input variable are included in scheduling vector $\mathbf{s}(k)$.

The local stability analysis is then performed by computing the eigenvalues of matrix $\mathbf{A}$ and by representing the eigenvalues in the complex real-imaginary plane. An LLSS model exhibits potential local instability if some eigenvalues of $\mathbf{A}$ have a magnitude that is smaller than one, i.e., they lie on the complex plane outside the unitary circle.

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